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Mezzanine Cards for the EMU CSC System Upgrade at the CMS

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In this paper we discuss two ideas related to the design and application of mezzanine cards in the Endcap Muon (EMU) Cathode Strip Chamber (CSC) electronic system at the CMS experiment at CERN. The first is a proposal to upgrade the FPGA-based mezzanine cards using the most advanced Xilinx Virtex-5 family of FPGA. The second is related to design of a simple and compact mezzanine card with a commercial serializer/deserialzer device and industry standard pluggable optical or copper transceiver module. Such a card could be a basic element of the general purpose gigabit data transmission link.

Summary

The CSC detector comprises 468 six-layer multi-wire proportional chambers arranged in four stations in the Endcap regions of the CMS. Its Triggering and Data Acquisition systems consist of more than 14,000 electronic boards with approximately 4,500 Xilinx FPGA devices. More than 1,000 FPGAs are mounted on custom mezzanine cards that have been produced and installed on host boards of five types. The host boards reside directly on chambers, in the 9U crates on the periphery of the return yokes and in the Track Finder crate in the underground counting room. The mezzanine approach allows us to independently design, develop and upgrade the FPGA-based processing logic while preserving the host board functionality. The present electronic system is based on mature Virtex-E and Virtex-2 technologies. The new and most advanced family of Xilinx FPGA, the Virtex-5, offers several advantages over previous generations, including higher performance, lower power consumption, more flexible basic slice block, better clocking routing, more embedded memory. We have targeted two of our existing FPGA projects, the Muon Port Card and the Muon Sorter, to the Virtex-5 XC5VLX family of FPGA. The results of simulation show an increase in performance of ˜50% for the same speed grade device. The ability of the new FPGA family to self-correct single event errors and report double errors is essential for the future SLHC upgrade.

The mezzanine approach can also be applied to data transmission links. The main parts of a typical serial digital link include the serializer (SER) and optical or copper transmitter on a transmission end and the optical or copper receiver and deserializer (DES) on a receiver end. In many cases the SER and DES functions are combined in a single SERDES device. Optical modules are typically transceivers; among industry standards in the range from 1Gbps to 4Gbps the most popular is the Small Form-factor Pluggable (SFP) standard. In addition to optical, copper SFP modules (either passive or active) are also available. The idea of combining a SERDES device and a pluggable transceiver on a mezzanine card is not new, but existing implementations usually require relatively large space. Since both the Texas Instruments TLK family of SERDES devices and the SFP standard have significant potential for future projects, including the SLHC upgrade, we have decided to build a simple, compact and inexpensive mezzanine card using these components. Several pin compatible TLK devices support serialization and deserialization of 16- and 18-bit parallel data from 25MHz to 156.25MHz with the industry standard 8B/10B or start/stop encoding, provide either current- or voltage-mode serial interface and have an embedded PRBS generator. We describe this mezzanine card in detail in the paper. Sample boards with the TLK1501/2501/3101 devices are available for evaluation.

Primary authors: Mr MATVEEV, Mikhail (Rice University); Mr PADLEY, Paul (Rice University)

Presenter: Mr MATVEEV, Mikhail (Rice University)

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