



Technologies for a DC-DC ASIC

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Outline

- Survey of available technologies
 - Specifications
 - Comparative table
- Radiation results on 0.35μm technology
 - High Voltage transistors
 - “Logic” low voltage transistors
- Plan for the future

Technology Specifications

- Both high-voltage (for power switching) and low-voltage (for control circuitry) have to be available on the same chip
- High-voltage (15-20V) transistors
 - For radiation:
 - Thin gate oxide – 8nm or (much better) less
 - For performance:
 - Small on-resistance per unit width
 - Small gate capacitance to both source and drain
- Low-voltage transistors
 - For radiation:
 - Thin gate oxide – 8nm or (much better) less

Comparative table

- Offer mainly driven by automotive applications

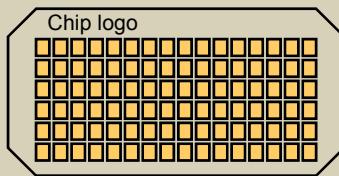
Technology node	Transistor type	Vds max (V)	Vgs max (V)	t ox (nm)	Ron*um (kOhm*um)	Cgs/um (Vds=0, Vgs=0) fF/um	Cgd/um (Vds=0, Vgs=0) fF/um	Ron*Area (mOhm*mm ²)
0.35	80V vertical	80	3.63	7	33	1.5	8.5	450
	80V vertical A	80	3.63	7	18	6.25	18.75	450
	14V lateral	14	3.63	7	8	20	32.5	37
0.35	50V lateral	50	3.6		27	7		45
0.18	20V lateral NFETI20T	20	1.8	4.45	9.3	7		30-46
	25V lateral NFETI20M	25	5.5	12.5	14	3.71		57-91
	25V lateral NFETI20H	25	20	52	6.7	1.41		26-38
	NMOS logic	1.8	1.8	3.5	1.55	0.825		
0.18	20V lateral	20	5.5	12	4.75	1.6	0.34	10
0.13	20V lateral	20	4.8	8.5		2.534	1.56	14.2

AMIS I3T80 technology

- Chosen 2 years ago as first technology to be studied for its large offer of devices (both lateral and vertical high-V transistors)
- It has been used for first DC-DC prototype (see poster by S.Michelis)
- Its radiation tolerance has been studied in detail

Test vehicle

- Dedicated set of test structures developed by CERN and manufactured in the AMIS I3T80 technology (typical W of high-V transistors is 80um)



- Large transistors (W=10cm) compatible with sizing required for power switches in DC-DC converters have also been designed
- Type of devices studied:
 - High-voltage transistors:
 - Vertical NMOS (rated 80V V_{ds}, 3.3V V_{gs}), standard and ELT layout
 - Lateral NMOS (rated 14V V_{ds}, 3.3V V_{gs}), standard and ELT layout
 - Lateral PMOS (rated 80V V_{ds}, 3.3V V_{gs})
 - Low-voltage (“logic”) transistors, standard and ELT layout for the NMOS

Irradiation sources and procedure

X-rays (for TID studies)

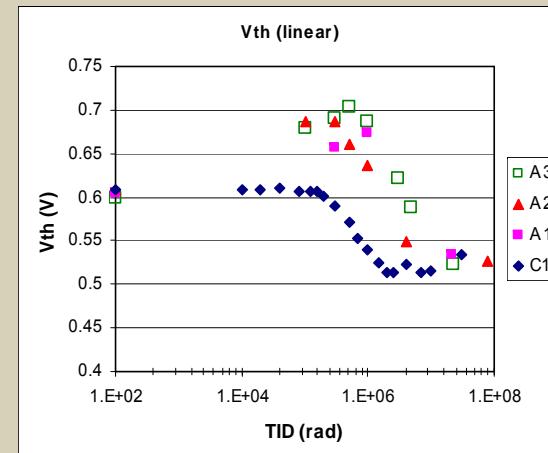
- Test performed with 10keV machine @ CERN, 20-30 krd/min, room T
 - Bias and measurements through dedicated probe card (use of probe station)
 - Bias:
 - PMOS all terminals grounded
 - NMOS
 - High-V: Vg=3.3V, all other terminals grounded; Vg=2V, Vd=14V, all other terminals grounded
 - Measurements immediately after each irradiation step
- Protons
- 24GeV/c beam at CERN PS (no bias, room T)
 - 5MeV beam at Legnaro National Laboratories (It) (no bias, room T)
 - Measurements after weeks to allow for induced radioactivity levels to drop
 - Measurements made at 3 fluences – see table below
- Results shown for W=80um unless indicated otherwise

Fluence (p/cm ²)	Source	Equiv TID	Equiv NIEL (1MeV neutron equivalent)
3x10 ¹⁴	5MeV LNL	166 Mrd	5.8x10 ¹⁴
9x10 ¹⁴	24GeV/c CERN	29 Mrd	4.5x10 ¹⁴
5.2x10 ¹⁵	24GeV/c CERN	166 Mrd	2.6x10 ¹⁵

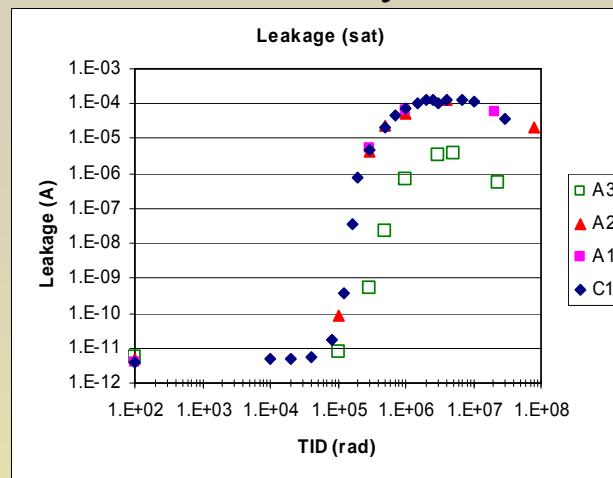
High-V_{th} lateral NMOS transistors (1)

X-ray irradiation results (TID only)

- V_{th} shift $\approx 80\text{mV}$, acceptable
- Large leakage in standard layout transistors, eliminated by ELT layout
- R_{on} increase $\sim 10\%$



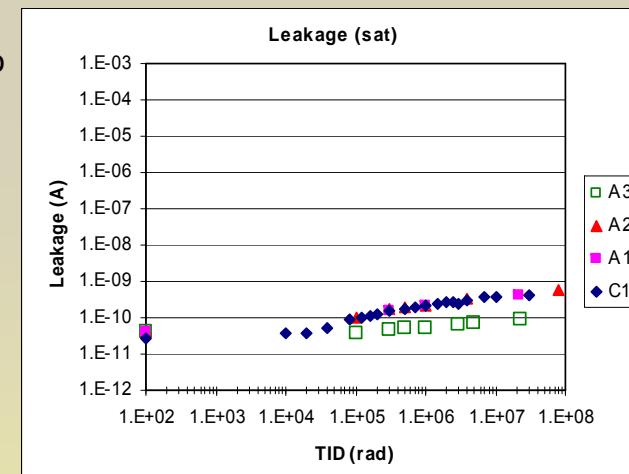
Standard layout



Layout modified to
eliminate edges
(Enclosed Layout
Transistor)



ELT

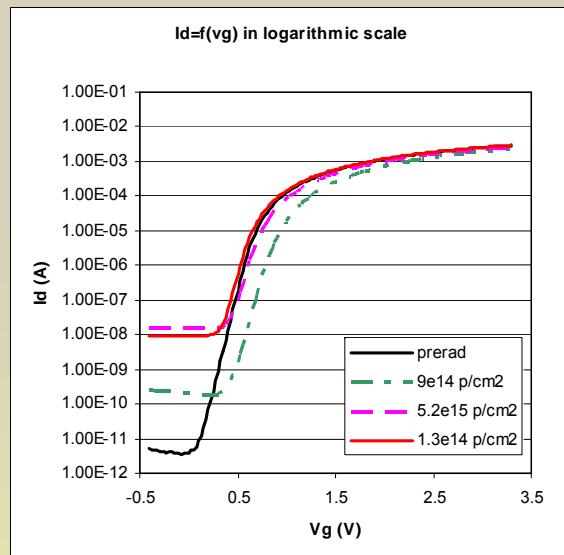


High-V lateral NMOS transistors (2)

Proton irradiation results

Standard layout

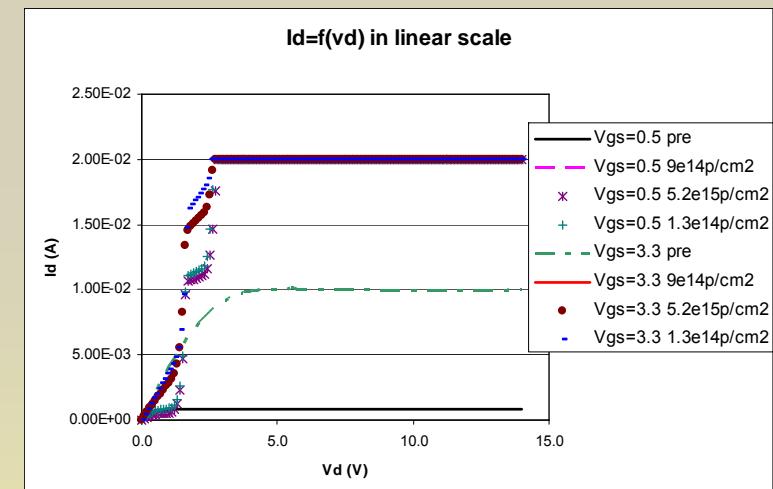
- V_{th} shift $\approx 300\text{mV}$ max
- Leakage increase observed and attributed to TID
- R_{on} increase $\sim 45\%$ max



Layout modified to eliminate edges (Enclosed Layout Transistor)

ELT

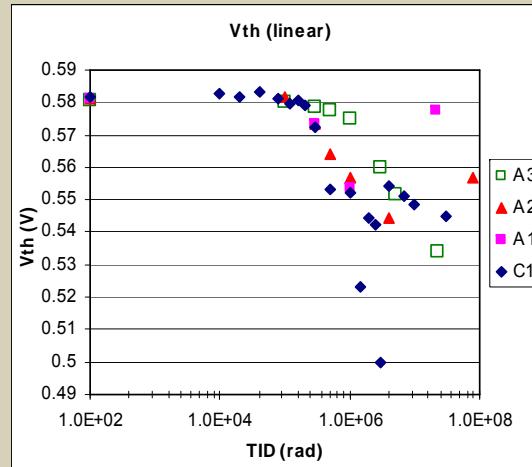
- All transistors (but one) do not work correctly anymore => unable to keep high V_{ds}
- Current bulk-drain observed
- Layout modification affected voltage rating after NIEL



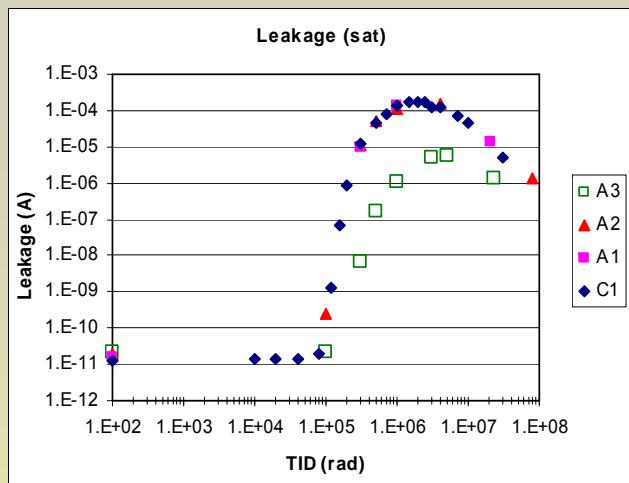
High-V vertical NMOS transistors (1)

X-ray irradiation results (TID only)

- V_{th} shift $\approx 80\text{mV}$, acceptable
- Large leakage in standard layout transistors, eliminated by ELT layout
- R_{on} increase $\sim 10\%$

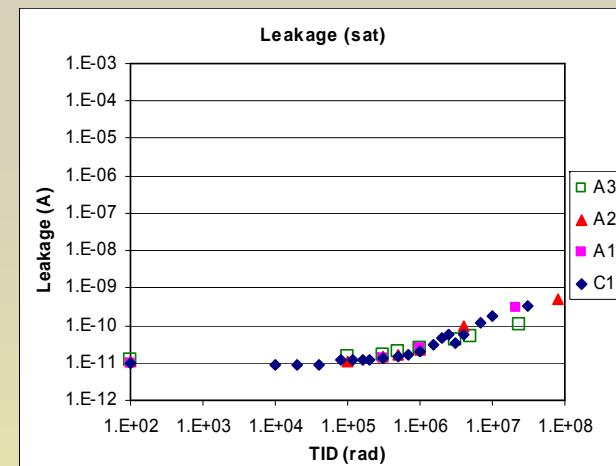


Standard layout



Layout modified to
eliminate edges
(Enclosed Layout
Transistor)

ELT

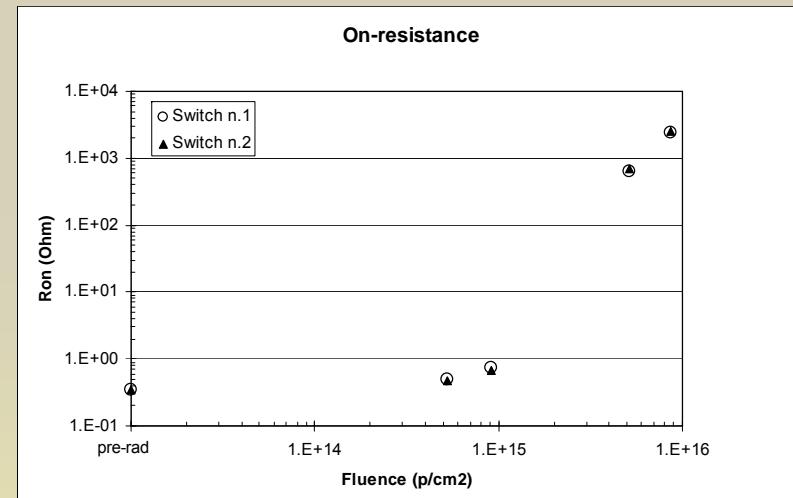
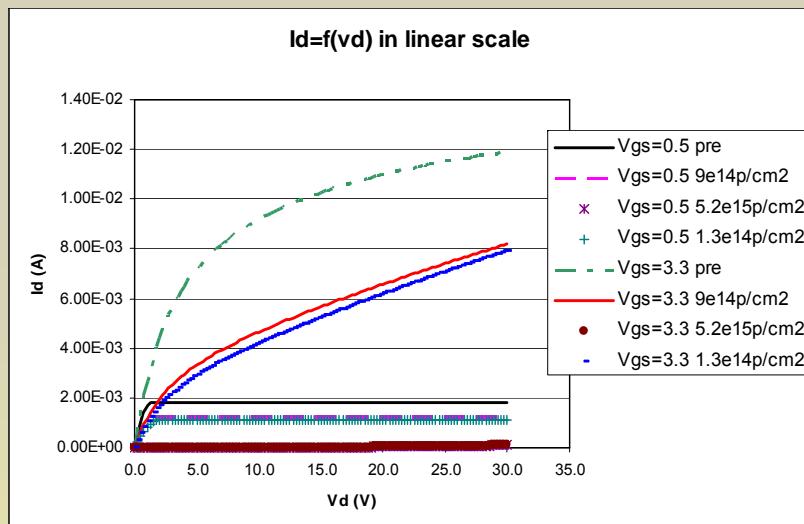


High-V vertical NMOS transistors (2)

Proton irradiation results

Standard and ELT layout

- Large increase of R_{on} with NIEL
- Comparable results for same NIEL (but very different TID) => displacement damage in the lowly doped n epitaxial layer
- Not compatible with SLHC requirements

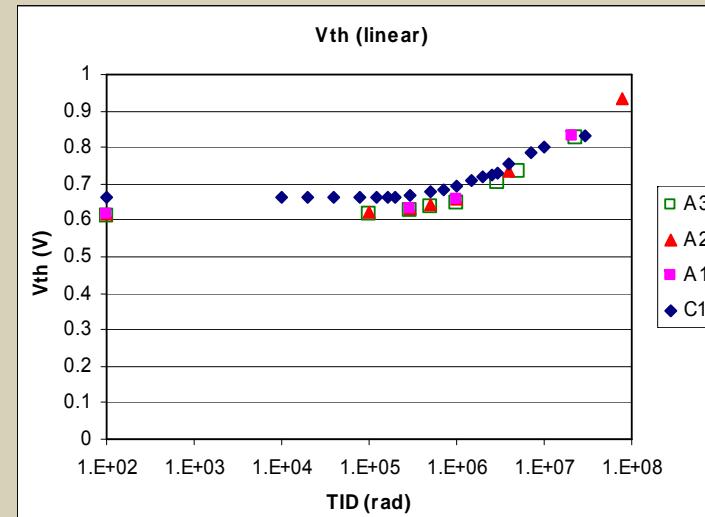


24GeV/c proton irradiation impact on vertical NMOS transistors with $W=10\text{cm}$

High-V_t lateral PMOS transistors

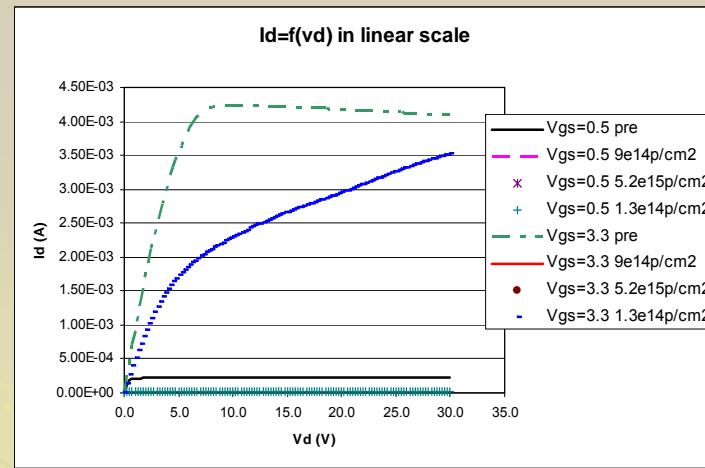
X-ray irradiation results (TID only)

- Large V_t shift with TID
- No leakage current as expected for PMOS transistors
- R_{on} increase ~ 25%



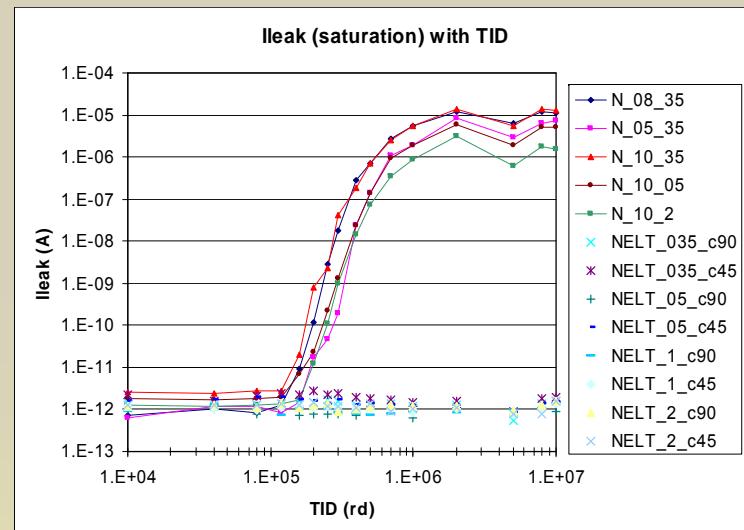
Proton irradiation results

- TID-induced V_t shift
- Large increase of R_{on} (2x after ~ 5×10^{14} 1MeV n equivalent/cm²)



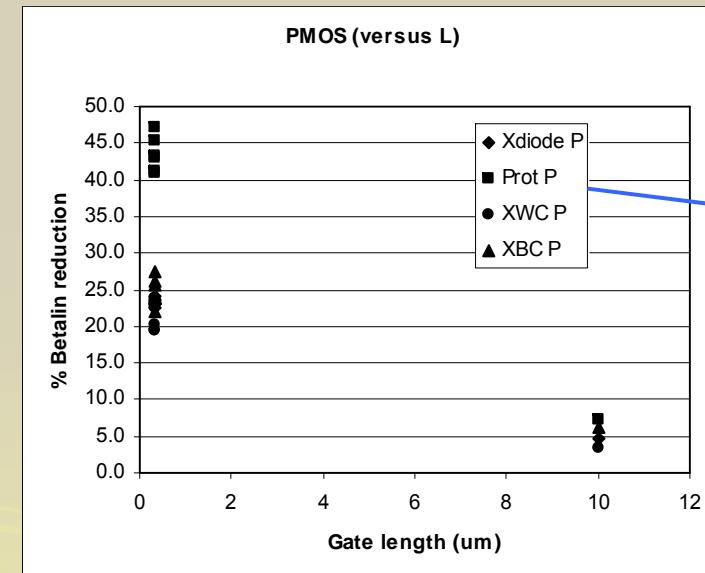
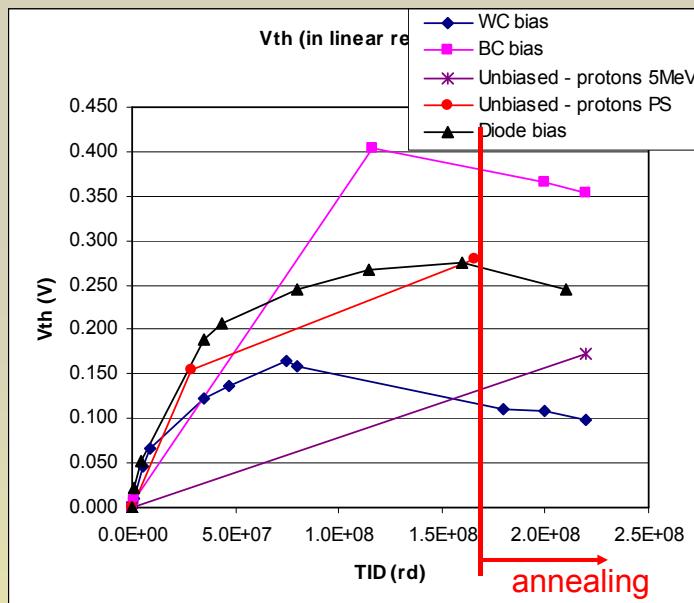
Low-voltage transistors (1)

- Large increase of NMOS leakage current starting around 200 krd => need for ELT



Low voltage transistors (2)

- NMOS ELT
 - V_{th} shifts by ~ 30-50mV
 - Beta decreases by up to ~ 25%
- PMOS
 - Much larger V_{th} shifts (order of 150-400mV)
 - Beta can decrease by up to 45% for short channel transistors and proton irradiation



X=X-rays
Prot = protons
WC = Worst case
BC = Best case

Conclusion on AMIS I3T80

- High voltage transistors
 - Only the lateral NMOS could possibly be usable if appropriate enclosed layout can be found (or relying on thermal annealing effects of leakage current....)
 - Electrical performance are not excellent to start with for our application (large C_{gd}), then worsen with irradiation (R_{on} increases by up to 45%)
- Low voltage transistor
 - PMOS transistors are sensibly affected by irradiation in terms of both V_{th} (large shift up to 400mV) and beta. This should be carefully considered in the design
- A more advanced technology, with thinner gate oxide, has better chances to meet our requirements
- For our present converter prototypes, we still use this technology which is relatively well known and has stable design kit

Future plans

- Characterize the natural radiation tolerance of other available technologies:
 - 0.18 um (2 manufacturers) and 0.13 um technologies
- Evaluate in each technology the possibility to modify the layout to increase radiation tolerance
- Continue to survey the market for new and more advanced technologies
- Eventually move the converter design to the best technology found