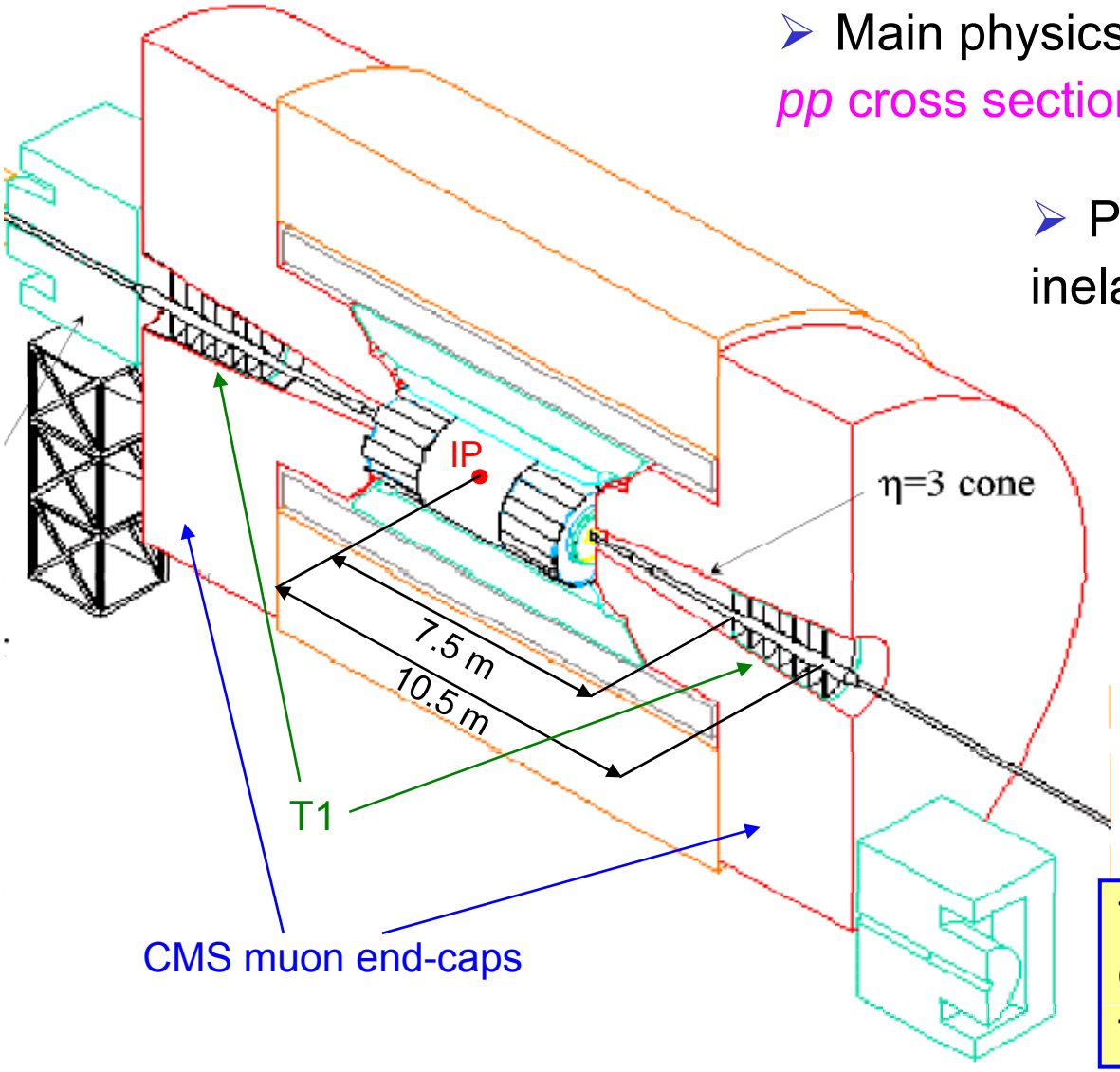
The TOTEM T1 Electronics System.

On behalf of T1 collaboration group

The T1 telescope



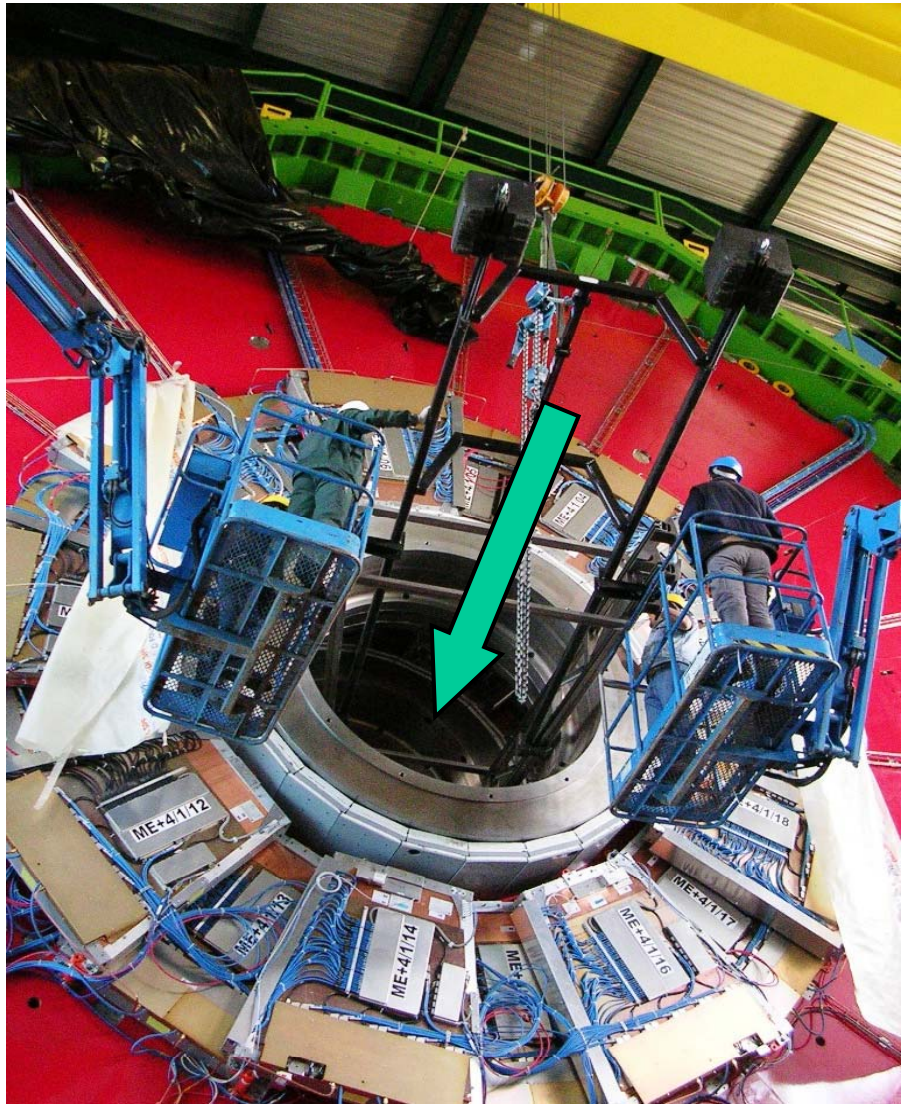
- Main physics context: measurement of the total *pp* cross section

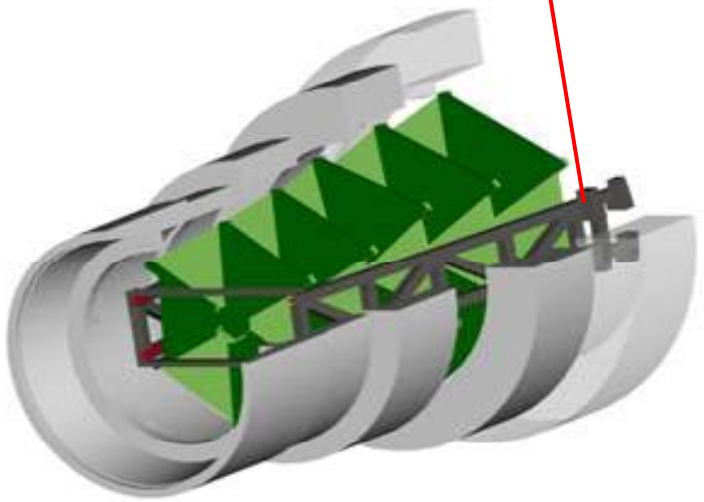
- Primary goal: detect particles from inelastic scattering processes (including single-diffractive and double-diffractive events) in the region $3.1 < |\eta| < 4.7$

- Placed inside the CMS muon end-caps, around the conical section of the beam pipe at $\eta = 4.9$

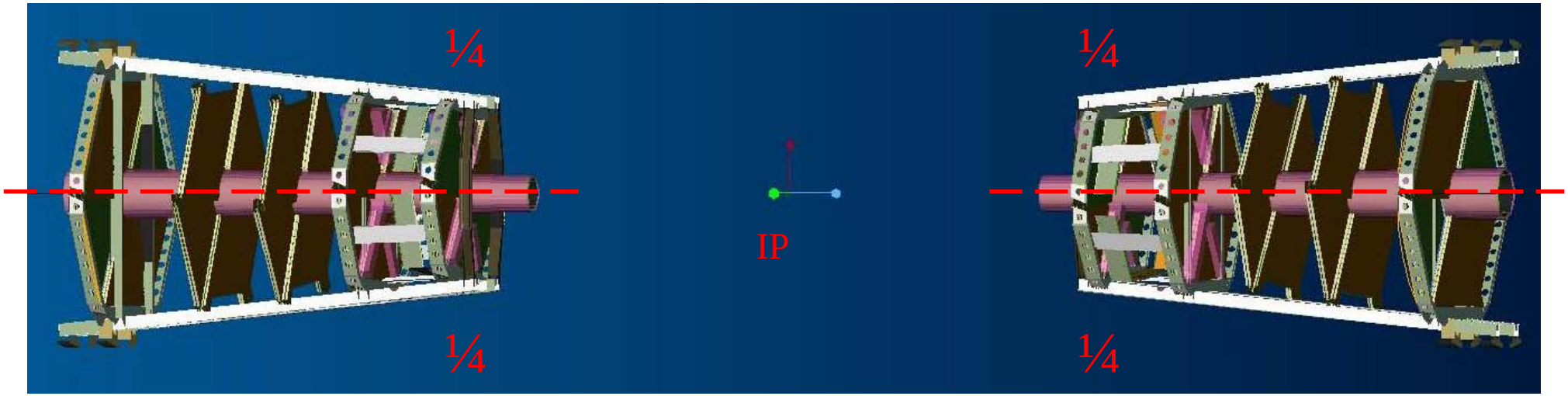
TOTEM has 3 separate and distinct detector technologies used within the three detector systems; RP, T1 and T2.

T1 support installation for the CMS magnet test





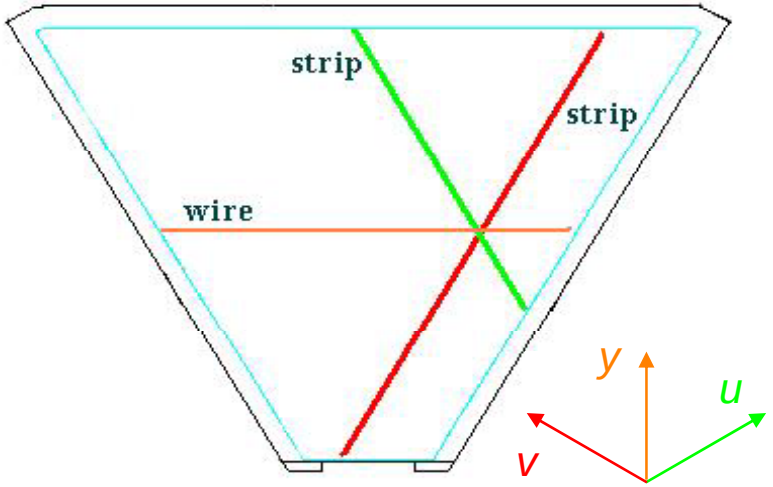
General structure



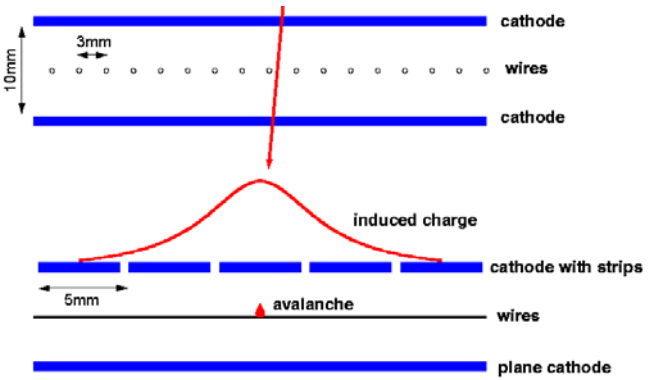
- Two symmetric arms, each with five planes of multi-wire proportional chambers with cathode strip read-out (CSC)
  - split in two half-arms, independently sliding on the support structure
- Each plane made up of 6 independent trapezoidal CSC:
  - overlapping edges to have complete azimuthal coverage;
  - planes slightly rotated with respect to each other
- For mechanical reasons, each arm is divided into two halves : each half is considered independent to the other also from electrical/logical point of view.
- In total, each halve include 15 chambers.

Chamber design

- Design similar to CMS muon chambers
- Each chamber is realized by 1 anode and 2 cathode planes.
- Chamber volumes:
  - 10 mm gap;
  - 10 different sizes (two smaller chambers in each plane to make place for rails)
- Anodes:
  - 30 μm Ø gold-plated tungsten wires;
  - pitch: 3 mm;
  - tension: 120 g
- Cathodes:
  - gold-plated copper strips on both planes at ±60°
  - pitch: 5 mm;
- Gas:
  - Ar/CO2/CF4 mix

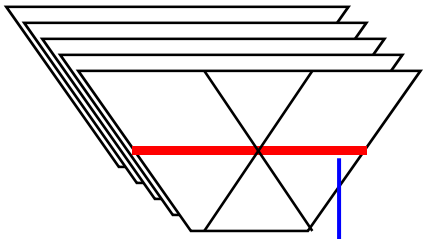


Read-out of anode wires and cathode strips at ± 60º

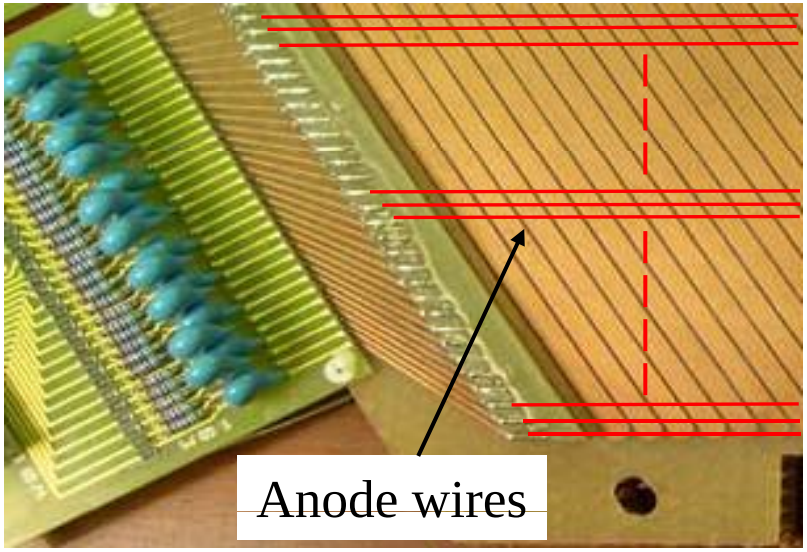


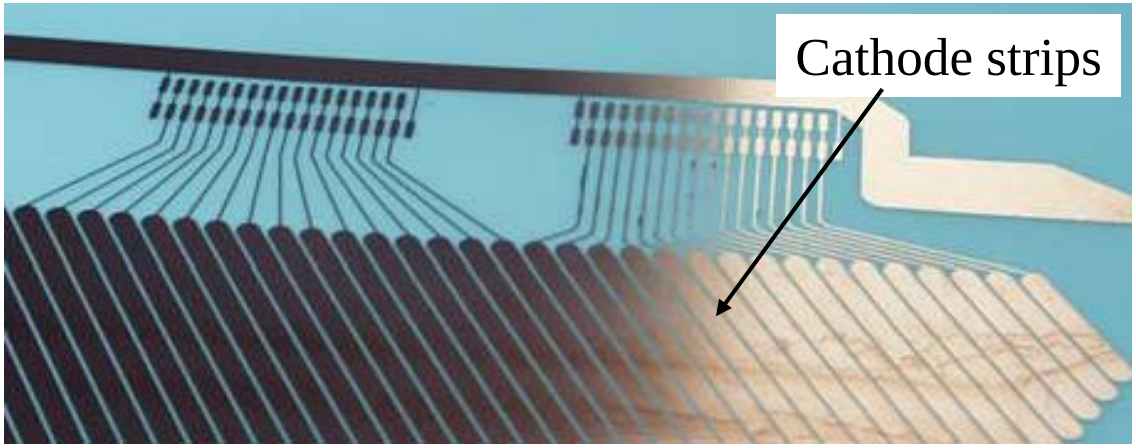
Chamber read-out

- All wires and strips read out independently
  - Anode Front End Card (AFEC)
  - Cathode Front End Card (CFEC)
- Both wires and strips will be read out digitally
  - No zero suppression.
- Trigger primitives formed from η-wise groups of wires



1 trigger bit = 16 wires





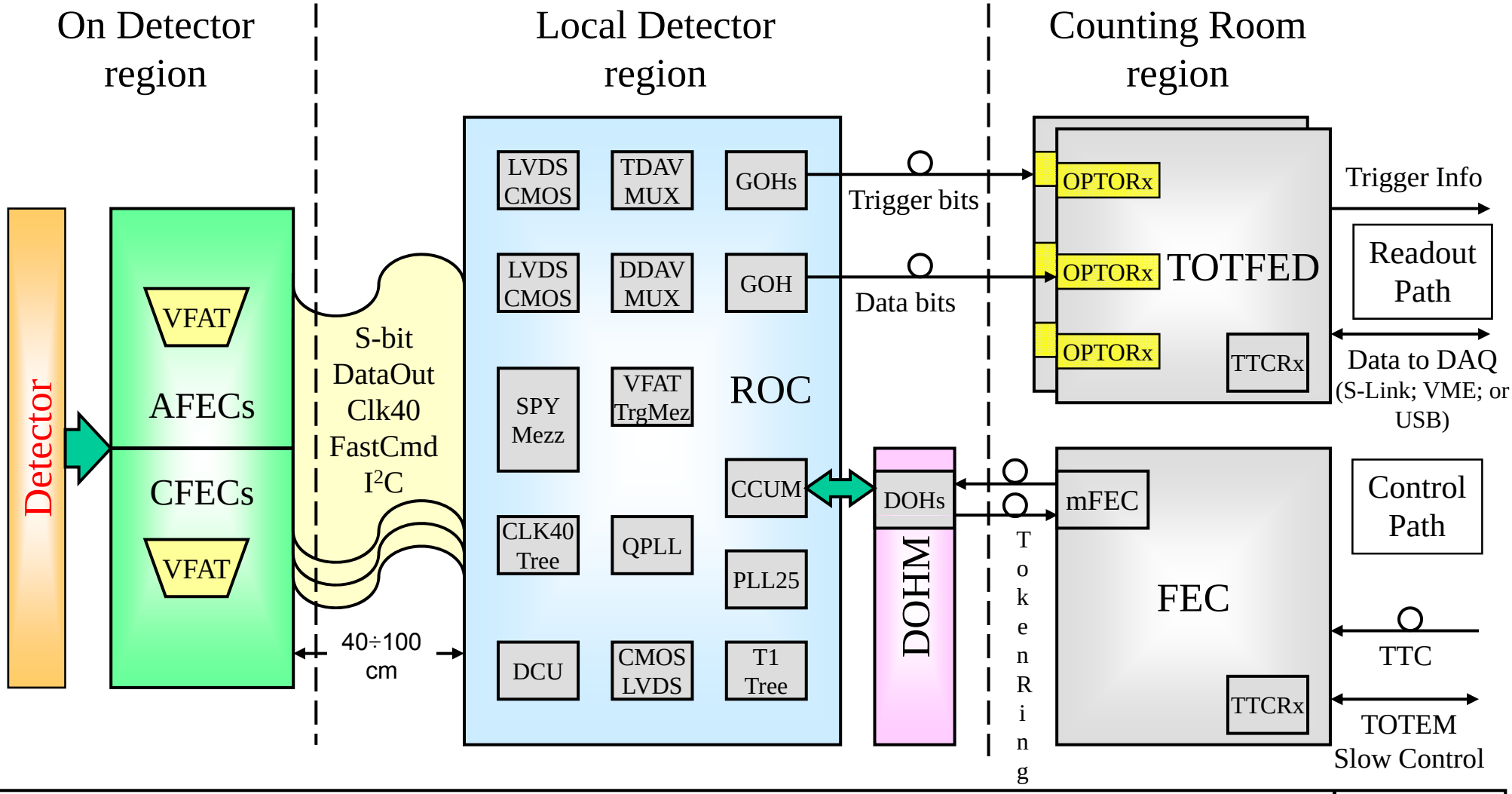
Detector / Electronics Requirements

- Each TOTEM detector system has it's own physically separate electronics
  - each system is made following one common system architecture.
  - benefits of reducing design effort by using common electronic components, data formats and DAQ software.

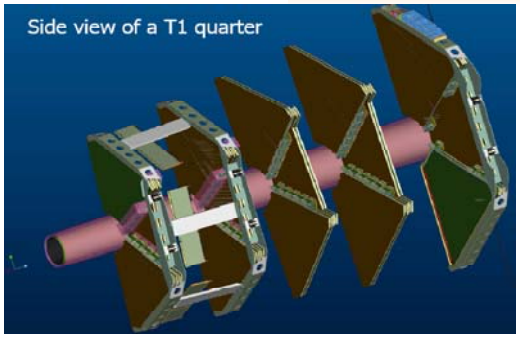
	Roman Pots	T1	T2
Number and type of detectors	240 Si strip detectors	60 Cathode Strip Chambers	40 Gas Electron Multipliers
Number of channels .	122880 .	11124 anodes 15935 cathodes	62400 pads 20480 strips
Number of VFATs	960	480	680
Typical input charge	~4fC	~50fC	~50fC
Channels/trigger sector	32	16 or less	15
Number trigger sectors	768	960	416
Radiation dose	< 10 Mrad	< 50 Krad	< 50 Mrad

- The signal properties vary considerably between detectors
  - it was decided at an early stage to design one common front-end ASIC (VFAT) that would be capable to provide the charge readout for all detectors.
  - VFAT provides a common data format and common control and readout needs in the electronic system for all 3 detectors.

T1 functional electronics system architecture



T1 FE Electronics sub-system overview



DOHM-CCU

SLOW CONTROL RING

T1-CK40
4 x I²C

GOL

ROC

3

2

1

Distributed Patch Panel

Distributed Patch Panel

12

12

In-line Patch Panel

In-line Patch Panel

96

96

TRG TOTFED

DATA TOTFED

40cm

25cm

100cm

CSC Plane_n+1

6xCFEC = 2x192chs

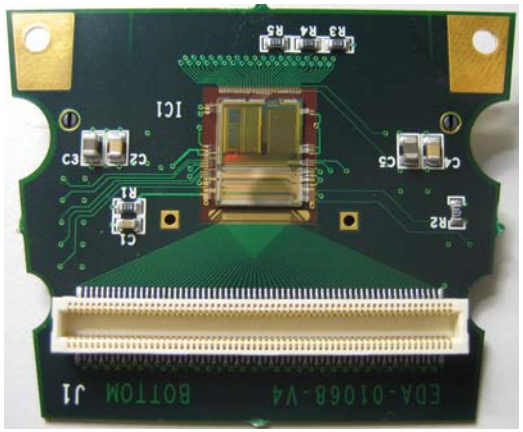
AFEC 220chs

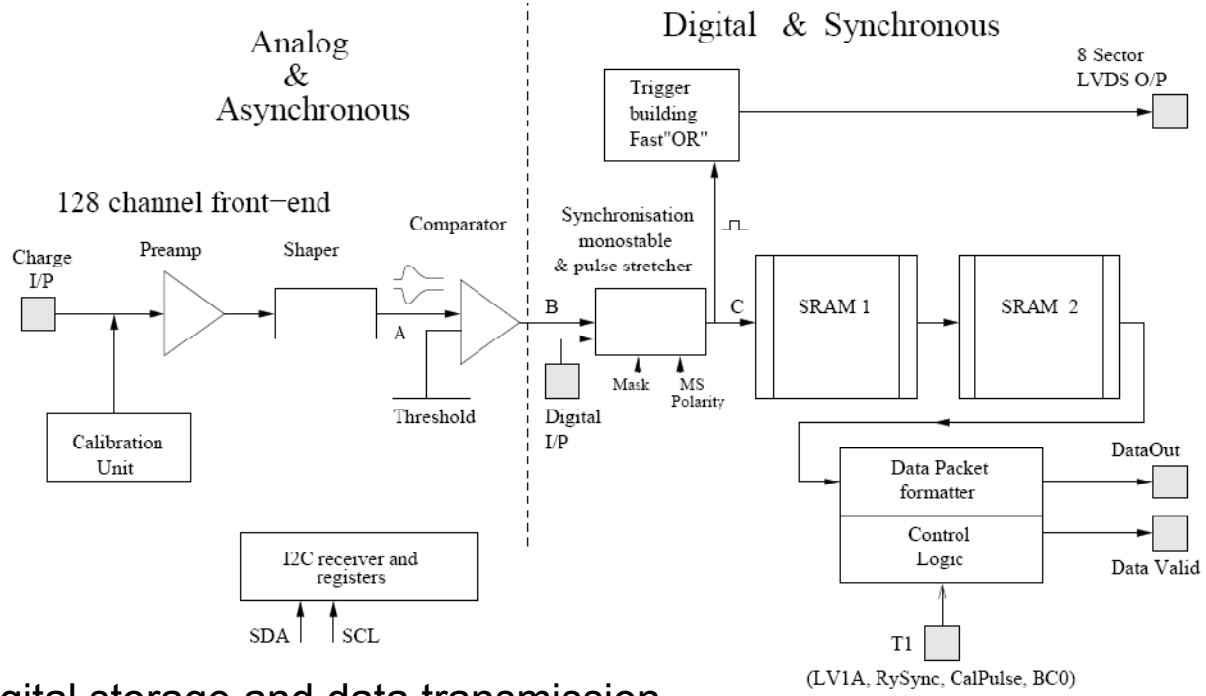
50cm

CSC Plane_n

TOTEM - VFAT block diagram

P. Aspell et al.
TWEPP 2007



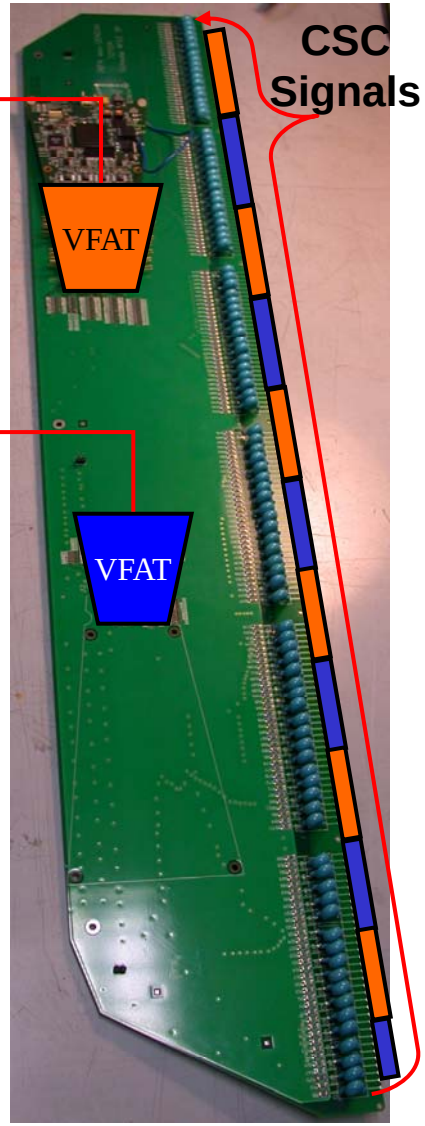


- 128 analog input channels with digital storage and data transmission
  - very low noise pre-amplifier and a 22 ns shaping stage plus comparator.
- SRAM enables trigger latencies of up to 6.4 μs and storage of data for up to 128 triggered events.
- Programmable functions controlled through an I2C interface
  - Calibration unit allows delivery of controlled test pulses to any channel for calibration purposes.
  - Programmable threshold discriminators and monostable stage before hit storage within SRAMs.
  - 8 programmable trigger sector outputs; channels mask
- Designed for radiation tolerance; low power

AFEC

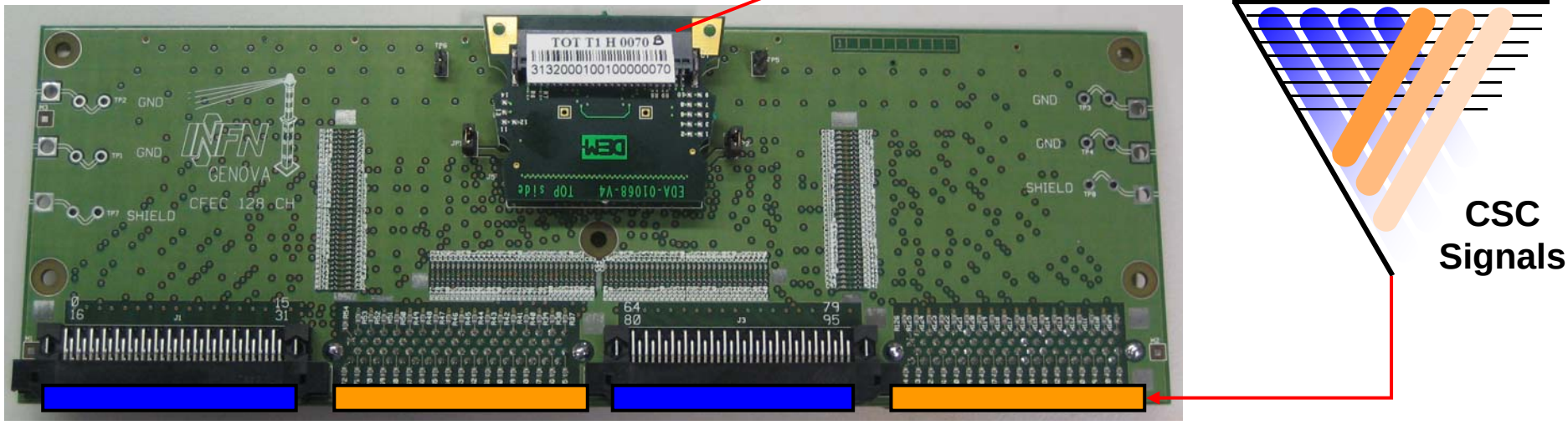
- 10 different types.
  - 5 planes * 2 type (small - large)
- Manages up to 256 channels (2 VFAT).
  - Interleaved anode wires connection
- The primary functionality of the AFEC is to adapt the CSC anode signal to the VFAT preamplifier stage, designed at the beginning for silicon detector
  - Detector Capacitance
  - Preamplifier Shaping time
  - ……
- Compatibility studies have been done using a dedicated circuit housing a prototype die with only 16 VFAT preamplifier channels.

- Impedance measured with TDR method.
- Capacitance measured with 4 wires LCR instrument.
- Anode wires:
  - Z = 330 ÷ 390 Ω
  - cap. 7 ÷ 16.5 pF (others to gnd)
  - Anode wires length 20 ÷ 100 cm

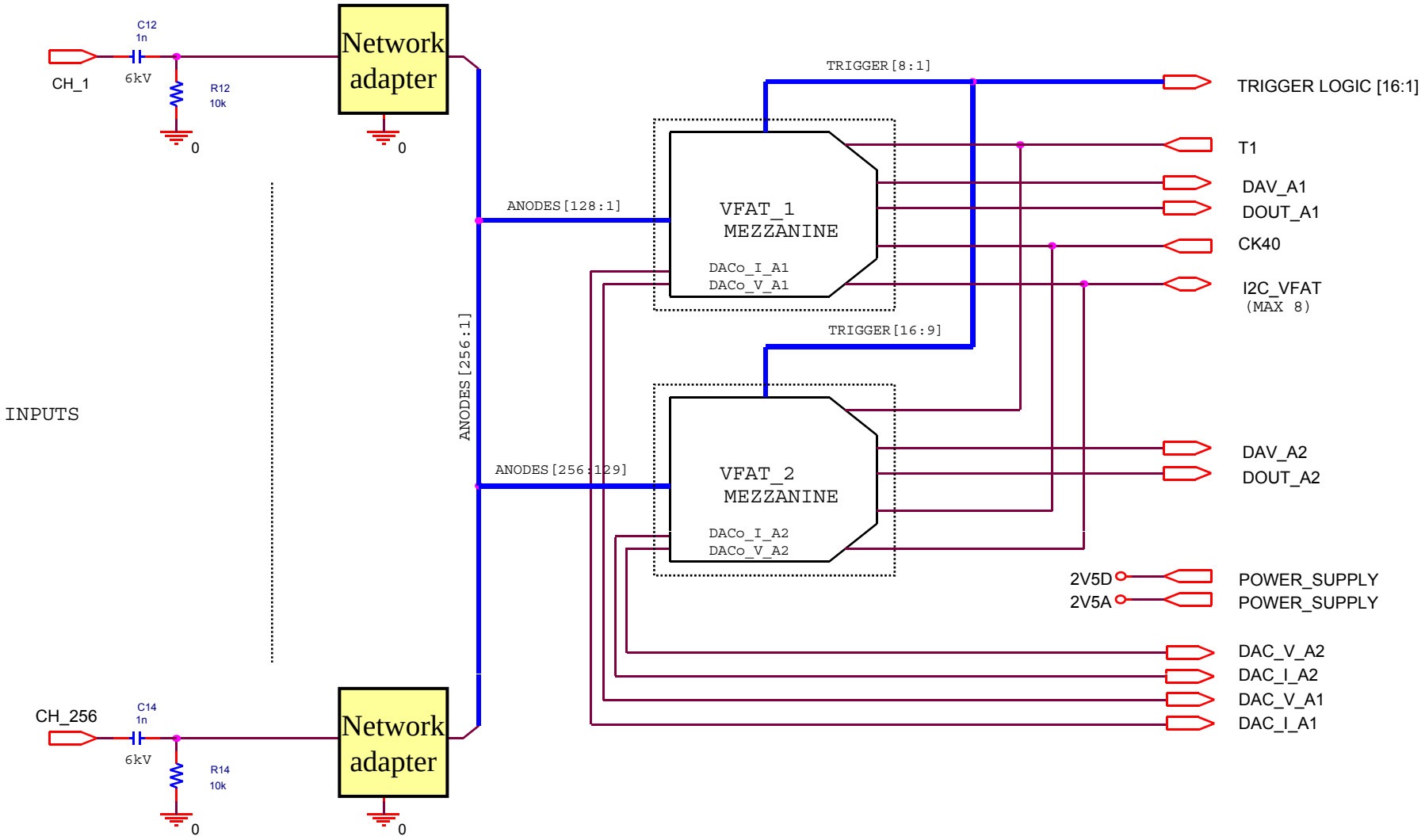


CFEC

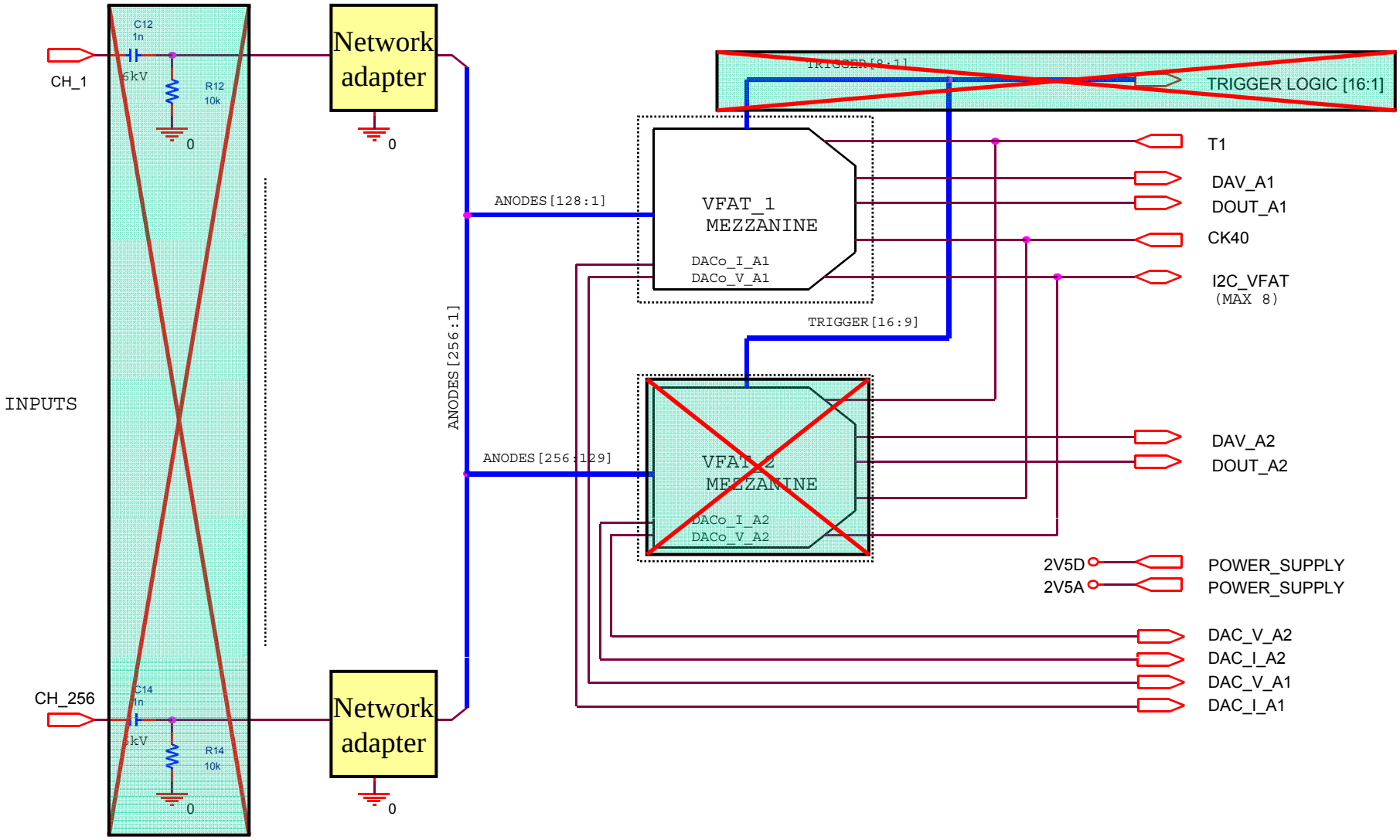
- 1 type only → manages up to 128 chs (1 VFAT)
- Installed 40 for ¼ T1 = 15 CSC chambers.
- As the AFEC, its main functionality is to adapt the CSC cathode signal to the VFAT preamplifier stage
  - Detector Capacitance
  - Preamplifier Shaping time
  - ¼ signal max compared to the anode charge
- Cathode Strips:
  - Z = 120 ÷ 150 Ω
  - cap. 7 – 88 pF (others to gnd)
  - Cathode Strips length 6 – 80 cm



Anode FE Card block diagram



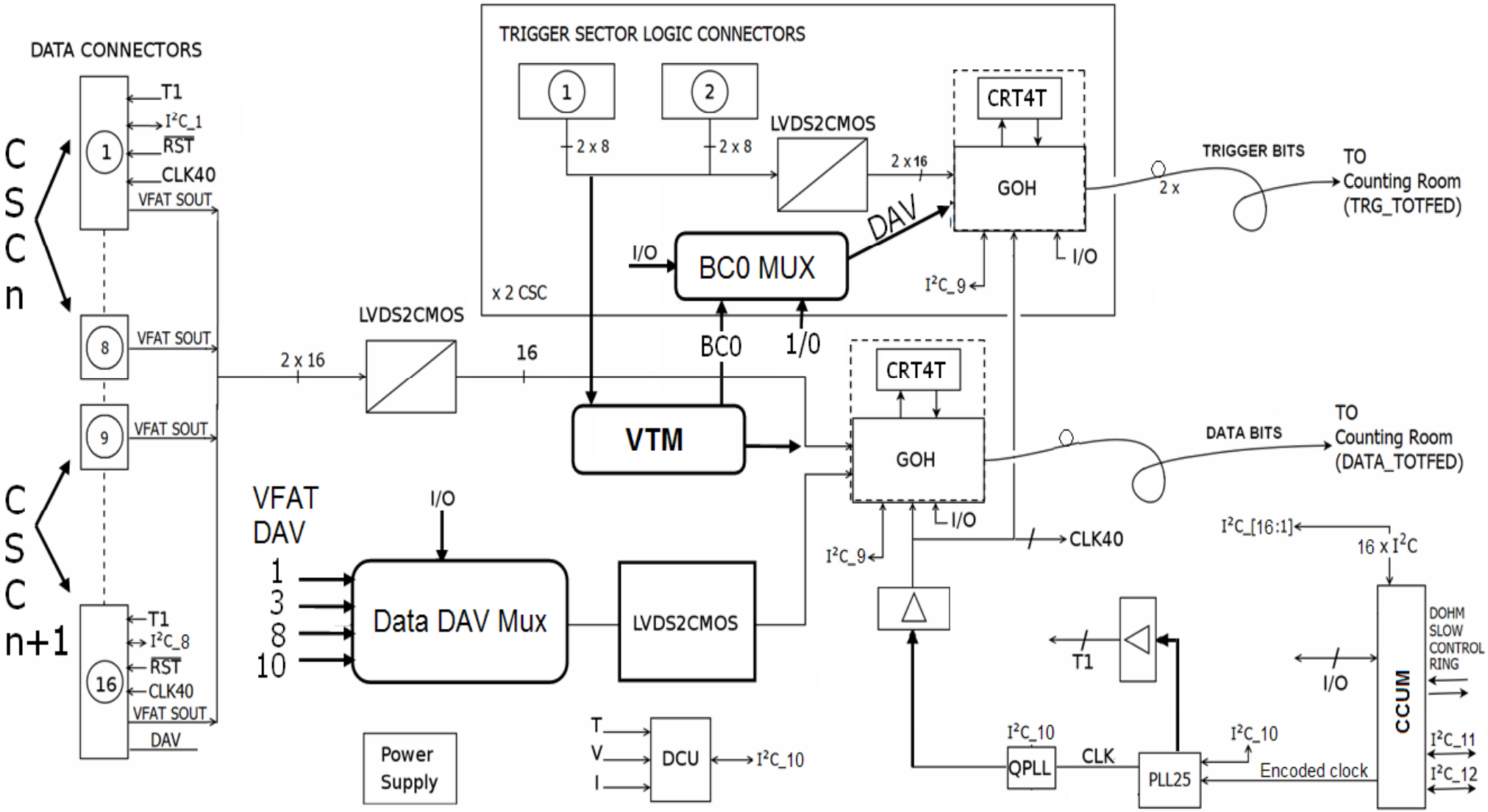
Cathode FE Card block diagram



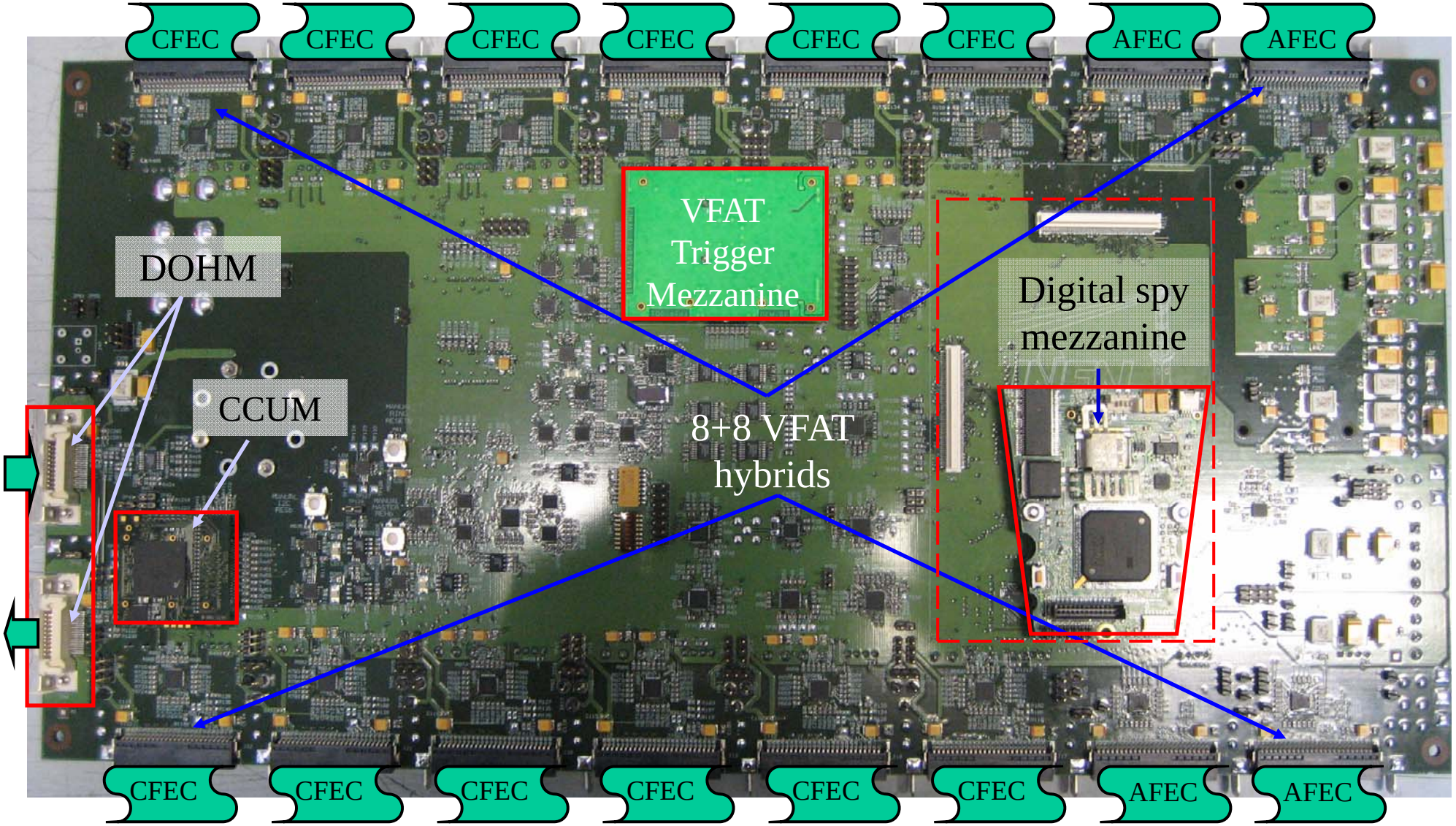
ReadOut Control board

- The ROC board manage two CSCs detectors.
- Collects the serial data streams coming out from the VFAT hybrids and transmit them to the Counting Room, via a Gigabit Optical link Hybrid (1 GOH).
- Trigger bits also sent via optical links (2 GOHs), they are
  - made available within the next clock (25 ns) after the detection of a hit on one of the channels.
  - No coded before optic transmission.
  - Collected also by VTM and optionally transmitted within tracking data. (VFAT Trigger Mezzanine)
- Performs the trigger bits synchronization circuitry (VTM → BC0 fast command).
- Gigabit Optical Link → Ethernet Slow mode (data rate 800Mbit/s) → Line Coding 8B/10B
- Distribute and regenerate the LHC 40Mhz clock and T1 Fast Commands to all the FE boards.
  - PLL25 extracts the LHC clock from the Token Ring encoded clock signal and decodes the T1 Fast Commands (LV1, BC0, Resync, Calib) → I^2C programmable clock phase shift.
  - Quartz crystal based Phase-Locked Loop (QPLL) locks to the LHC master clock signal (40.078686 MHz) and provides a low-jitter copy of it → autoRestart locking operation mode.
- Handles the Communication Control Unit (CMS-CCUM) node for Embedded Slow Control
  - distributes the I^2C control lines to the FE electronic cards.
  - Parallel I/O port manages GOH power cycle, DAV and BC0 selection, Hard and Soft reset….
  - Redundant Skip Fault Architecture
- Hosts custom spy mezzanine, in order to emulate the CCUM functions and acquire data and trigger bits coming out from the FE cards.

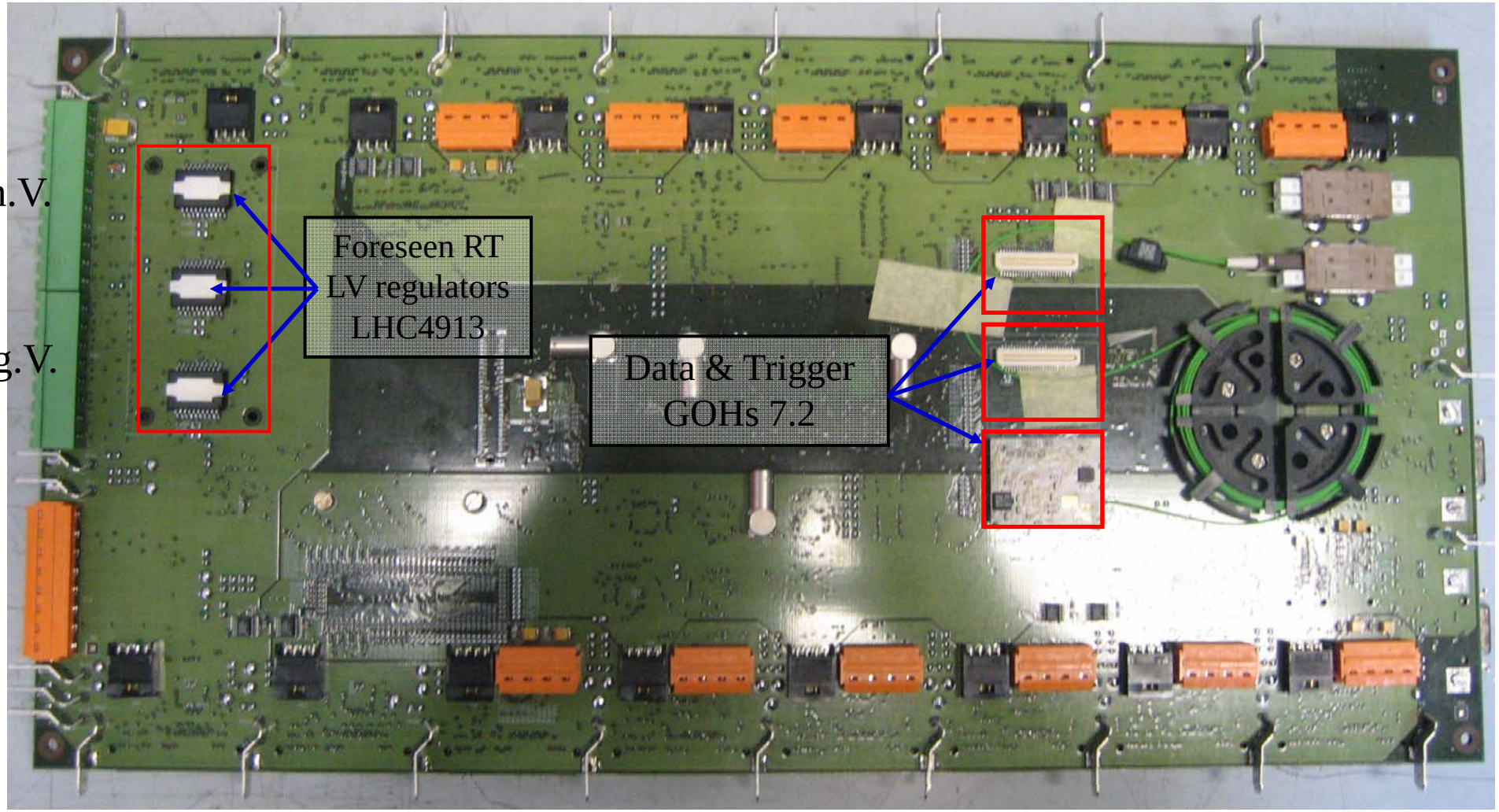
ReadOut Control board diagram



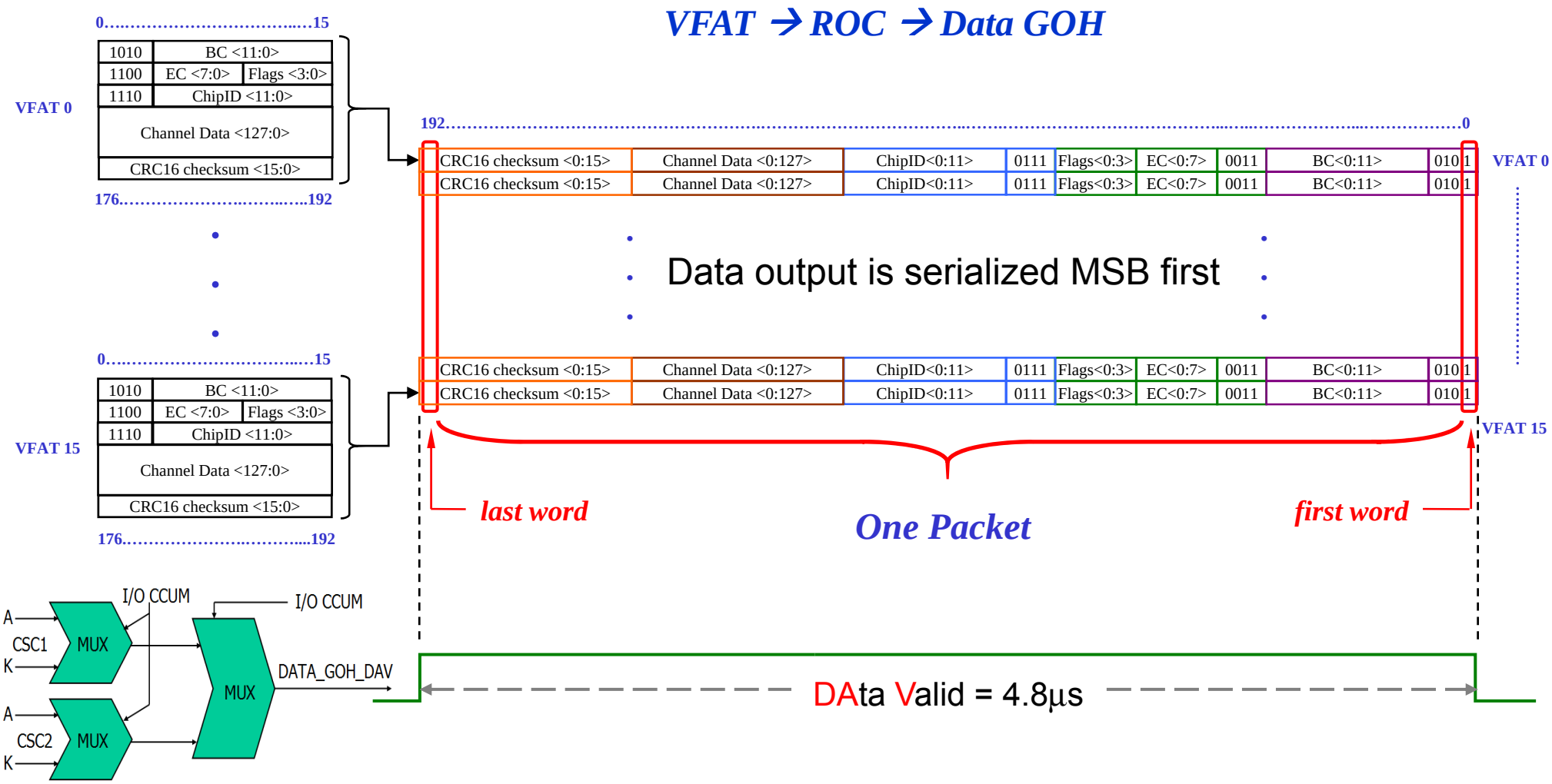
ROC top


CFEC
CFEC
CFEC
CFEC
CFEC
CFEC
AFEC
AFEC
VFAT
Trigger
Mezzanine
DOHM
CCUM
8+8 VFAT
hybrids
Digital spy
mezzanine
CFEC
CFEC
CFEC
CFEC
CFEC
CFEC
AFEC
AFEC

ROC bottom

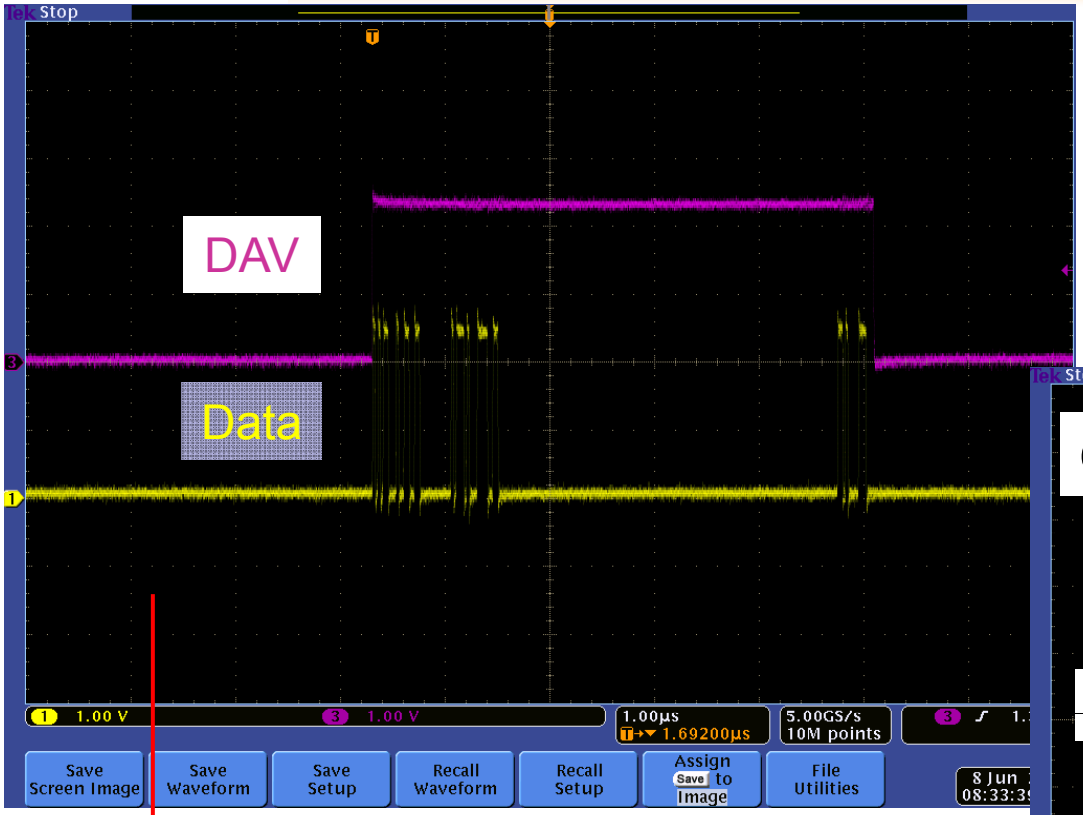

An.V.
Dig.V.
Foreseen RT
LV regulators
LHC4913
Data & Trigger
GOHs 7.2

VFAT data packet format

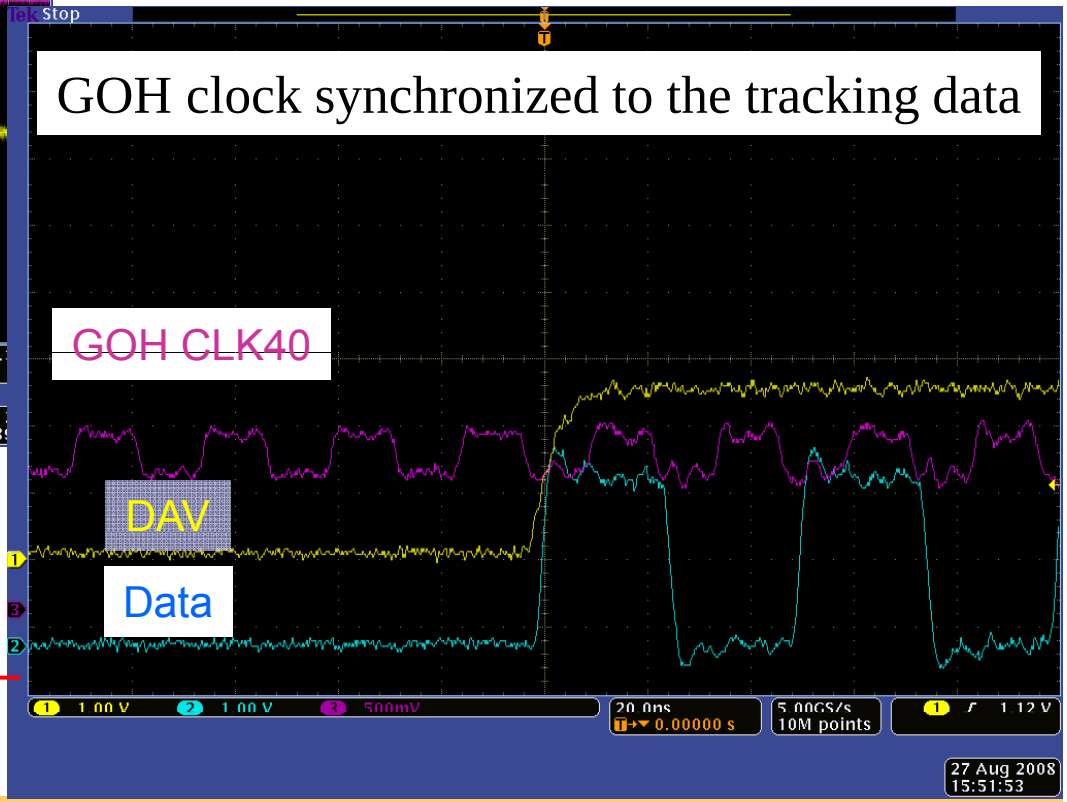


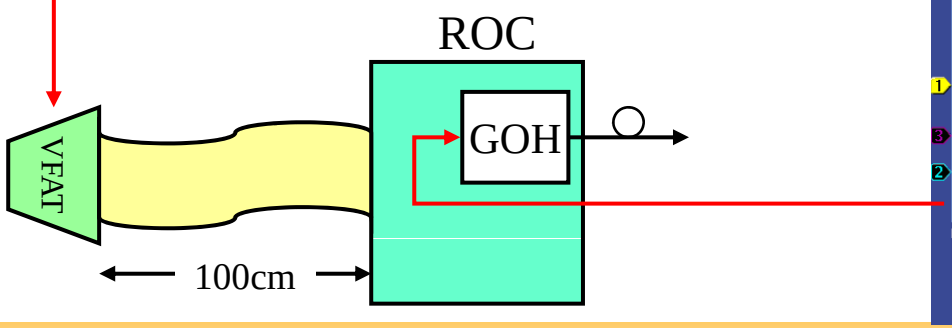
VFAT 192 serial bits → 16VFATs per GOH → 12GOHs per OptoRX and S-Link modules → 192x16x12=36864 bits → ~4kB packet

Data packet transmission



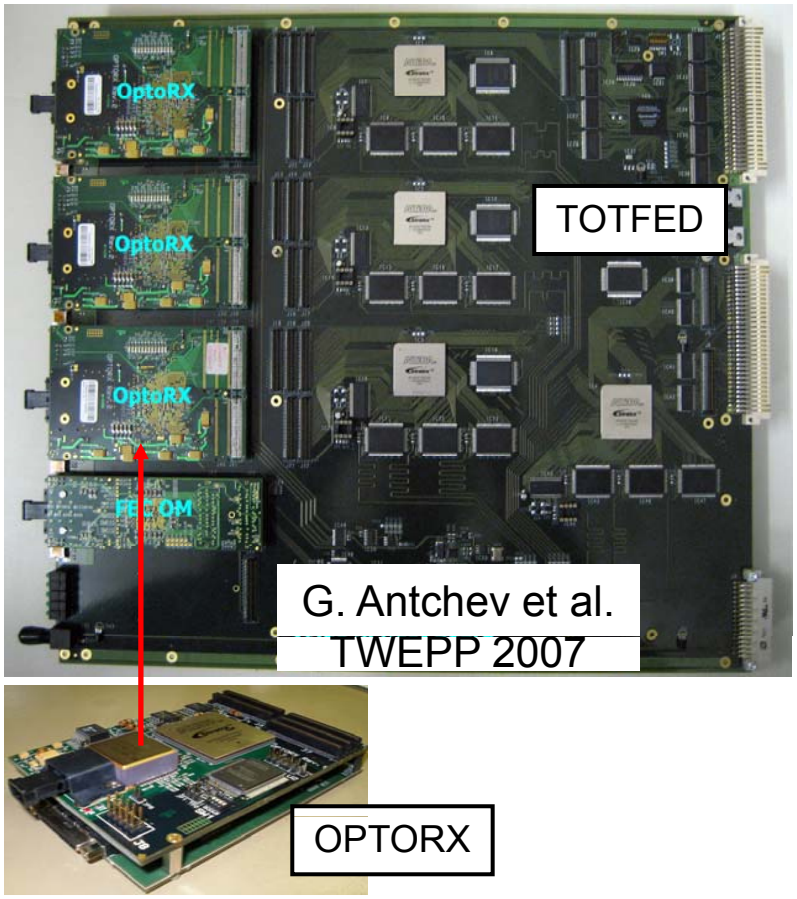
← VFAT Tracking data





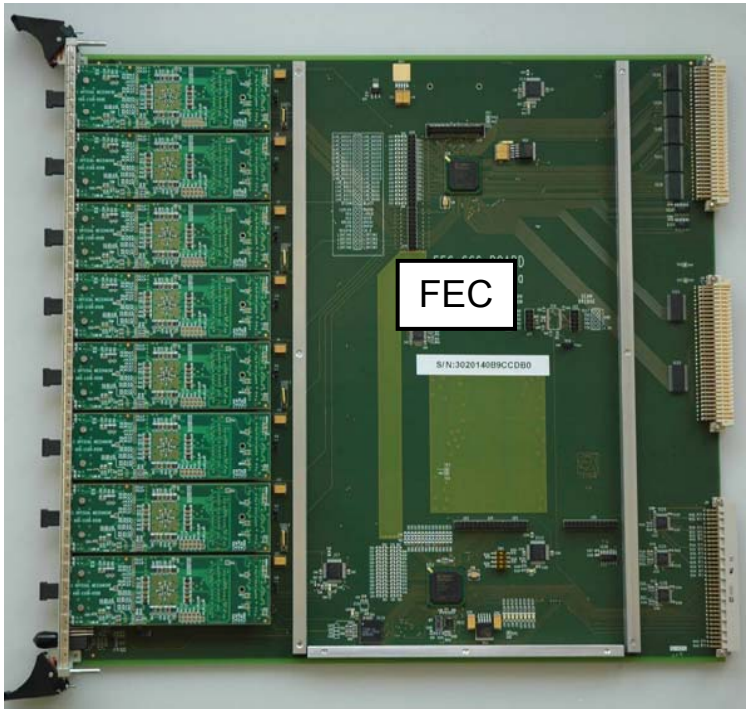
Counting room electronics

- Integrated deserializers to receive optically transmitted data from detector
- Slink64, VME, for USB possible
- Large effort on firmware

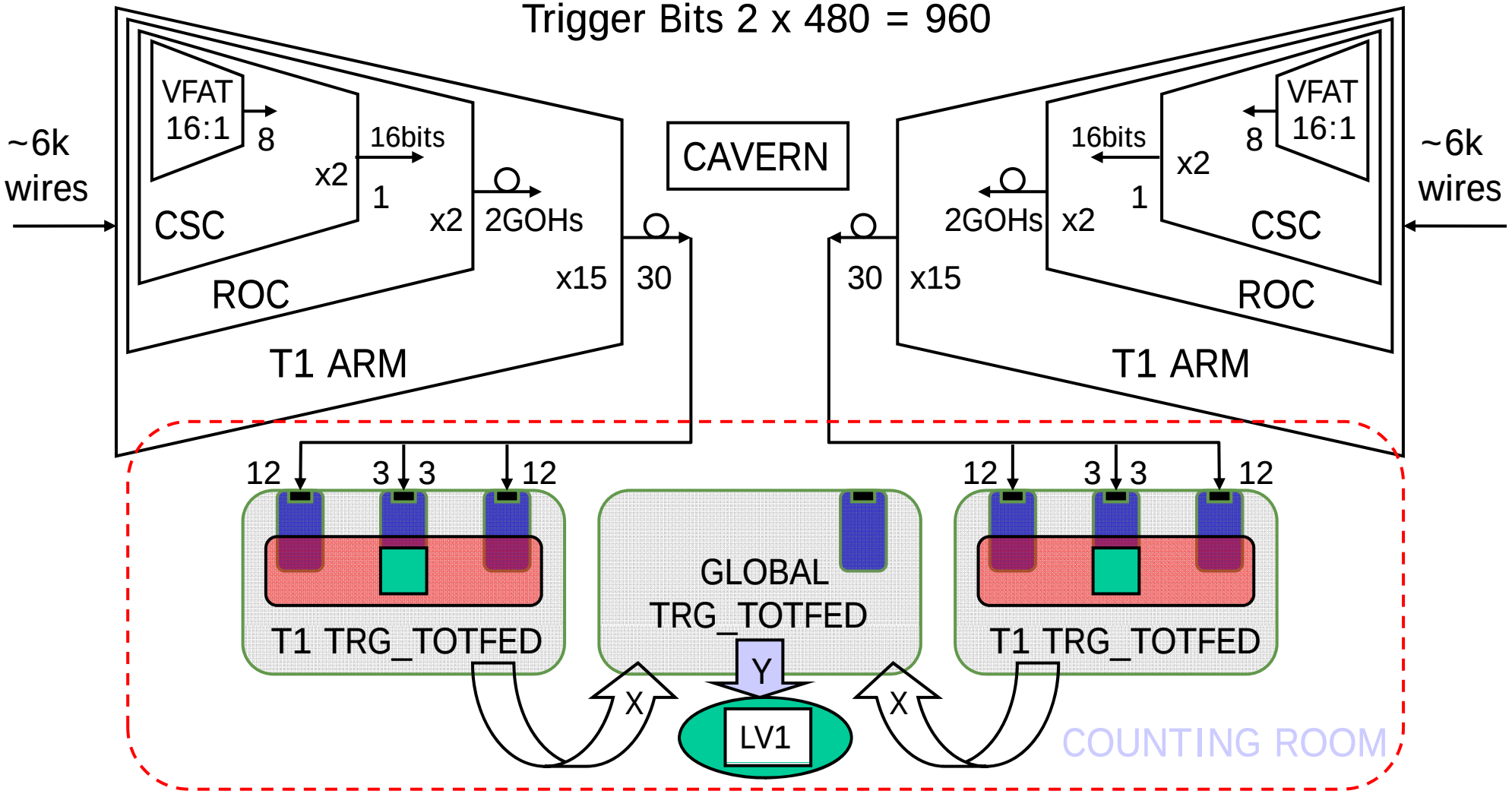


FEC-CCS card; K. Kloukinas et al.

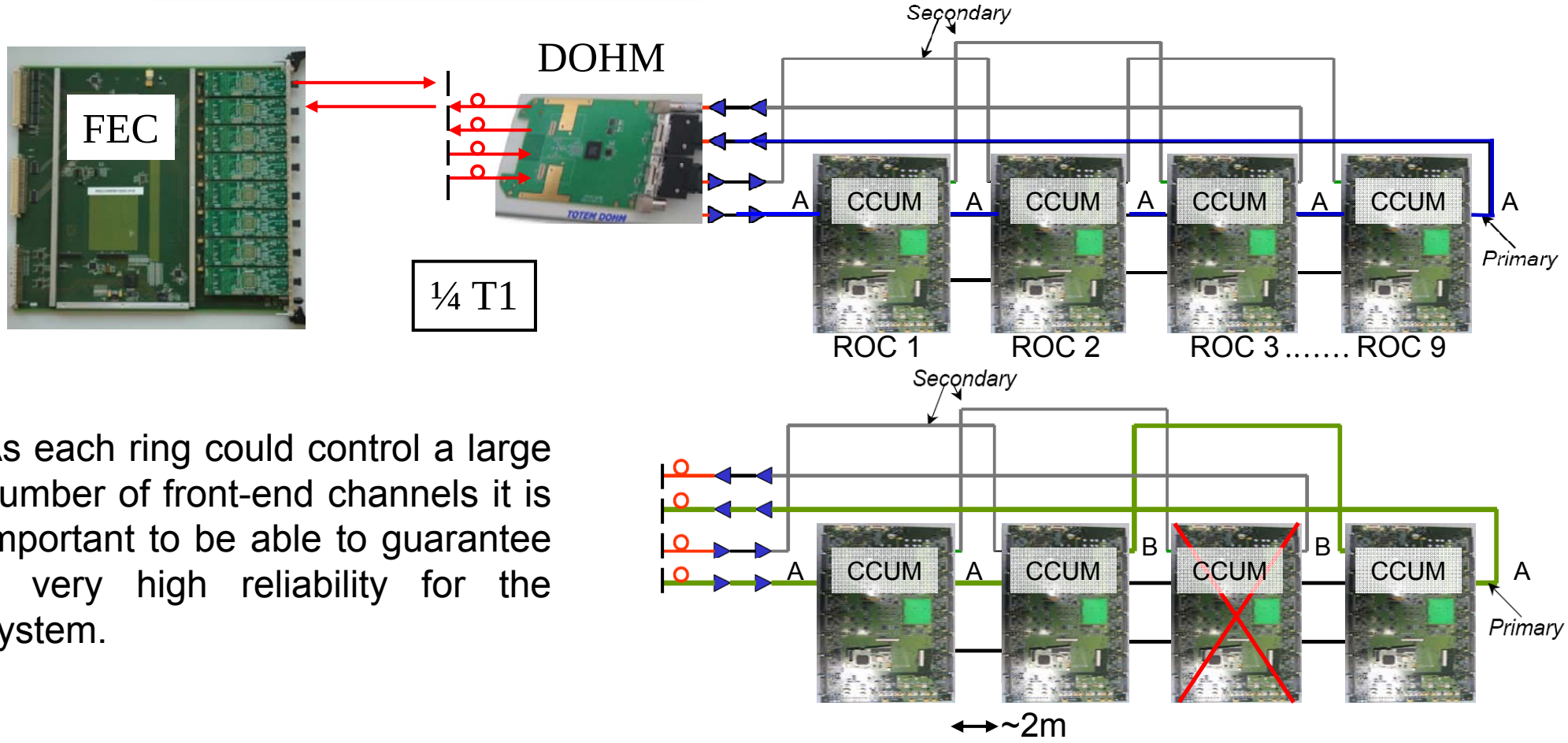
- sends and receives control data for the on-detector electronics
- sends timing and trigger information
- Can drive up to 8 control loops through 8 mezzanine FECs or mFECs



T1 trigger architecture



Redundant skip fault architecture

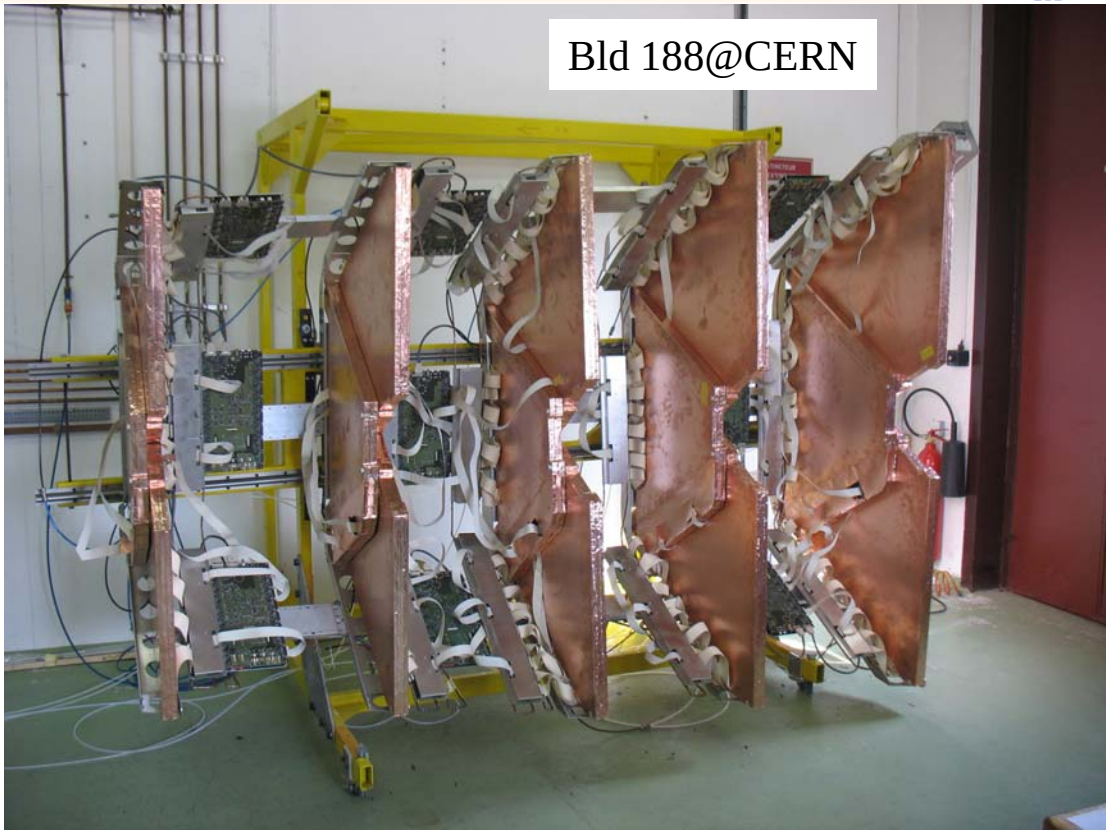


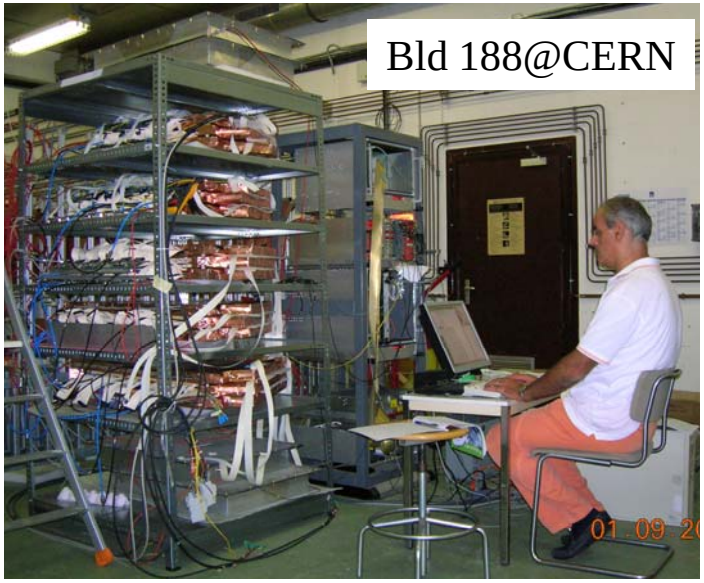
As each ring could control a large number of front-end channels it is important to be able to guarantee a very high reliability for the system.

The redundancy scheme, based on CMS devices and architecture, consists of two independent data paths, one connecting the CCU modules serially and a second redundant path which alternatively skips one CCU module in the chain.

Conclusions

- ✓ All ¼ T1 boards + spares have been produced and separately tested.
  - ➢ fully assembled ¼ T1 detector tests on going.
- ➢ Ready to start for full production.



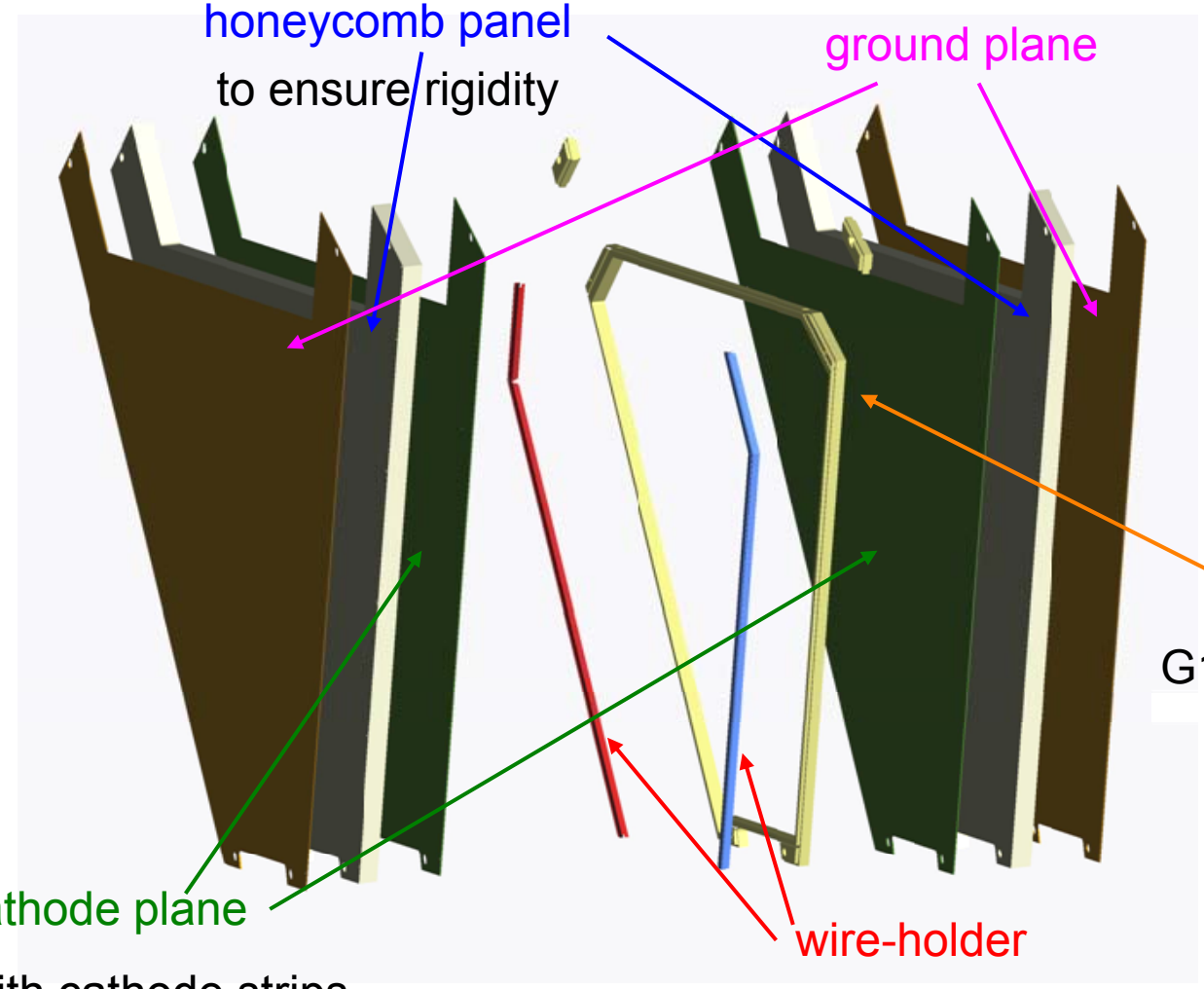


- ✓ CSC chambers available, flushed and HV tested.
- ✓ Mechanics elements ready.
- ➢ Large efforts still needed from the firmware and DAQ Software point of view.

Thank you.

Extra slides

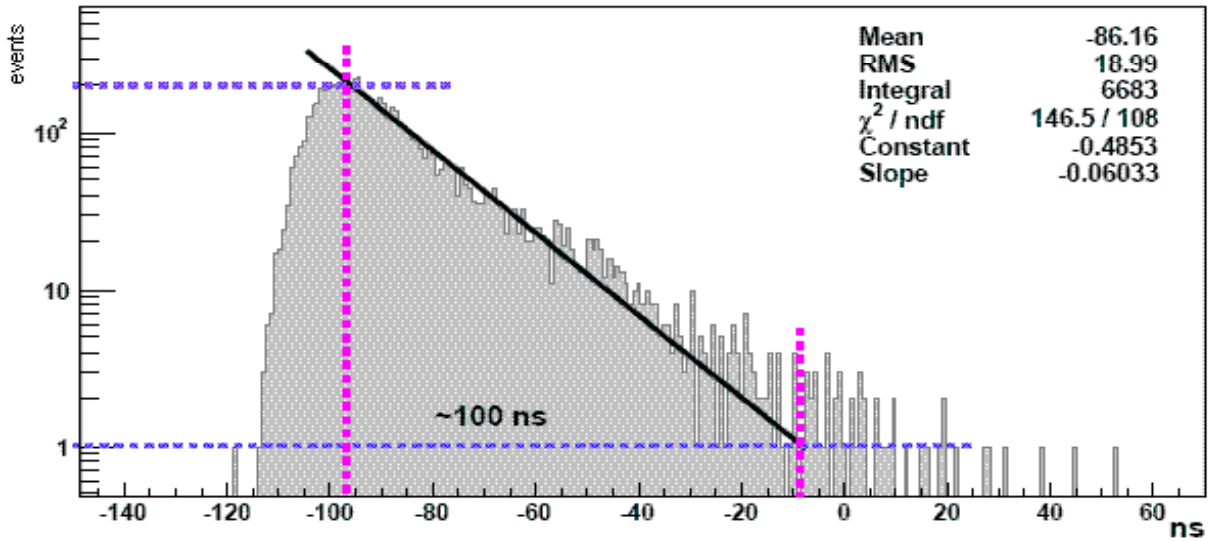
Material for chamber construction



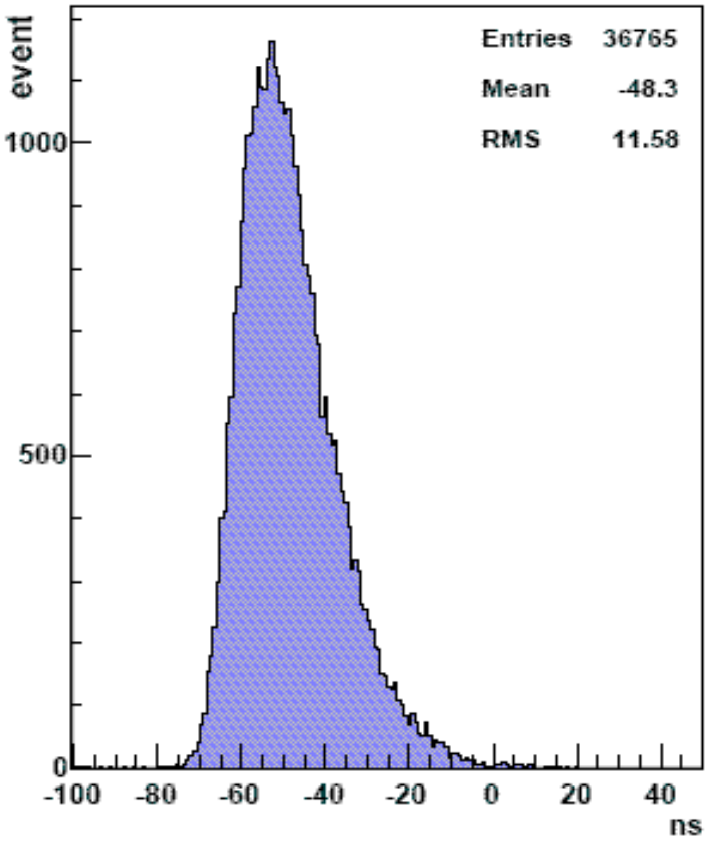
Time resolution

- Measurements done with TDC in test beam
- Jitter for single wire ~100 ns
- Better time determination by use of coincidence logic

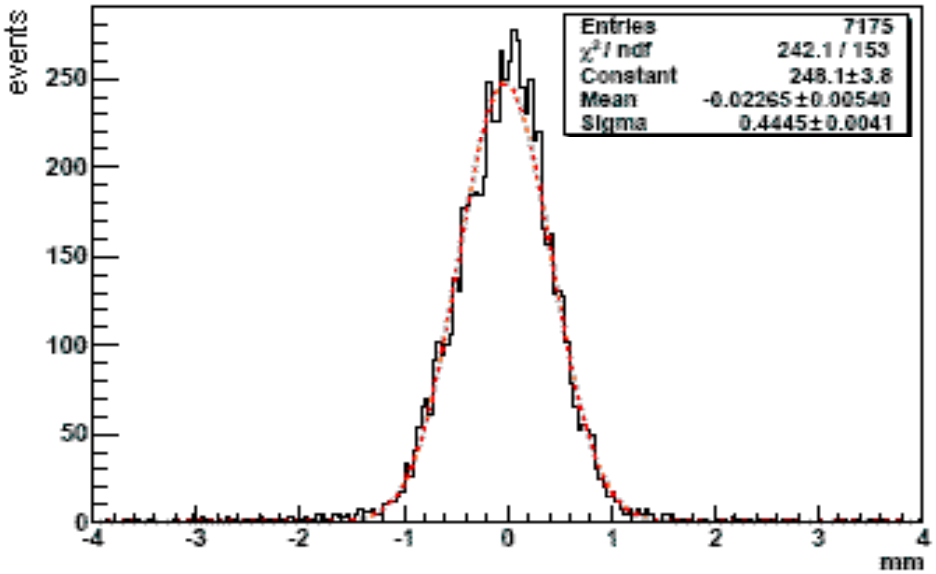
Single wire time distribution



Time distribution for second wire in 3/3 coincidence



Position resolution



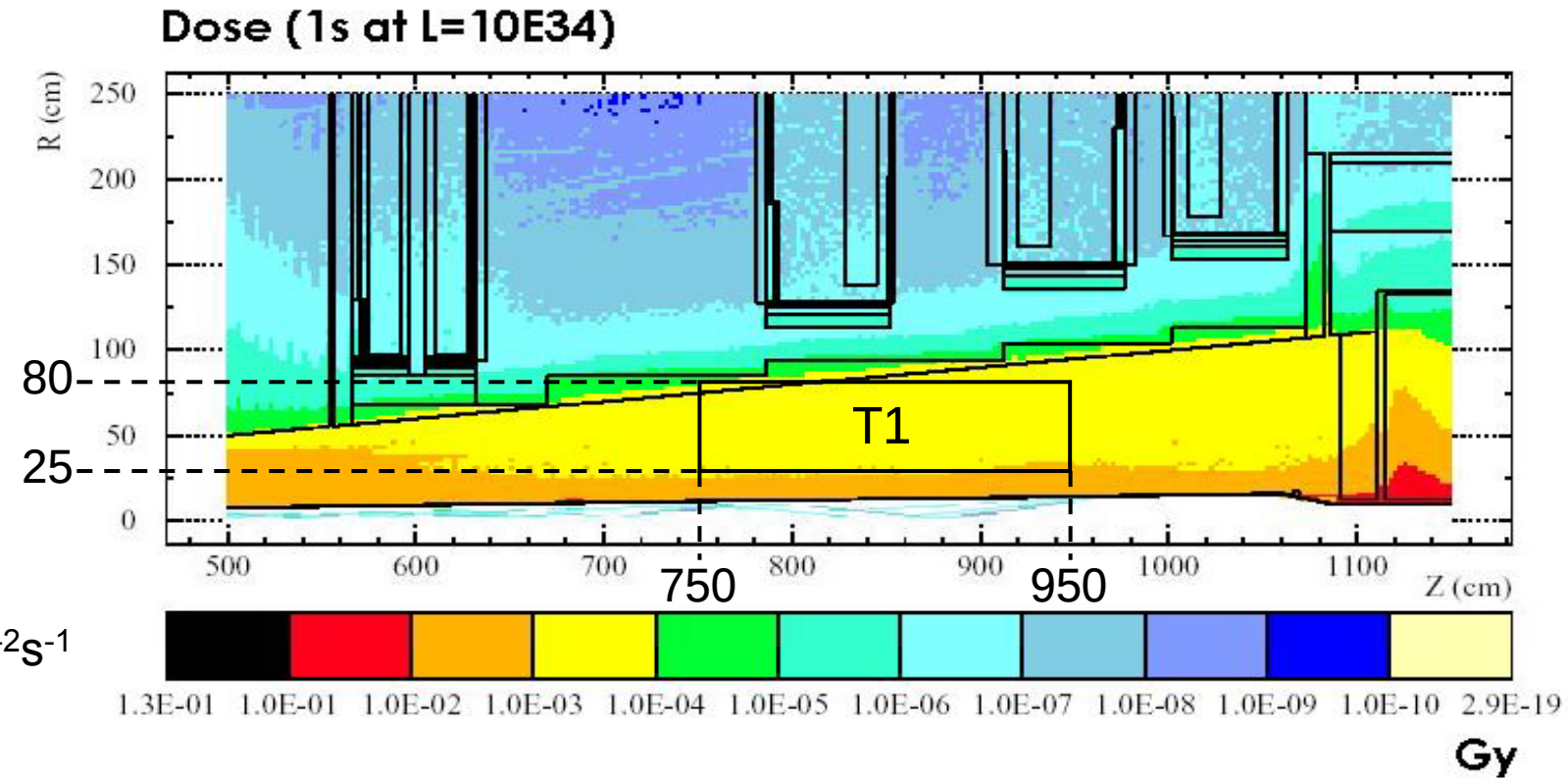
- Best *u*-view resolution obtained in test beam with the “center of mass” method for the strips is ~0.4 mm

- If digital readout with half strip determination is used, expected resolution is (5 mm)/√12 ~ 0.7 mm
- Preliminary results from simulation:
  - half-strip peak finder ⇒ σ_u ~ 0.7 mm;
  - fully digital (whole clusters) ⇒ σ_u ~ 1.5 mm;
  - substantial improvement in hit loss and ghost hit rejection with half-strip method in high multiplicity events

T1 Radiation Environment

Mika's data

- Assuming:
  - 10^7s/year
  - L=10^{32}cm^{-2}s^{-1}



- T1 CSCs are placed between 7.5m and 9.5m
- Anode worst position R = 25 cm → $10^7*10^{-3}*10^2/10^2$ = 10krad/year
- Cathode position R = 63÷80 cm → $10^7*10^{-4}*10^2/10^2$ = 1krad/year

VFAT radiation studies

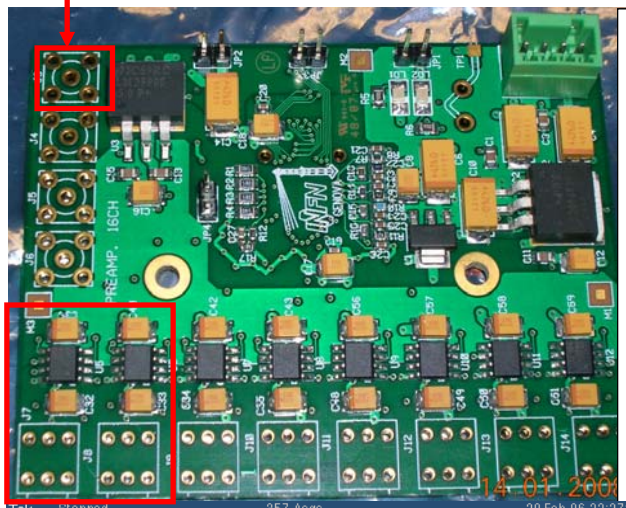
- Preliminary results:
  - X-ray machine on 5th floor of building 14 at CERN.
  - Dose rate 4.2 Mrad / hour
  - VFAT is resistant to Total Ionising Dose up to 150Mrad
  - No functions failing
  - Noise unchanged
  - Slight change in DAC gradient. Perhaps the need for periodic adjustment of DAC setting.

VFAT power consumption			
(mW)	Sleep	Run (nominal)	Run (max)
Analog	33	378	378
Digital	135	194	237
Total	168	572	615

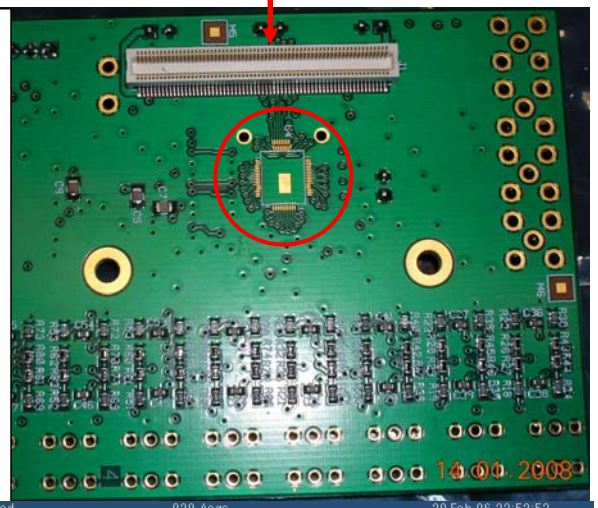
AFEC/CFEC tests

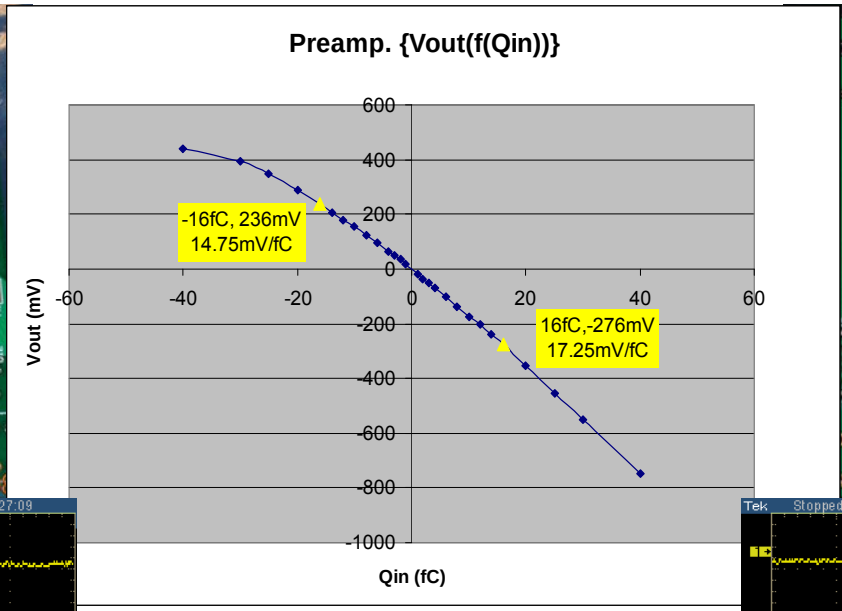
- This small boards use the same FE preamplifier integrated inside the VFAT ASIC (Av=~18mV/fC) (Jan Kaplon).

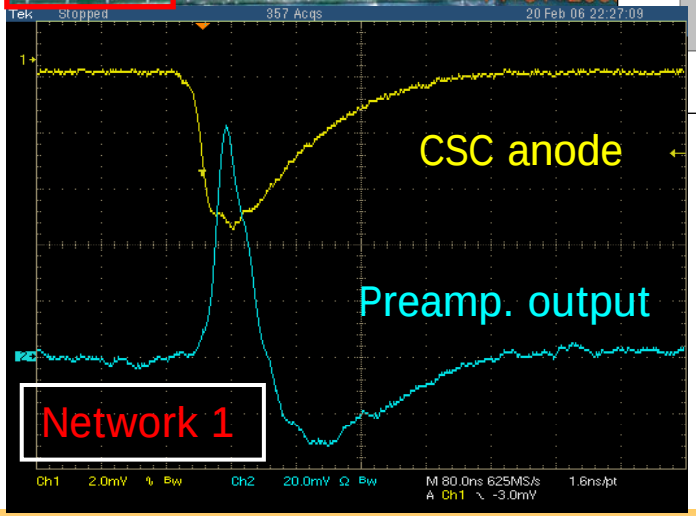
Vcal

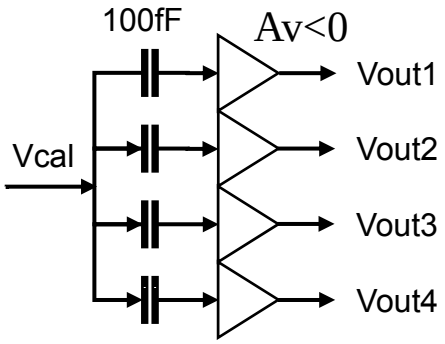


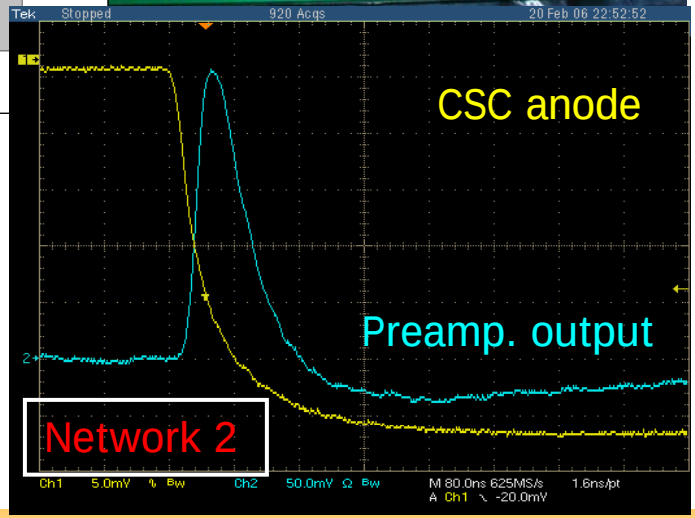
CSC signals





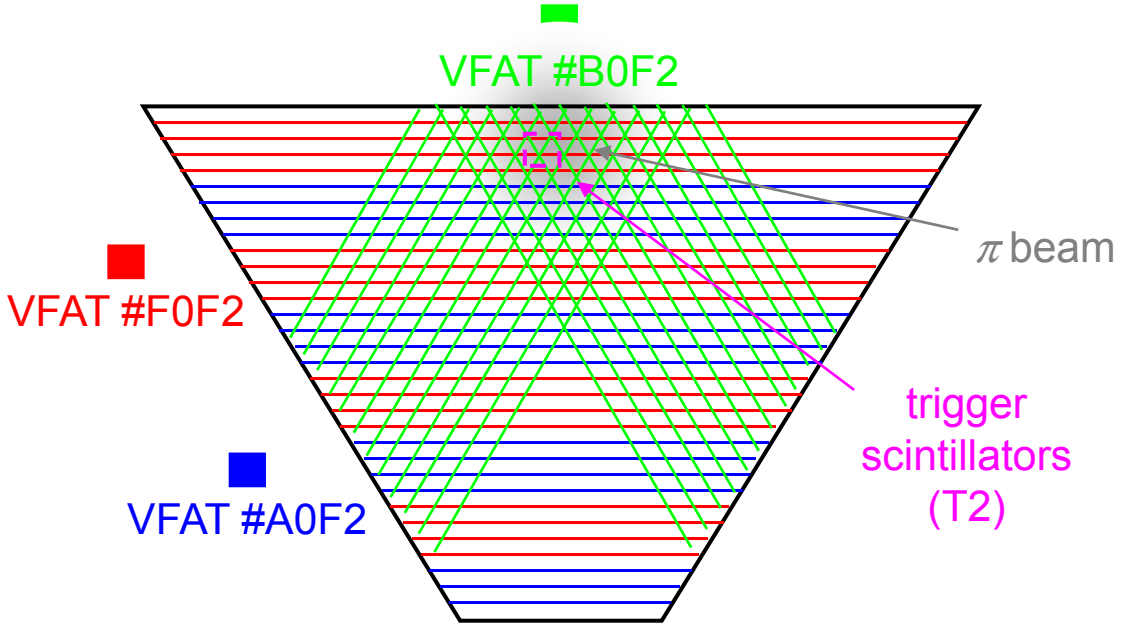




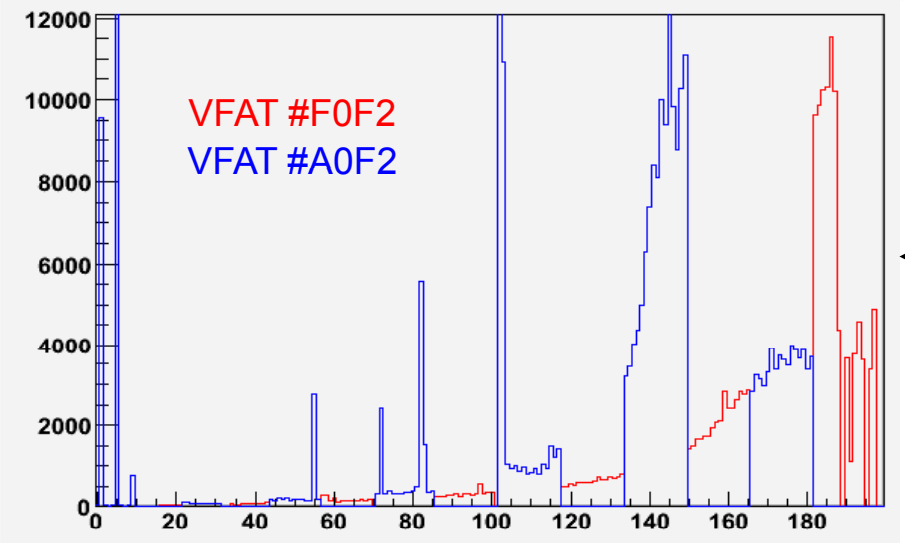


Test beam set-up

- One pre-production chamber (5P-type) installed on the beam
- Gas mixer flux meters not working properly: flushed with approximately Ar(50%)/CO_2(50%) mix
- All anode wires read out by two VFAT on AFEC; approximately 1/3 cathode strips read out on both sides by one VFAT on CFEC128



Channel occupancy



HV ≥ 3.4 kV, thr ≤ –22

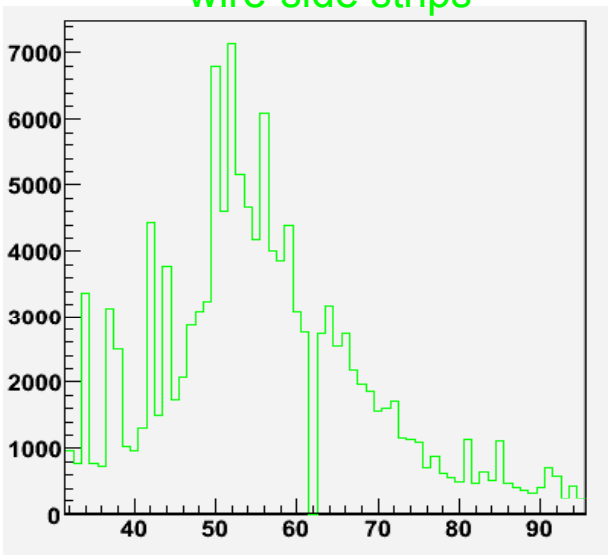
← something's wrong

Wires

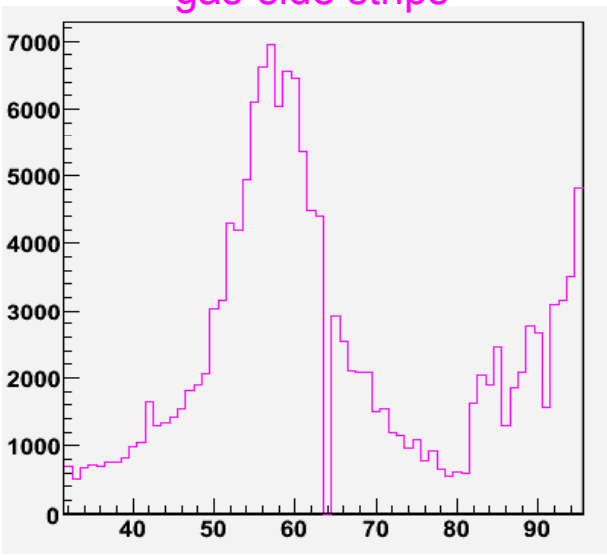
HV ≥ 3.4 kV, thr ≥ 32

shapes look ~OK →

wire-side strips



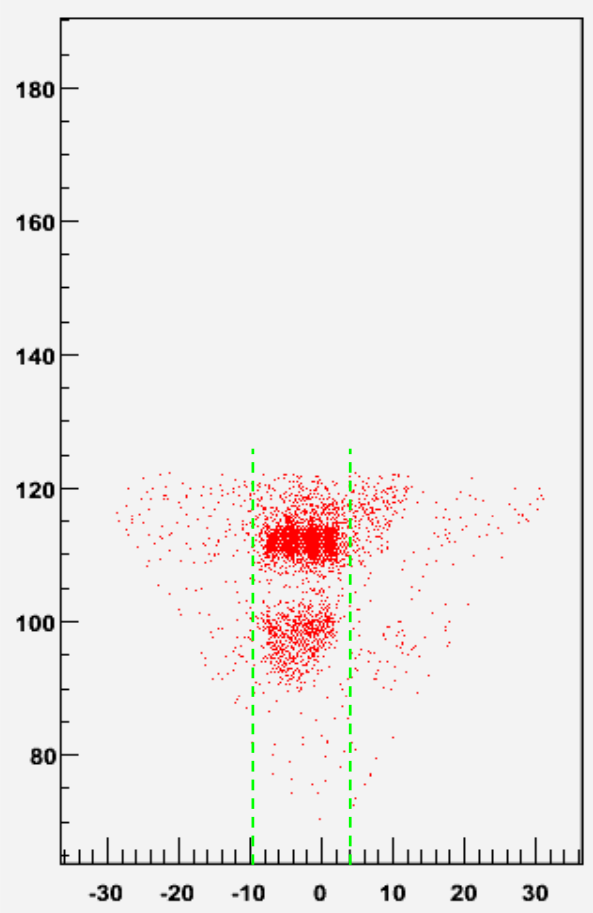
gas-side strips



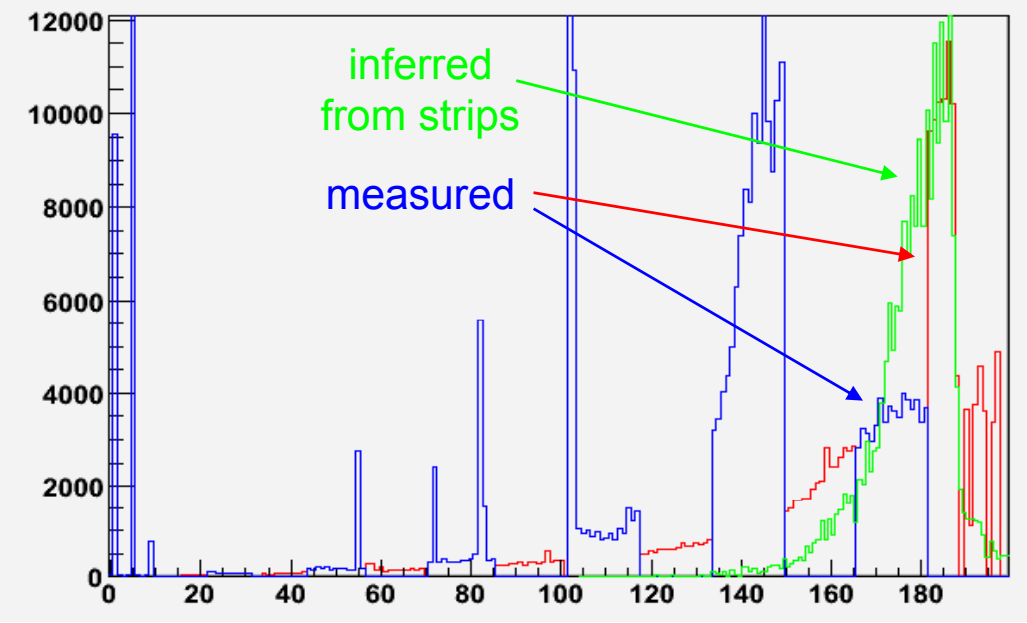
Using strips information

Map of 2D points from strips…

…after requiring wire confirmation



wire occupancy



- About 40% of the beam signal is lost
  ⇒ real efficiency is close to 1