The TOTEM T1 detector electronics system

S. Minutoli [b], F. Ferro [b], M. Lo Vetere [a,b], E. Robutti [b] and P. Musico [b]

[a] Dipartimento di Fisica, Via Dodecaneso, 33 – 16146 – Genova, (*Italy*)
[b] Istituto Nazionale di Fisica Nucleare, Via Dodecaneso, 33 – 16146 – Genova, (*Italy*)

saverio.minutoli@ge.infn.it

Abstract

The T1 detector of the TOTEM experiment is devoted to the measurement of the inelastic rate of proton-proton interactions at LHC. It is made of Cathode Strip Chambers. We describe the complete electronic chain including the front-end, the readout and the trigger. Key features are high radiation tolerance and compliance with the CMS standards.

I. THE T1 TELESCOPE

TOTEM [1] is an LHC experiment in construction at Interaction Point 5 (IP), the same of CMS [2] experiment. It is composed of three sub-detectors, covering the high pseudo-rapidity (η) regions on both sides of the IP named RP, T1, T2. The Roman Pots (RP) are special beampipe insertions equipped with silicon strip detectors mounted in the straight sections of the LHC tunnel at a distance of 142 m and 220 m from the IP. The Cathode Strip Chambers (T1) and the GEM detectors (T2) are gas detectors located inside CMS volume (Figure 1).

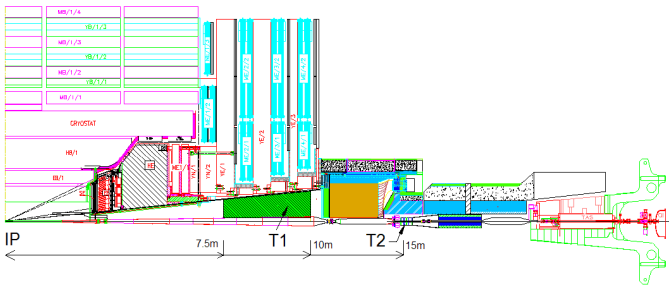

Figure 1: The TOTEM forward trackers T1 and T2 embedded in the CMS detector.

The T1 telescope [4], installed in two cone-shaped regions in the end-caps of CMS, delimited by the beam pipe and the inner envelope of the flux return yoke of the magnet, detects charged particles in the pseudo-rapidity range $3.1 \leq |\eta| \leq 4.7$.

Each telescope arm consists of five planes of CSC equally spaced in z at a distance between 7.5 m and 10.5 m from the interaction point. Each detector plane is composed of six trapezoidal CSC covering roughly a region of 60° in ϕ. Ten types of chambers of different geometry (two for each plane) have been designed in such a way to maximize the sensitive area of the detector.

Each telescope arm is built in two vertically divided halves (half arms) as depicted in Figure 2, in order to allow the installation and removal of T1 when the vacuum chamber is in place.

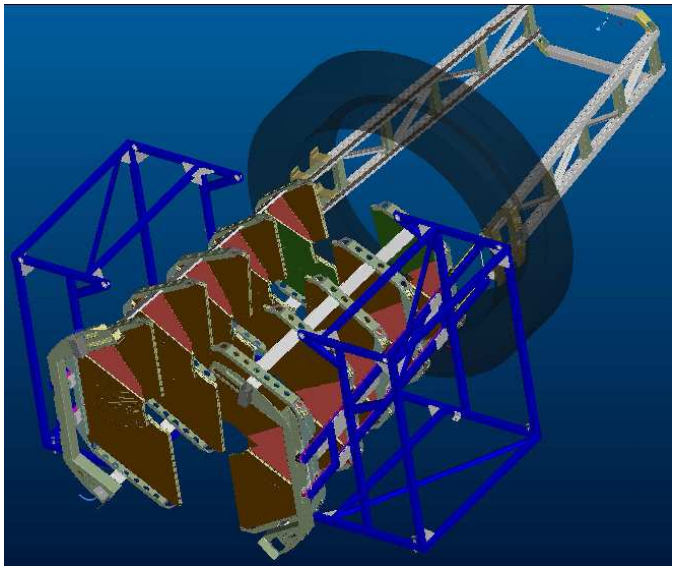

Figure 2 : The two halves of one T1 telescope arm.

In each chamber, gold-plated 30 μm diameter anode wires are strung with a tension of 0.7 N parallel to the base of the trapezoid, with a pitch of 3.0 mm. The wires are supported in place by two printed circuit bars ("wire holder", Figure 3) precisely machined to a thickness of 5.0 mm and glued on one of the two cathode planes inside the gas volume.

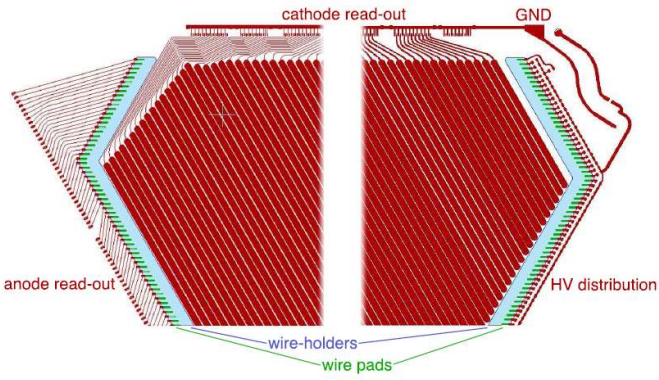

Figure 3: Cathode strips and Anode wire-holder printed circuit boards

In each chamber the cathode electrodes are gold-plated parallel strips oriented at ±60º with respect to the direction of the wires. The pitch is 5.0 mm (4.5 mm strip width, 0.5 mm separation).

The orientation of the cathode strips and of the anode wires provides three measured coordinates of the position of each hit in the CSC plane, useful to reduce the number of fake hits from random combinations ("ghosts") in case of multiple hits.

The T1 detector will be subjected to a large occupancy, particularly in the regions close to the beam pipe due to the characteristic topology of minimum bias events and to the background from particles interacting in the beam pipe.

At a luminosity $L = 10^{28}$ cm^{-2}s^{-1} the expected number of interactions per bunch crossing is 2.5×10^{-3}, which results in an inelastic interaction rate of about 1 kHz. The average number of charged particles per event going through each detector plane is expected to be roughly 40.

II. TOTEM ELECTRONICS OVERVIEW

The electric signals generated by the ionizing particles going through the three detectors are different both in terms of pulse amplitude and in terms of pulse shape. RP generate positive charge signals, T2 negative, and T1 both polarities (anodes and cathodes). Moreover, gas detectors generate more signal charge then silicon crystals and T1 signals are affected by greater jitter than RP or GEM detectors.

In addition, the electronics of the three detectors must comply with different requirements in terms of radiation dose. An overview of the main properties and constraints of the electronics of the three detectors is given in Table I.

Table I: Overview of electronics requirements.

	Roman Pots	T1	T2
No. and type of Detectors	240 Si strip detectors	60 Cathode Strip Chambers	40 Gas Electron Multiplier Detectors
No. of channels	122880	11124 an. 15936 cath	62400 pads 20480 strips
Input charge	~4fC	~50fC	~50fC
Occupancy	<1%	<10% an. <20% cath.	<5% pads <30% strips
Radiation dose	< 10 Mrad	< 50 krad	< 50 Mrad

A common TOTEM front-end ASIC has been designed to perform the charge readout of the three detectors. It has been produced using radiation hard technology that stands radiation doses up to 10 Mrad. This ASIC, called VFAT2 [3] is the key to provide a common data format and a common control and readout scheme. It is fully compatible with TOTEM and with CMS electronic requirements.

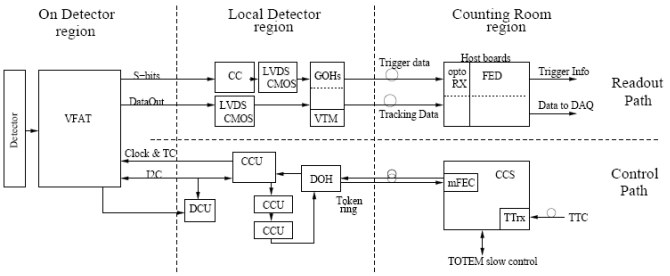

Figure 4: TOTEM electronics system functional block diagram.

Each detector system has a separate read-out system; however a common system architecture is used.

A basic block diagram of the functional components of the system is shown in Figure 4. We may define three logically and physically separated regions. VFAT2 front-end ASICs are located as close as physically possible to the detector (the "On Detector Regions"). Custom read-out boards are placed in the neighborhood of the detector (the "Local Detector Region"): they distribute control signals to the VFAT2, collect and concentrate data from the front-end ASICs, transmit the data to read-out boards in the counting room (the "Counting Room Region").

III. THE T1 ELECTRONICS SYSTEM

An overview of the T1 electronics system [5] is shown in Figure 5.

The CSC anode and cathode signals are collected by custom designed anode front-end cards (AFEC) and cathode front-end cards (CFEC), equipped with VFAT2.

The serial digital data stream and the trigger bits coming from the AFEC and CFEC are collected by a custom designed read-out card (ROC), where they are serialized and optically transmitted to the DAQ system by means of a dedicated CMS Gigabit Optical Hybrid (GOH).

The configuration and monitoring of the system is performed using the I^{2}C standard protocol [6] distributed through the optical CMS Slow Control Ring (SCR), based on the Digital Opto-Hybrid Mezzanine (DOHM) and the Communication and Control Unit Mezzanine (CCUM).

The DAQ system is based on a custom board named TOTFED [11] that can process both data and trigger signals.

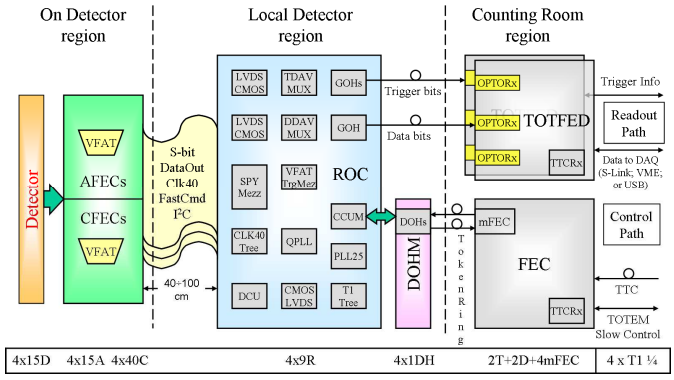

Figure 5: T1 electronics system block diagram.

The low voltage power supplies for the front-end electronics are located a few meters from the detector. The front-end electronic is electrically isolated from the counting room, making use of floating power supplies and optical signal transmission.

The high voltage power supplies are located in the counting room 100m away.

The T1 front-end system globally involves 60 AFEC, 156 CFEC, 36 ROC, 96 GOH, 4 DOHM, 36 CCUM. A sketch of the system is shown in Figure 6.

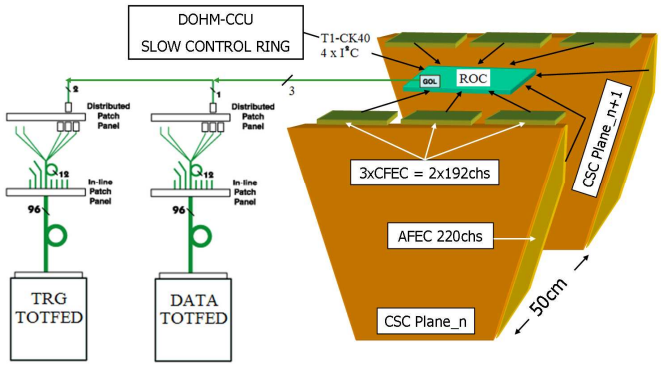

Figure 6: Overview of the T1 electronics system implementation.

In the following the data and trigger electronic systems will be described in more detail starting from the detector hybrids moving up to the counting room.

A. *VFAT2 and the hybrid circuit*

The VFAT2 is a trigger and tracking front-end ASIC [3] with 128 analog input channels, designed in quarter-micron CMOS technology. It measures 9.43 mm by 7.58 mm. The input stage includes internal overload protection circuits that help to avoid destructive breakdown of the chip in the case of sparks (uncontrolled discharges) from the detector.

The chip has two main functions: the first (tracking) is to provide precise spatial hit information for a given triggered event; the second (trigger) is to provide programmable "fast OR" information based on the region of the hit, which can be used for the creation of a level-1 trigger.

All data (1 bit per channel per event) corresponding to a triggered event is transmitted without zero suppression, since the occupancies vary widely and are large for some detectors (see Table I).

VFAT2 has many programmable functions controlled through an I^2C interface. The fast synchronous commands are applied via an encoded LVDS signal (T1) which is then decoded to 4 synchronous commands by an internal command decoder.

A hybrid circuit that hosts one naked VFAT2 has been developed for the TOTEM gas detectors (Figure 7). This hybrid is mounted on the detector as a mezzanine card. A compact 130-pin NAIS PANASONIC connector carries the input signals. A cable connector serves as interface to the outside world.

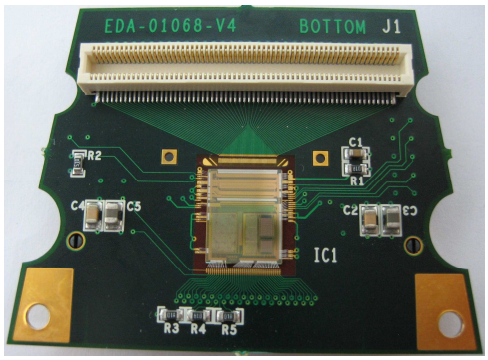

Figure 7: VFAT hybrid.

This mezzanine card also allows digital signals to be fed into the VFAT2 chip digital inputs, thus offering the possibility to process signals coming from an external front-end device.

B. *Anode Front-End Card*

The AFEC (Figure 8) [7] is the board that collects and groups signals from the anode wires of the CSC detector. Ten different types of AFECs have been adapted to the chamber shapes, for a total of 60 boards for the whole detector.

Figure 8: AFEC layout type 2P – 60 cm length.

The AFECs are soldered directly on the edges of the chambers: their length varies between 60 cm and 100 cm. For every channel a double-stage high-pass filter isolates the high voltage on the wire from the readout, breaking the DC ground loop and adapting impedance, capacitance and signal shape (Figure 9).

The readout of up to 256 wires per chamber is carried out by two VFAT2 mounted on a VFAT hybrid each. Trigger information is generated on the VFAT2 by grouping signals from up to 16 contiguous anode wires.

Two high-density halogen-free 50-wires cables connect the AFEC to the ROC.

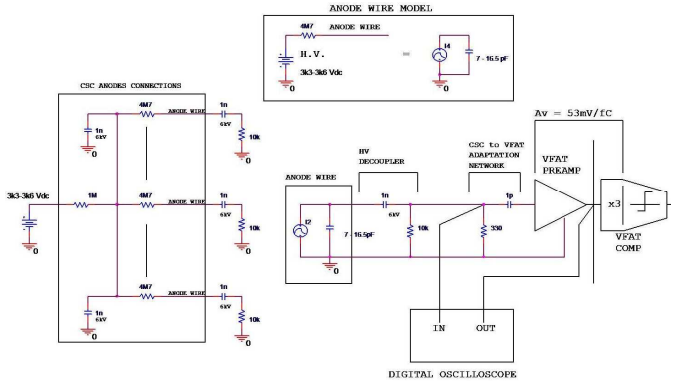

Figure 9: Anode wire model scheme.

C. Cathode Front-End Card

The CFEC (Figure 10) [8] is the board that collects and groups the charge pulses induced in the CSC strips by the positive ions created by the crossing particle and moving towards the cathode. Each board processes 128 input signals.

The CFEC hosts for every channel a high-pass filter and delivers the outputs to a VFAT hybrid. The CFEC input signals are connected to the detector through four compact Hirose 68-pin connectors.

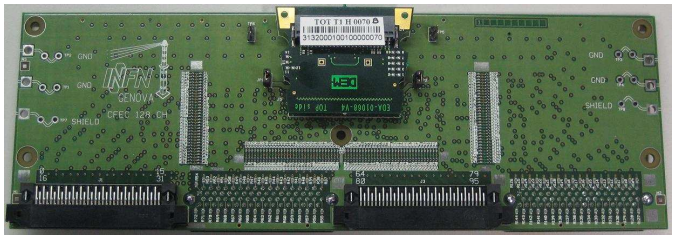

Figure 10: Cathode Front-End Card top view

Due to the different sizes of the detectors, for each layer of the telescope a different number of CFEC boards is needed.

The connection of each CFEC to the DAQ system is done by a fine-pitch halogen-free 50-wires cable.

D. Read Out Card

The ROC board (Figure 11) [9] interfaces the AFEC and CFEC cards to the DAQ system, located in the counting room (Figure 5). It represents the data, trigger, slow control and low voltage junction point of two CSC detectors (Figure 6). The board receives data from 16 VFAT hybrids hosted on the AFEC and CFEC cards, for a total of 2048 CSC signals.

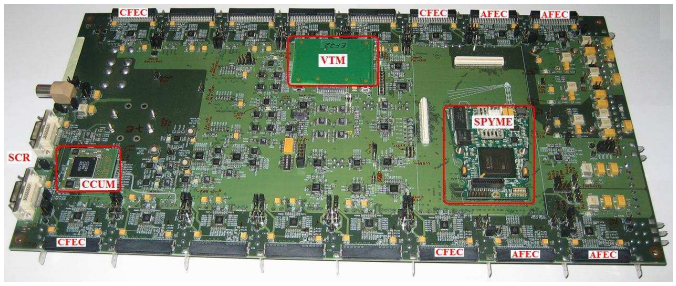

Figure 11: ROC top view.

The serial tracking data stream received from the front-end hybrid is converted from LVDS to CMOS levels and optically transmitted, through the GOH mezzanine [10], to the TOTFED board [11] in the counting room.

The GOH groups the 16 data inputs in two 8-bit words treated in parallel and transmitted over a fiber through a 0.8 Gbit/s Ethernet 8B/10B parallel-to-serial encoder.

Each chamber has up to 8 allocated front-end connections, two for the anodes and six for the cathodes. Only the AFECs produce trigger information. For each CSC 16 trigger bits are generated and transmitted to the TOTEM T1 trigger system via a dedicated GOH optical link. The trigger information can also be merged with the readout data stream using a spare Gigabit Optical Link data channel and a special VFAT Trigger Mezzanine (VTM) hybrid (Figure 11). This mezzanine card also decodes the fast command signal and extracts the Bunch Crossing Zero (BC0) command in order to insert it in the trigger building signal stream for synchronization purposes.

The Slow Control Ring (SCR, Figure 12) adopted for all three TOTEM detectors, is based on the CMS tracker and electromagnetic calorimeter token ring system [12]. The ROC manages the Trigger Timing and Control (TTC) [13] signals by means of the DOHM module [14] and communicates with the on-detector chips through the addressable CCUM mezzanine card plugged on it (Figure 11). The SCR can manage up to 127 CCUM nodes and also implement skip fault architecture for additional redundancy based on the doubling of signal paths and bypassing of interconnection lines between CCUM.

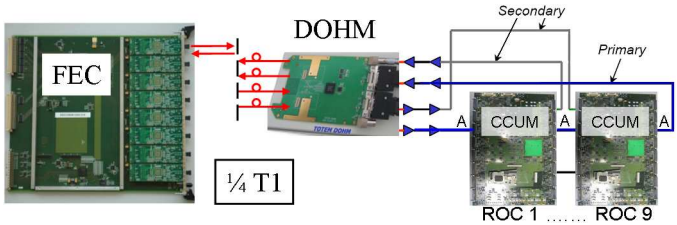

Figure 12: Slow Control Ring redundancy.

Each CCUM controls the reset signal, three 8-bit general-purpose I/O ports and up to 16 I^2C serial line connections. The 40 MHz LHC master clock and the fast commands from the LV1 signal are also extracted in the ROC from the token ring. The regeneration of the clock is performed by the PLL25 [15] component while further clock jitter reduction necessary for optical signal transmission is implemented using a QPLL device [16]. The distribution of the clock and the LHC fast commands to the front-end boards is implemented adopting a tree structure in order to minimize the skew and the delay time between different front-end receiver circuits.

In order to avoid missing data in case of failure of the master VFAT that enables the GOH serial data transmission, redundancy logic has been foreseen in the design of the ROC. The swapping of the master VFAT can be done via the general purpose I/O bits available through the SCR. As for the data, the trigger bit transmission is modifiable changing the functionality of the logic with the SCR I/O connections.

A spy test port is foreseen on the ROC board: all the front-end connections are routed to dedicated connectors in order to plug a piggy-back mezzanine (SPYME, Figure 13) [17] where a Xilinx FPGA type XC3S1500FG456 provided of USB 2.0 serial port [18] can emulate the DAQ system chain.

Figure 13: SPYME mezzanine.

The ROC also provides connectivity for monitoring signals (PT100, radiation monitor, humidity and pressure sensors).

E. Counting Room Hardware

The counting room hardware has been fully standardized across detectors and the same hardware is used for data readout and trigger signal generation.

The TOTFED board (Figure 14) [11], equipped with optoreceiver (optoRX) mezzanines, receives both trigger and tracking data. It is the result of a shared development: the CMS pre-shower group has designed the opto-receiver mezzanine; TOTEM the TOTFED board. The board is equipped with SLINK64, USB and VME interface. It also generates level-1 trigger signals.

For the whole T1 telescope, 2 TOTFED boards are needed for the tracking data and 2 for the trigger system.

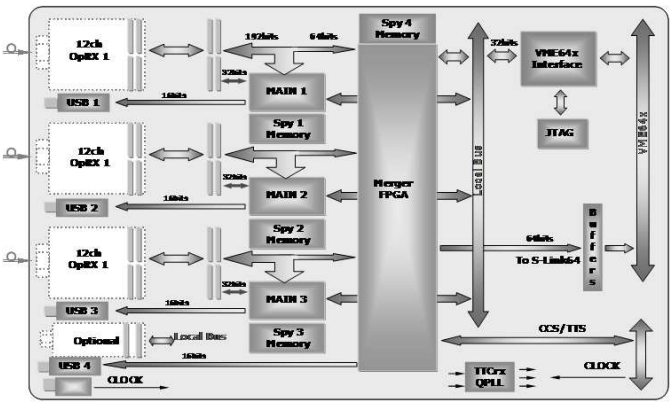

Figure 14: TOTFED block diagram.

The CMS FEC-CCS [19] and TTCci [20] cards are used to interface the on-detector electronics with the Trigger, Timing and Control (TTC) system. They also provide read-out of slow control data from the detector. One FEC-CCS card is enough for T1 telescope.

IV. The T1 Trigger Architecture

All TOTEM sub-detectors will contribute to the generation of the first-level trigger signals. Each sub-detector will provide a set of "primitives", based on particular configurations of the hits recorded: these will then be combined to form the global trigger signals. Their precise definition will critically depend on the luminosity and the running and background conditions, as well as on the targeted physics.

The general architecture of the trigger system is common to the three sub-detectors: a detailed description for T1 is given in the following.

A. Trigger Electronics system

The T1 Trigger information is provided by the anode wires. The trigger bits are generated by the two VFATs chips hosted on the AFEC: each of them provides 8 fast programmable outputs that are made available within the next clock cycle (25 ns) after the detection of a hit on one of the channels. For T1, each trigger bit is configured as the output of a logic OR gate with a group of up to 16 anode wires as input.

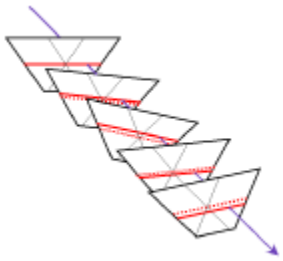

Figure 15: CSCs 3º rotation

Due to the complex detector geometry (the chambers are rotated by 3º with respect to each other, Figure 15) that makes it difficult to have on detector coincidences, the 16 trigger outputs per AFEC are optically transmitted to the T1 Trigger TOTFED boards located in counting room. Here, all trigger bits from the five planes (480 per arm) are collected and properly combined.

Each T1 Trigger TOTFED is equipped with a custom programmable FPGA-based TRIgger MEzzanine (TRIME) that merges the trigger signals received from one telescope arm. The TRIME card runs a configurable algorithm for track roads reconstruction and send the resulting trigger bits, encoded, to the Level ONE General (LONEG) board through a LVDS cable bus (Figure 16).

The LONEG represents the connection node between the TOTEM and CMS trigger systems. It receives, from each TRIME card, 32 encoded trigger bits, 12 bunch crossing counter bits and the 40-MHz LHC system clock.

The synchronisation of the trigger bits is based on the BC0 signal (Bunch Crossing Zero). This signal -- related to the first bunch of an LHC beam revolution cycle -- is issued every 3564 bunch crossings and broadcast by the TTC system. On the detector side, it is received via the control token ring and decoded by a VFAT Trigger Mezzanine (VTM) on the ROC as shown in Figure 5. It is then superimposed onto the trigger data stream transmitted to the counting-room.

The TTC signals are also received by the Trigger TOTFEDs: the trigger bits can thus be temporally aligned to the BC0 signal. The same scheme is used for the 16 trigger bits sent from TOTEM to the CMS global trigger system for common runs [21].

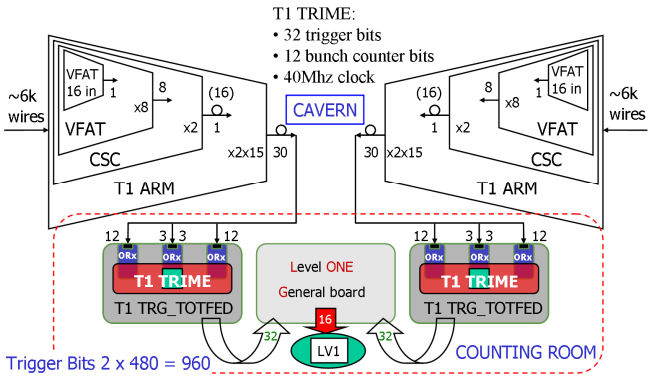

Figure 16: T1 Trigger Architecture.

Once the level-1 trigger is formed, it is transmitted to the detectors using the TTC system through the FEC-CCS card.

The latency of the VFAT can be adjusted to account for the differences in signal delay due to the spatial spread of the subdetectors.

V. Conclusions

After production and testing of prototypes, a pre-production of all boards have been built and tested extensively and have proven to reproduce the required functionalities and performances. The TOTEM T1 detector electronics system is fully integrated within the TOTEM tracking data and trigger building systems; it is also fully compatible with CMS DAQ requirements. The production of the whole T1 custom boards will be completed early in 2009 and installed inside the LHC IP5 experimental area in April 2009.

VI. Acknowledgments

The authors would like to thank Stefano Cerchi for its valuable contribution during the T1 detector integration and also together with Massimiliano Cresta and Giuseppe Gariano for their work on the VFAT chip wire bonding set-up, Fabio Siccardi for its work on the layout of the SPYME mezzanine.

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