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Design Considerations for Area-Constrained In-Pixel Photon Counting in Medipix3

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Medipix3 is a single photon-counting hybrid pixel detector which records the discrete number of photons incident on a pixel. It aims to diminish the effects of charge diffusion across the sensor volume by considering the total charge collected by all pixels within a local neighbourhood during the evaluation of a charge event. The integration of multiple functions within the compact pixel area requires the manual layout of custom transistors, optimizing their physical placement and connections using non-standard techniques. This work describes various area-saving design strategies to optimize the use of available space in the digital section of the Medipix3 pixel.

Summary

The digital section of the Medipix3 pixel two binary counters which can be read out in three readout modes: sequential read/write (SRW), continuous read/write (CRW), and semi-sequential read/write (SSRW). In SRW, both counters record charge events during the same exposure time, and then are read out in turn during the readout time. During readout, no charge events are recorded; thus there is "deadtime."In CRW, one counter records charge events while the contents of the other counter are serially shifted. In this mode, there is no deadtime, but only a single energy threshold is considered in the evaluation of charge events. In SSRW, the counters operate independently.

The digital counters can be configured as two 1-bit, two 4-bit, two 12-bit, or a single 24-bit binary ripple counter. In the event that a counter's maximum value is reached, the charge counting pulses are halted in order to prevent overflow from occurring. The counters can be reset by either serially shifting '0'through all the bits during readout, or by asserting an asynchronous FastClear flag.

The digital circuits occupy a total area of 52 μm by 21 μm. In order to fit as many transistors as possible within that area, minimum-sized transistors are used for the 0.13 μm IBM process.

Schematic-Level Area-Saving Techniques

The 24 counter bits occupy the most amount of space within the digital section of the pixel. Thus, extensive effort was expended on the optimization of the design of the bit. This paper will include a study of different flip-flop architectures which were considered for use in the counter bit. A 16 transistor master-slave static flip-flop was chosen for its small size and robustness. The paper will also discuss how area optimization was considered in the design of the overflow prevention and reset circuits.

Layout-Level Area-Saving Techniques

Standard digital design flows use pre-designed logic gates from digital design libraries. These libraries include a layout description of each logic gate. Place and route tools logic gate descriptions as fundamental building blocks and connect the individual logic gates together to realize the overall circuit. Although this is the simplest way to lay out a circuit, it is not the most area-efficient. Much area can be conserved by overlapping as many pairs of common nodes as possible within the same active area, to reduce the area cost of placing two discrete active areas side by side. Using this principle, the counter circuits are optimized in blocks of up to 120 transistors, and the layout of these transistors are physically placed such that as many pairs of common nodes share the same active area as possible. Furthermore, metal lines and vias are arranged such that the minimum spacing required by the process design rules is respected. Techniques to reduce the number of manual iterations required to find the optimal physical configurations of these transistors will be discussed. Such techniques are appropriate for area-constrained layouts where standard digital libraries and place and route tools cannot be used, and where the speed requirements are relaxed.

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