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A Pixel Read-Out Architecture for the NA62 Gigatracker with on Pixel Time-To-Digital Conversion and Data Derandomization.

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The NA62 experiment will need hybrid pixel sensors with a size of 300 um x 300 um and a time resolution of 150 ps (rms). To meet the timing requirement an adequate strategy to compensate the discriminator time-walk must be implemented and an R&D effort investigating two different options is ongoing. In this presentation we describe the two different approaches. One is based on the use of a costant-fraction discriminator followed by an on-pixel TDC. The other one is based on the use of a Time-over-Threshold circuit followed by a TDC shared by a group of pixels.
The global architectures of both the front-end ASIC will be discussed

Summary

The aim of the proposed NA62 experiment at the CERN SPS is to study the very rare decay of the charged K meson into a pion and neutrino-antineutrino. One of the key components of NA62 will be the Gigatracker, which consists of three matrices of Si-pixel stations, each covering a sensitive area of 60 mm x 27 mm. The silicon sensor will be read-out by 10 front-end ASICs, each one with 45x40 read-out cells.
The Gigatracker should measure the particle trajectory with a space resolution of 100 um and a timing accuracy of 150 ps (rms). The latter is an unusual requirement for a traditional pixel detector and none of the existing systems has such a capability.
Two major issues has to be addressed to achieve the required time resolution: the compensation of the discriminator time-walk and the time measurement with such an high density of channels.Time-walk problem can be addressed either via a constant fraction discriminator (CFD) or a Time-over-Threshold (ToT) correction. While the first approach requires only one measurement per hit, it poses more challenges on the design of the comparator.The issue of precise time resolution with an high readout channel density can be dealt either with a per pixel, Time-to-Amplitude Converter based TDC or via a bank of DLL-based TDCs shared among pixels. The TAC-based TDC solution requires more circuitry on the pixel area, thus potentially creating noise problems. Moreover, the pixel area will receive an high radiation dose and therefore it has to be designed in order to be radiation-tolerant in both total dose and SEU aspects.
On the other hand, the DLL-based TDC has to be much faster in order to keep the dead time under control because the TDC is shared among pixels. Ambiguities can arise if two pixels which belong to the same TDC are hit at the same time. Moreover, the TDC bank has to be placed at the end of the pixel column and therefore the signal carrying the time information has to be transmitted over a well calibrated transmission line in order not to degrade the timing information.
Preliminary investigations did not give a clear advantage of one solution over the others, therefore two prototypes will be designed in order to have an experimental comparison of the performances.

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