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# A front end chip for the INNOTEP project including a 8 bits, 100 MS ADC.

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This paper describes the front end electronic developed for the IN2P3 INNOTEP project by the pole microelectronic Rhone Auvergne. (Collaboration LPC Clermont Ferrand and IPNL Lyon).
This circuit handles the signals coming from LSO crystals trough photo detectors (APD, PM...), and has to provide energy and time measurement, with medium accuracy (8 bits) for the energy but very high accuracy (500 ps at least) for the time.
The electronic consist of a high gain charge amplifier, a fast shaper and a pipe line ADC.
Two versions of charge amplifier and shaper were realized and tested, the ADC is under development, its first version should be send to foundry in June.
This ADC is 4 stages, 2.5 bits per stage pipe line, with open loop track and holds and amplifiers.
It is design in SiGe 0.35µm technology.

## Summary

The signals delivered by APD's are very small: 20 to 50 fC, and must be amplified and shaped with small time constants to allow a good time measurement.
The charge amplifier is then design in the classical way: a common mode folded cascode with high gain and a small feedback capacitor of 500 fF.
The gain achieves is only 1.5 mV/fC, not big enough to be directly digitized.
To overcome this problem, an extra gain of 10 is added in the shaper itself, to obtain a signal of 700 mV, capable to drive an ADC.
The time constant of this shaper must be short (20 ns) to allow a good time measurement, and then needs a high gain, high bandwidth amplifier.
The architecture and measured performances of these two components, including a noise measure, are detailed and discussed.
The second part of the paper concerns the 100 MHz ADC.
The architecture chosen is a 4 stage pipe line.
This architecture needs 6 comparators per stage, a track and hold, a 3 bits DAC and an amplifier with a good accuracy and a gain of 4.
Each design is fully differential and open loop, to try to minimize the kick back noise and the stability problems.
The choice to handle the signal as a current instead as a voltage in the comparison and subtraction stage as well as in the DAC is discussed, and simulation results are given.

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