Evaluation of Multi-Gbps Optical Transceivers for Use in Future HEP Experiments

Luis Amaral
CERN – PH/ESE/BE – Opto
16/09/2008
Outline

• Introduction
  – Optical Links Upgrade for SLHC
  – Project Organization
• Commercial Optical Transceivers
  – Overview
  – Devices Under Test
• Performance Evaluation of Commercial Optical Transceivers
  – Setups and Procedures
  – Performance metrics
  – Specification Proposal for Operation at 5Gbps
• Analysis of the Data and Results
  – Figure of Merit
  – Results of the Devices Under Test
• Summary
Optical Link Upgrade for LHC

• The future SLHC upgrade is expected to increase the LHC luminosity by an order of magnitude. This implies:
  – More data to be transmitted;
    • Assuming more complex DAQ/TTC/SC systems.
  – Higher radiation doses.
• The optical links are also required to have low power dissipation and to reduce the mass inside the detector.
• The solution is to increase the bandwidth of each individual link.
  – The links will be required to:
    • Run at multi-Gbps speeds;
    • Have better radiation tolerance;
    • Operate at low temperatures and in strong magnetic field;
    • Be easy to install and operate.
• The goal is to come up with a common solution that offers:
  – System architectures;
  – Basic building blocks.
Project Organization

Radiation-Hard Optical Link for Experiments

GBT

Versatile Link

GBT

Timing and Trigger
DAQ

Slow Control

GBTX

TIA

LDD

LD

PD

FPGA

TRx

On-Detector
Custom Electronics and Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

Timing and Trigger
DAQ

Slow Control
Project Organization

- The **GBT** project covers the **ASIC design**, verification and packaging.
- The **Versatile Link** project covers **system architectures** and the components.
- One of the main F.E. components is a **Versatile Transceiver (VTRx)**, which results from the customization of a commercial transceiver (TRx).

**On-Detector**
Custom Electronics and Packaging
Radiation Hard

**Off-Detector**
Commercial Off-The-Shelf (COTS)
Custom Protocol

**Spokesperson:**
P. Moreira

**WP 1**
- System
  - WP 1.1 - P2P, SMU, J. Ye
  - WP 1.2 - PON
  - WP 1.3 - Mixed

**WP 2**
Components
- WP 2.1 - F.E. Components, CERN, J. Troska
- WP 2.2 - B.E. Components
- WP 2.3 - Passive Components, Oxford, C. Issever

**Versatile Link**
Spokesperson:
F. Vasey

** Radiation-Hard Optical Link for Experiments **

** Timing and Trigger **
DAQ
Slow Control

** Timing and Trigger **
DAQ
Slow Control
Commercial Transceivers Overview

- The goal is the VTRx customization of a commercial TRx.
- There are several families of commercial optical TRxs to target the Telecom and Datacom standards.
- The GBT project specifies a single lane running at 4.8Gbps which is not a standard.
Commercial Transceivers Overview

- The goal is the VTRx customization of a commercial TRx.
- There are several families of commercial optical TRxs to target the Telecom and Datacom standards.
- The GBT project specifies a single lane running at 4.8Gbps which is not a standard.

SFP+ TRxs seem to be worthy of our attention. What are they made of?

SFPs are similar but rated for lower speeds and the XFPs include a clock and data recovery circuit on both Tx and Rx paths.
### Devices Under Test

<table>
<thead>
<tr>
<th>Device #</th>
<th>TRx Type</th>
<th>Wavelength [nm]</th>
<th>Max. Bitrate [Gbps]</th>
<th>LD/PD type</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SFP</td>
<td>850</td>
<td>4.25</td>
<td>VCSEL/PIN</td>
<td>1/2/4GFC; 1000BASE-SX</td>
</tr>
<tr>
<td>2</td>
<td>SFP</td>
<td>1310</td>
<td>4.25</td>
<td>VCSEL/PIN</td>
<td>1/2/4GFC; 1000BASE-LX10</td>
</tr>
<tr>
<td>3</td>
<td>SFP+</td>
<td>850</td>
<td>10.5</td>
<td>VCSEL/PIN</td>
<td>2/4/8/10GFC; 10GBASE-SR</td>
</tr>
<tr>
<td>4</td>
<td>SFP+</td>
<td>850</td>
<td>10.5</td>
<td>VCSEL/PIN</td>
<td>2/4/8/10GFC; 10GBASE-SR</td>
</tr>
<tr>
<td>5</td>
<td>SFP+</td>
<td>1310</td>
<td>10.5</td>
<td>DFB/PIN</td>
<td>2/4/8/10GFC, 10GBASE-LR</td>
</tr>
<tr>
<td>6</td>
<td>SFP+</td>
<td>1310</td>
<td>10.5</td>
<td>DFB/PIN</td>
<td>2/4/8/10GFC, 10GBASE-LR</td>
</tr>
<tr>
<td>7</td>
<td>XFP</td>
<td>1310</td>
<td>10.3</td>
<td>DFB/PIN</td>
<td>10GBASE-LR/LW</td>
</tr>
<tr>
<td>8</td>
<td>SFP+</td>
<td>1310</td>
<td>10</td>
<td>VCSEL/PIN</td>
<td>Prototype for 10Gbps over SM fiber</td>
</tr>
<tr>
<td>9</td>
<td>SFP+</td>
<td>1310</td>
<td>10</td>
<td>VCSEL/PIN</td>
<td>Prototype for 10Gbps over SM fiber</td>
</tr>
<tr>
<td>10</td>
<td>SFP+</td>
<td>1310</td>
<td>10</td>
<td>VCSEL/PIN</td>
<td>Prototype for 10Gbps over SM fiber</td>
</tr>
<tr>
<td>11</td>
<td>SFP+</td>
<td>1310</td>
<td>10</td>
<td>VCSEL/PIN</td>
<td>Prototype for 10Gbps over SM fiber</td>
</tr>
<tr>
<td>12</td>
<td>SFP+</td>
<td>1310</td>
<td>10</td>
<td>VCSEL/PIN</td>
<td>Prototype for 10Gbps over SM fiber</td>
</tr>
</tbody>
</table>

- Our evaluation was guided towards the **performance at 5Gbps**, i.e. slightly faster than what the GBT protocol is targeting (4.8Gbps).
- Some devices are suitable for **MM links operating at 850nm** and other are suitable for **SM links operating at 1310nm**.
- Some devices have **VCSELs (850 and 1310nm)** and other have **DFB lasers (1310nm)**.

---

TWEPP 2008

Luis.Amaral@cern.ch
Tx Performance Evaluation – Eye Diagram

Setup A (Tx) Optical Evaluation

Clock Generator

PRBS Source

0.5-12.5GHz

PRBS7-PRBS31

Testboard and DUT

Receiver

Transmitter

2m Optical Fiber

10GHz Optical Sampling Module Without Filtering

SDA Scope

PC Automation: Runs through several bitrates and saves data

PRBS7 Test Pattern Jitter @5Gbps:
Tj@1E-12=0.10UI, Dj=0.03UI
20%-80% Rise/Fall Times: 28/27ps
Tx Performance Evaluation – Eye Diagram

**Setup A**
(Tx) Optical Evaluation

- **0.5-12.5GHz**
- **PRBS7-PRBS31**
- **Clock Generator**
- **PRBS Source**
- **Transmitter**
- **Receiver**
- **2m Optical Fiber**
- **10GHz Optical Sampling Module Without Filtering**
- **SDA Scope**
- **PC Automation:** Runs through several bitrates and saves data

**Tx optical output and metrics:**

- **Unit Interval (UI) = 200ps @5Gbps**
- **PRBS7 Test Pattern Jitter @5Gbps:**
  - Tj@1E-12 = 0.10UI, Dj=0.03UI
  - 20%-80% Rise/Fall Times: 28/27ps

**Specification Proposal for 5Gbps Operation**

<table>
<thead>
<tr>
<th>#</th>
<th>Specification</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OMA</td>
<td>300</td>
<td>uW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ER</td>
<td>3</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Eye closure</td>
<td>60</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Rise Time</td>
<td>65</td>
<td>ps</td>
<td>20%-80%</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Fall Time</td>
<td>65</td>
<td>ps</td>
<td>20%-80%</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Total Jitter</td>
<td>0.25</td>
<td>UI</td>
<td></td>
<td>@BER= 1E-12, (1)</td>
</tr>
<tr>
<td>7</td>
<td>Deterministic Jitter</td>
<td>0.12</td>
<td>UI</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The Tx jitter spec. is the 4GFC Tx jitter budget, not including the jitter of the test setup.

**Eye Closure**

\[ \text{Eye Closure} = \frac{\text{Opening}}{\text{OMA}} \]

**by processing the Tx eye raw data**

TWEPP 2008

Luis.Amaral@cern.ch
The mask defines an area which the eye diagram must not cross.

Although based on the 4GFC Tx mask, the jitter and slope are adjusted to the previous specifications and to the jitter of our test setup.

The maximum overshoot is 40% to allow laser driver pre-emphasis and because no filtering is being used.

The green arrows defines the mask margin from 0% to 100%.

The mask defines the limits for the overshoot and ringing but cannot be used to test jitter or rise/fall time compliance.

(2) The margins of the full and center mask must be measured as they will be used to compare different devices.

<table>
<thead>
<tr>
<th>Specification Proposal for 5Gbps Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
</tr>
<tr>
<td>8</td>
</tr>
</tbody>
</table>
Rx Performance Evaluation – Eye and Mask

PRBS7 Test Pattern Jitter @5Gbps (both 850 and 1310nm): 
\[ T_{j}@1E^{-12}=0.11\text{UI}, \quad D=0.04\text{UI} \]

0.5-12.5GHz  PRBS7-PRBS31  850nm/1310nm Optical Tx  2m Optical Fiber  2m Optical Fiber  Testboard and DUT  SDA Scope

555x344 555x117

20%-80% Rise/Fall Times: 
850nm: 38/46ps, 1310nm: 35/42ps

20GHz Electrical Sampling Module Without Filtering

PC Automation: Runs through several attenuations (and bitrates) and saves data

Clock Generator  PRBS Source  Optical Attenuator and Power Meter
Rx Performance Evaluation – Eye and Mask

**Specification Proposal for 5Gbps Operation**

<table>
<thead>
<tr>
<th>#</th>
<th>Specification</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>Total Jitter</td>
<td>0.26</td>
<td>UI</td>
<td></td>
<td>@BER= 1E-12, (3), (4)</td>
</tr>
<tr>
<td>10</td>
<td>Deterministic Jitter</td>
<td>0.11</td>
<td>UI</td>
<td></td>
<td>(3), (4)</td>
</tr>
<tr>
<td>11</td>
<td>Rx Mask Pass/Fail test</td>
<td></td>
<td></td>
<td></td>
<td>Pass/Fail test, (4)</td>
</tr>
</tbody>
</table>

(3) The Rx jitter spec. is the 4GFC Rx jitter budget, not including the jitter of the test set-up.
(4) Measured with an input OMA of 90uW.

**Rx Absolute Mask**

(based on the SFP+ SFI spec.)

Defines the limits for the electrical swing.
Rx Performance Evaluation – BER

Setup C (Rx) Sensitivity Evaluation

Clock Generator

FPGA-Based BER Tester

0.5-6.5Gbps PRBS7-PRBS31 and others

850nm/1310nm Optical Tx

2m Optical Fiber

Optical Attenuator and Power Meter

Testboard and DUT

Receiver

Transmitter

2m Optical Fiber

PC Automation: Runs through several OMAs and saves the BER
Rx Performance Evaluation – BER

By measuring the Bit Error Rate (BER) at different OMAs the BER curve is created.

The Rx sensitivity is defined as the minimum OMA which allows a 1E-12 BER.

### Specification Proposal for 5Gbps Operation

<table>
<thead>
<tr>
<th>#</th>
<th>Specification</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Sensitivity</td>
<td>45</td>
<td></td>
<td>uW</td>
<td>(5), (6)</td>
</tr>
</tbody>
</table>

(5) Specified for a BER of 1E-12.
(6) The sensitivity is specified as an OMA. The setup reads average power and the OMA is calculated using the Tx ER.
Evaluation of the TRx Power Dissipation

- To measure the power dissipation we can simply read current being supplied to the host board.
- The setup is to measure the power at different bitrates and Rx optical input levels.
- In reality we measured the non end-of-life power dissipation at room temperature.

<table>
<thead>
<tr>
<th>Specification Proposal for 5Gbps Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
</tr>
<tr>
<td>----</td>
</tr>
<tr>
<td>13</td>
</tr>
</tbody>
</table>

(7) End-of-life power dissipation and across all operating temperatures and all Rx optical input levels.

Our experience with commercial TRxs tells us that this spec. might be very harsh for non VCSEL-based transmitters.
Analysis of the Data

- The previous test setups generate a very large data set: raw eye diagrams, direct scope measurements, BER curves and measurements of the raw data.
- As we are interested in the TRx performance at 5Gbps we discard all other bitrates and compare the measurements with the specification.
- We flag the devices that do not meet the spec. and we have developed a Figure of Merit (FoM) that combines all the performance data into three numbers: for the Tx part (Tx_FoM), for the Rx part (Rx_FoM) and for the power dissipation (Pwr_FoM).
There is a strong correlation between the performance of the device and the FoM number.
Results

- SFP (devices 1 and 2): Tx problems with rise/fall times or jitter. Rx jitter problems. Both Tx and Rx masks fail.
- SFP+ 850mn VCSEL (devices 3 and 4): Good power dissipation and very good 5Gbps Tx performance. The sensitivity of the PINs at 850nm was found to be around -16dBm. The Rx jitter is good with 90uW of OMA (spec.).
- SFP+ 1310mn DFB (devices 5 and 6): Good 5Gbps Tx performance but high power dissipation. The sensitivity of the PINs at 1310nm was found to be around -19dBm.
- XFP 1310nm DFB (device 7): Great jitter performance but very high power dissipation.
- SFP+ 1310mn VCSEL (devices 8 to 12): Great power dissipation and good 5Gbps Tx performance in most of the modules. Considerable overshoot and ringing.
- The sensitivity of all 850nm PINs was found to about 3dB worse than the sensitivity of 1310nm PINs.
- The only modules that were able to meet all 13 points of our spec. (Tx, Rx and power) were 850 and 1310nn VCSEL-based SFP+ modules.
Summary

• The future Versatile Transceiver will be
  – built from radiation-qualified optoelectronic components;
  – customized from a commercial transceiver.
• Using commercial devices we have developed test methods for transceiver testing to
  – select a transceiver family for VTRx customization;
  – test the performance of the prototype VTRx modules.
• The results from our evaluation of several commercial transceiver modules show that
  – the SFP+ is the most suitable candidate for VTRx customization;
  – to achieve low power dissipation we need to target VCSEL-based lasers;
  – there are 1310nm VCSEL diodes capable of being operated at 5Gbps with sufficient performance.
Extra Slides
The Rx performance is not decoupled from the Tx.

The Jitter is from the entire TRx.

The sensitivity may be different and less consistent.

Rx eye, jitter components and bathtub, mask test

PC Automation

Rx sensitivity

Luis.Amaral@cern.ch
FoM Definition

\[
T_{xFOM} = \frac{100}{15} \times \left( \frac{OMA}{OMA_{Spec}} + \frac{\text{Rise}_{Spec}}{\text{Rise}} + \frac{\text{Fall}_{Spec}}{\text{Fall}} + 3 \times \frac{T_{j_{Spec}}}{T_j} + \frac{D_{j_{Spec}}}{D_j} + 3 \times \frac{\text{Closure}}{\text{Closure}_{Spec}} + \frac{ER}{ER_{Spec}} + \text{FullMaskM} + 3 \times \text{CenterMaskM} \right)
\]

\[
R_{xFOM} = \frac{100}{10} \times \left( 6 \times \frac{\text{Sensitivity}_{Spec}}{\text{Sensitivity}} + 3 \times \frac{T_{j_{Spec}}}{T_j} + \frac{D_{j_{Spec}}}{D_j} \right)
\]

\[
P_{wrFOM} = 100 \times \frac{\text{Power}_{Spec}}{\text{Power}}
\]
Results – Tx and Power

SFP VCSEL modules:
Problems with rise/fall times and jitter. The mask fails.

SFP+ 850mn VCSEL modules: Good power dissipation and very good 5Gbps Tx performance.

SFP+ 1310mn DFB modules: Good 5Gbps Tx performance but high power dissipation.

XFP 1310nm DFB module: Great jitter performance but high power dissipation.

SFP+ 1310mn VCSEL modules: Great power dissipation and good 5Gbps Tx performance in most of the modules. Considerable overshoot and ringing.

---

<table>
<thead>
<tr>
<th>Device #</th>
<th>#</th>
<th>TRx Type</th>
<th>Pass/Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>SFP 4G 850VCSEL</td>
<td>Fail Pass</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>SFP 4G 1310VCSEL</td>
<td>Fail Pass</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>SFP+ 10G 850VCSEL #1</td>
<td>Pass Pass</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>SFP+ 10G 850VCSEL #2</td>
<td>Pass Pass</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>SFP+ 10G 1310DFB #1</td>
<td>Pass Fail</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>SFP+ 10G 1310DFB #2</td>
<td>Pass Fail</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>XFP 10G 1310DFB</td>
<td>Pass Fail</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>SFP+ 10G 1310VCSEL #1</td>
<td>Fail Pass</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>SFP+ 10G 1310VCSEL #2</td>
<td>Fail Pass</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>SFP+ 10G 1310VCSEL #3</td>
<td>Pass Pass</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>SFP+ 10G 1310VCSEL #4</td>
<td>Pass Pass</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>SFP+ 10G 1310VCSEL #5</td>
<td>Pass Pass</td>
</tr>
</tbody>
</table>
Results – Rx and Overall Performance

SFP modules: Our jitter spec. is too harsh for 4G SFP receivers. Also their electrical swing can be much higher than is allowed by our mask.

Modules with 1310nm PINs: The sensitivity at 1E-12 was found to be around -19dBm (about 3dB better than with 850nm PINs).

SFP+ with 850nm PINs: Using an input with an OMA of 90uW (spec.), the jitter seems not to be made worse by the lower sensitivity of 850nm PINs. Using this OMA the jitter seems to depend mostly on the electronics, i.e. TIA, LA and PCB design.

---

<table>
<thead>
<tr>
<th>#</th>
<th>TRx Type</th>
<th>Pass/Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SFP 4G 850VCSEL</td>
<td>Fail/Fail</td>
</tr>
<tr>
<td>2</td>
<td>SFP 4G 1310VCSEL</td>
<td>Fail/Fail</td>
</tr>
<tr>
<td>3</td>
<td>SFP+ 10G 850VCSEL #1</td>
<td>Pass/Pass</td>
</tr>
<tr>
<td>4</td>
<td>SFP+ 10G 850VCSEL #2</td>
<td>Pass/Pass</td>
</tr>
<tr>
<td>5</td>
<td>SFP+ 10G 1310DFB #1</td>
<td>Pass/Fail</td>
</tr>
<tr>
<td>6</td>
<td>SFP+ 10G 1310DFB #2</td>
<td>Pass/Fail</td>
</tr>
<tr>
<td>7</td>
<td>XFP 10G 1310DFB</td>
<td>Pass/Fail</td>
</tr>
<tr>
<td>8</td>
<td>SFP+ 10G 1310VCSEL #1</td>
<td>Pass/Fail</td>
</tr>
<tr>
<td>9</td>
<td>SFP+ 10G 1310VCSEL #2</td>
<td>Pass/Fail</td>
</tr>
<tr>
<td>10</td>
<td>SFP+ 10G 1310VCSEL #3</td>
<td>Pass/Pass</td>
</tr>
<tr>
<td>11</td>
<td>SFP+ 10G 1310VCSEL #4</td>
<td>Pass/Pass</td>
</tr>
<tr>
<td>12</td>
<td>SFP+ 10G 1310VCSEL #5</td>
<td>Pass/Pass</td>
</tr>
</tbody>
</table>

The only modules that were able to meet all 13 points of our spec. (Tx, Rx and power) were 850 and 1310nm VCSEL-based SFP+ modules.