Contribution ID: **55** Type: **Oral**

A MAPS-based readout for Tera-Pixel electromagnetic calorimeter at the ILC

Tuesday 16 September 2008 10:10 (25 minutes)

The leading proposed technology for electromagnetic calorimeters for ILC detectors is a highly granular silicon-tungsten calorimeter. We have developed an active pixel sensor for such a calorimeter, which would have extremely fine granularity, allowing binary pixel readout. A first generation chip (TPAC1) has been fabricated, and this contains a 168x168 pixel array, consisting of 50x50 micron pixels. Each pixel has an integrated charge pre-amplifier and comparator. TPAC1 has been manufactured in the 0.18 micron CMOS INMAPS process which includes a deep p-well. We present recent results of the performance of the TPAC1 chip together with comparison to device-level simulations.

Summary

The ILC physics program requires detectors with unprecedented jet energy resolution. To achieve this goal, the detectors will need highly granular calorimeters and, for the electromagnetic calorimeter, the use of a silicon-tungsten calorimeter has been favored. The granularity and readout requirements of such a calorimeter are closely interrelated. Detailed simulations show that a pixel size of 50x50 microns results in most pixels being only hit once per event. Thus we can employ a simple binary readout using a comparator instead of an analogue measurement. We have designed and fabricated such a CMOS Monolithic Active Pixel Sensor (MAPS) using a novel “INMAPS” process.

The first prototype chip (TPAC1) comprises 168x168 pixels with a total of over 8 million transistors. TPAC1 consists of 4 sub-arrays of 84x84 pixels implementing two distinct pixel architectures, with two variants of each. Each pixel contains four N-well diodes for charge collection, analogue front-end circuits for signal pulse shaping, a comparator for threshold discrimination, and digital logic for per-pixel threshold trim adjustment and pixel masking.

For readout, pixels are served by shared row-logic which stores the location and time-stamp of pixel hits in local SRAM, and was designed to target the 189 ns beam bunch crossing rate of the ILC. The sparse hit data are read out from the columns of logic in the quiet time between bunch trains.

The INMAPS process is a standard 0.18 micron CMOS image-sensor technology but includes a high energy deep p-well implant. A conventional MAPS design will allow charge absorption by any PMOS active devices in the pixel. Hence, the signal charge is shared between the N-well collection diodes and the rest of the circuit, dramatically reducing the efficiency of the pixel. By implanting the deep p-well in the regions of the pixel containing the PMOS active devices, charge deposited in the epitaxial layer is reflected and conserved for collection only at the exposed N-well collection diodes.

The charge collection performance of pixel test structures on the chip has been evaluated using a focused IR laser and clearly demonstrates the improvement achieved by the deep p-well implant. These results will be compared with device simulations. The performance of the main sensor pixels has been evaluated in terms of gain, noise and pixel uniformity. A Fe55 radioactive source is used to calibrate the pixel gain, and the laser is used to evaluate per-pixel gain uniformity. Further tests include cosmic

rays, and alpha and beta radioactive sources. The status of the project, including latest results on the sensor performance, will be reported.

This is an exciting CMOS technology that offers a competitive alternative to the challenges of large-scale silicon detector systems both in performance and cost. The INMAPS process which has been developed under this program would also be applicable to a wide range of other applications.

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Session Classification: Parallel session A1 - ASICs