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SKIROC : A front-end chip to read out the imaging Silicon-Tungsten calorimeter for ILC

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Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which is currently in test beam in Fermilab.
A new version of a full integrated read out chip (SKIROC) has been designed to equip the technologic prototype to be built for 2009. Based on the running physics prototype ASIC (FLC_PHY3), it embeds most of the required features expected for the final detector.
The dynamic range has been improved from 500 to 2000 MIP. An auto-trigger capability has been added allowing built-in zero suppress. The number of channel has been doubled reaching 36 to fit smaller silicon pads and the low-noise charge preamplifier now accepts both AC and DC coupled detectors. After an exhaustive description, the extensive measurement results of that new front-end chip will be presented. The characteristics of the new features such as internal ADC, auto-gain select or self-trigger will be detailed. The results on the technological R&D concurrently conducted on the ultra-thin PCB hosting both the front-end electronic and the silicon detectors will also be described.

Summary

A new front-end chip called SKIROC –standing for Silikon Kalorimeter Read-Out Chip –has been designed to read-out the upcoming generation of Si-W calorimeter featuring ILC requirements. The analogue core of SKIROC is based on the front-end electronic designed for that physics prototype. It has been enhanced in many ways using an intermediate prototype called ILC_PHY4. The Maximum input charge has been extended from 500 to 2000 MIP.
The number of channel has been doubled –reaching 36 - to fit a pad size reduction in the silicon detector design conducted concurrently. A stand alone working capability comes along with the full power pulsing feature. That means SKIROC does not need any external component such as decoupling capacitance or bias resistor involving a huge room saving. The wake up sequence duration of the power pulsing is around 2µs to ensure a lower than 1% duty cycle in an ILC-like beam structure, involving more than two order of magnitude of power saving.
Beyond the analogue core improvement, many features have been implemented in SKIROC. A channel by channel auto-trigger capability has been added allowing a built-in zero suppression. A multi-channel ADC is embedded. The trigger and gain selection threshold is set by an internal dual DAC. Voltage references used in the analogue core use a bandgap reference to get rid of temperature and supply variation. A digital core driving all the analogue features and the digital communication with the DAQ has been designed and is implemented in a FPGA to get debugged and improved before being embedded in the next version.
The SKIROC chips will be used to equip the 40,000-channel ECAL foreseen for 2009 that will validate the technological choices for the 82-million-channel final detector. Many of the final detector requested features have been embedded and the performance has been greatly improved compared to the physics prototype front-end chip. The production of that ASIC is foreseen in summer 2008 to be able to take data in 2009, before the engineering design report of the final detector planned for 2010 by the ILC Worldwide Study Bureau.

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