Contribution ID: **53** Type: **Oral**

SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out

Tuesday 16 September 2008 15:00 (25 minutes)

SPIROC embeds cutting edge features that fulfil ILC final detector requirements. It has been realized in 0.35m SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.
SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 1 ns accurate TDC.
An analogue memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analogue memory content (time and charge on 2 gains). The data are then stored in a 4kbytes RAM.

Summary

The SPIROC chip is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with Silicon photomultiplier (or MPPC) readout. This ASIC is due to equip a 10,000-channel demonstrator in 2009.
SPIROC is an evolution of FLC_SiPM chip used for the ILC analogue hadronic calorimeter physics prototype. It was submitted in June 2007 and the test started in September 2007. It embeds cutting edge features that fulfil ILC final detector requirements. It has been realized in 0.35 µm SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.
SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 1 ns accurate TDC.
An analogue memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analogue memory content (time and charge on 2 gains). The data are then stored in a 4 kbytes RAM. A very complex digital part has been integrated to manage all theses features and to transfer the data to the DAQ which is described on.
This new electronics readout is intended to be embedded in the detector. One important feature is the reduction of the power consumption. The huge number of electronic channels makes crucial such a reduction to 25 µWatt per channel using the power pulsing scheme, possible thanks to the ILC bunch pattern: 2 ms of acquisition, conversion and readout data for 198 ms of dead time. However, to save more power, during each mode, the unused stages are off.
After an exhaustive description, the extensive measurement results of that new front-end chip will be presented.

Primary authors: Mr DE LA TAILLE, Christophe (Laboratoire de l'Accélérateur Linéaire); Mr DULUCQ, Frédéric (Laboratoire de l'Accélérateur Linéaire); Mrs MARTIN-CHASSARD, Gisèle (Laboratoire de l'Accélérateur Linéaire); Mr FLEURY, Julien (Laboratoire de l'Accélérateur Linéaire); Mr RAUX, Ludovic (Laboratoire de l'Accélérateur Linéaire); Mr BOUCHEL, Michel (Laboratoire de l'Accélérateur Linéaire); Mr CALLIER, Stéphane (Laboratoire de l'Accélérateur Linéaire)

Presenter: Mr FLEURY, Julien (Laboratoire de l'Accélérateur Linéaire)

Session Classification: Parallel session A2 - ASICs