Commissioning Status and Results of ATLAS Level1 Endcap Muon Trigger System

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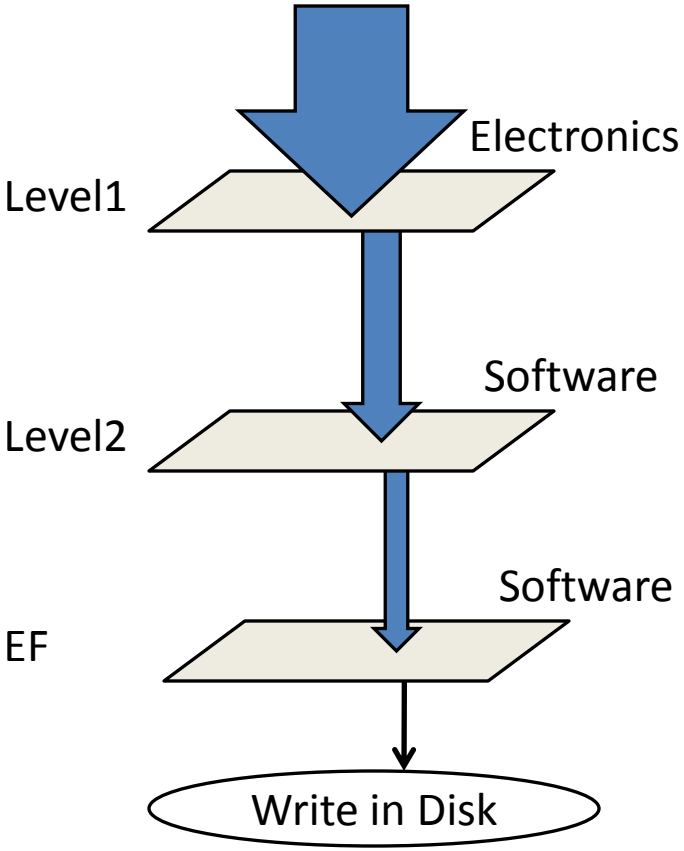
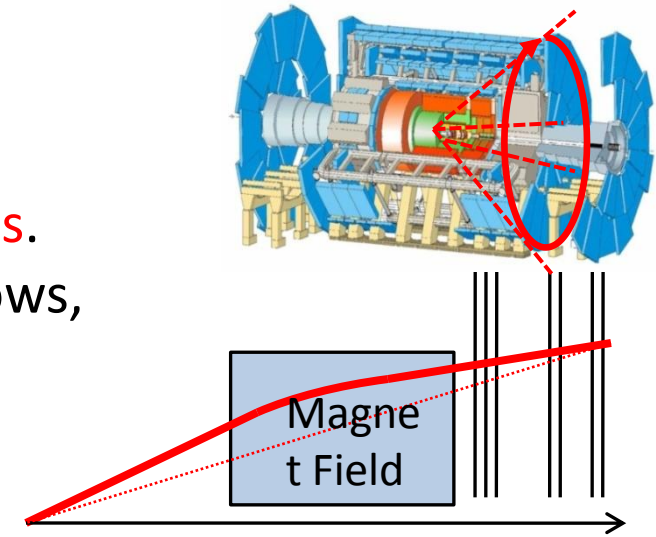
ATLAS Trigger DAQ System

- Trigger in LHC-ATLAS Experiment
  - 3-Level Trigger System
    - Level1 Hardware Trigger
      - 40MHz → 75kHz
      - 2.5 m sec
    - Level2 Software Trigger
    - Event Filter Software Trigger
  - Reduction 40MHz → 200Hz
- Level1 Trigger requirement
  - L1 latency ≤ 2.5 μ sec
  - L1 Rate ≤ 75kHz

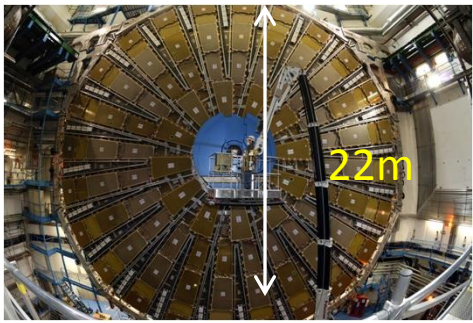


Level1 Endcap Muon Trigger System

- **TGC (Thin Gap Chamber)**
  - Gas chambers with fast signals
    (gap=1.4mm / wire spacing=1.8mm)
  - Wire R / Strip Phi Readout, total 320k channels.
  - Binary hit signal quantized in 25ns time windows, which is synchronized to LHC clock.
    (Bunch Crossing ID::BCID)



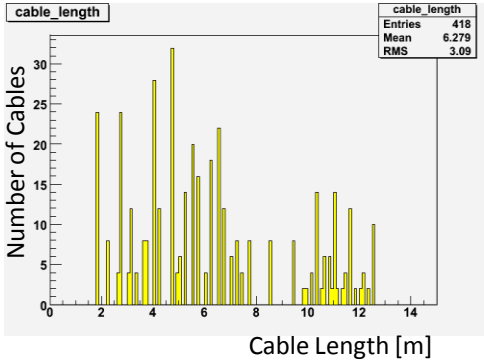
- **Measurement of Selection of high Pt muon (6GeV/c)**
  - Achieved by hit coincidence of 7 layers of TGC in every 25 n sec.
  - Picking high Pt muons out by rough tracking.

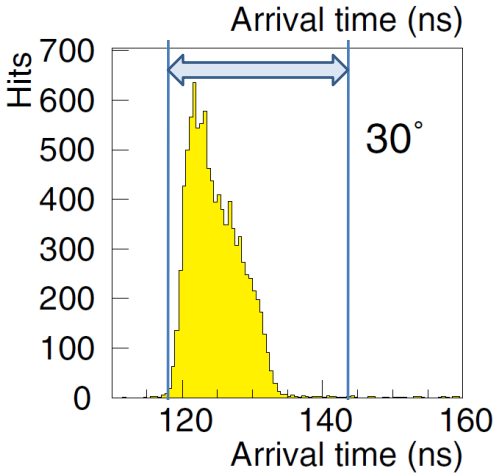


40MHz pipeline trigger with 3-step coincidence logic (SLB/HPT/SL) connected with serial links.

Requirements

- **Alignment of signals for all 320,000 channels with 1ns precision for bunch crossing ID(BCID)**
  - Variety of cables : 45 types (1.8m .. 12.5m)
  - Range of Time of Fright : 47ns - 53 ns
    - Delay of signals against collisions is different channel by channel.
  - TGC intrinsic time resolution : ~25ns
    - Gate should be opened with proper delay against collision timing.
- **Establishment of synchronization in High speed serial links for data transfer for correct work of 3-step coincidence logic.**
  - Delay adjustment of the links in a half clock at the receiver side.
  - Establishment of synchronization procedure for the serial link.

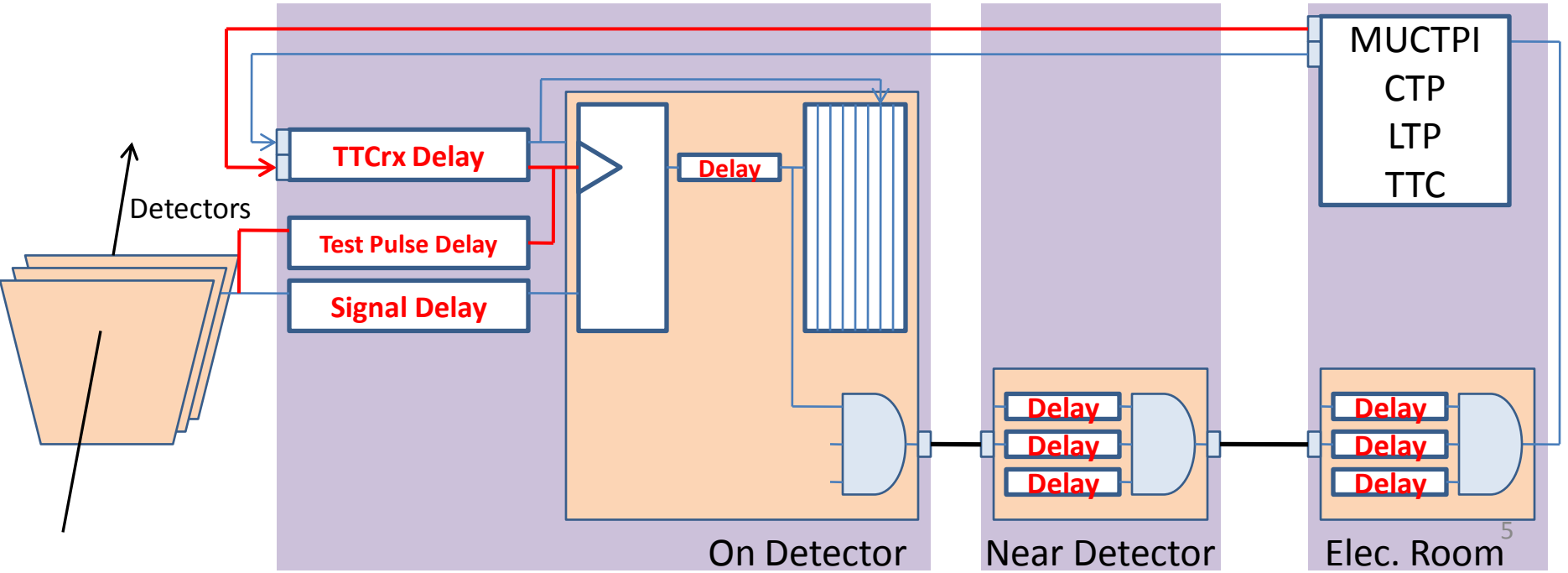




Overview of TGC timing Alignment system

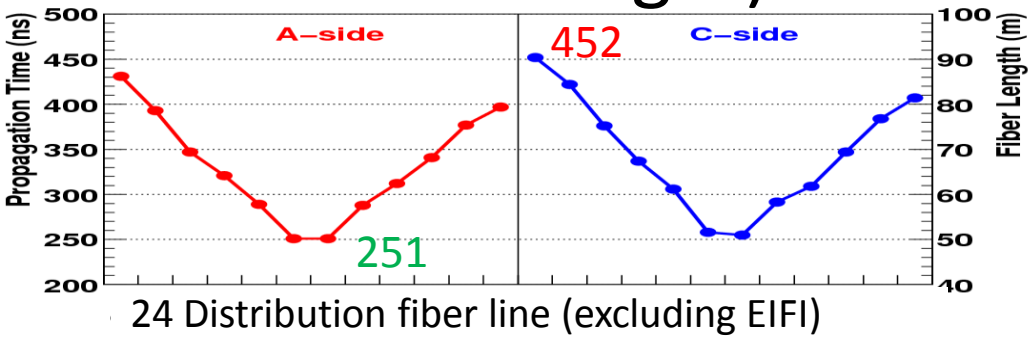
- Variable delay to align signal timing set up at each module.
- A functionality to inject test pulses emulating TGC hit signals for all 320k channels

  - TTC signals (L1A/clock/ECR/BCR/Reset/test pulse) alignment.
  - Hit signal delay (TOF + cable delay) alignment.
  - Delay alignment in serial link cable.

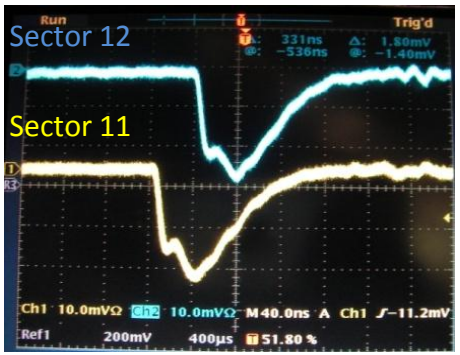


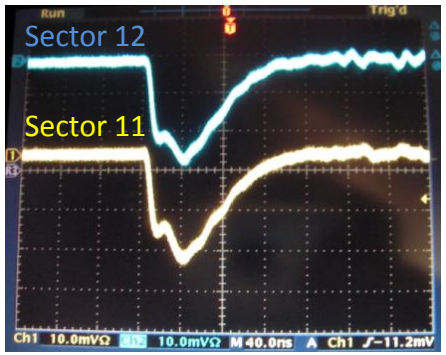
TTC signals alignment

- TTC signals are sent to all frontend electronics with 100 fiber links (26 different fiber length).
  - Max 452ns
  - Min 251ns



- TTCrx chip delay
  - Fine Delay (100ps Step)
  - Coarse Delay (25ns Step)

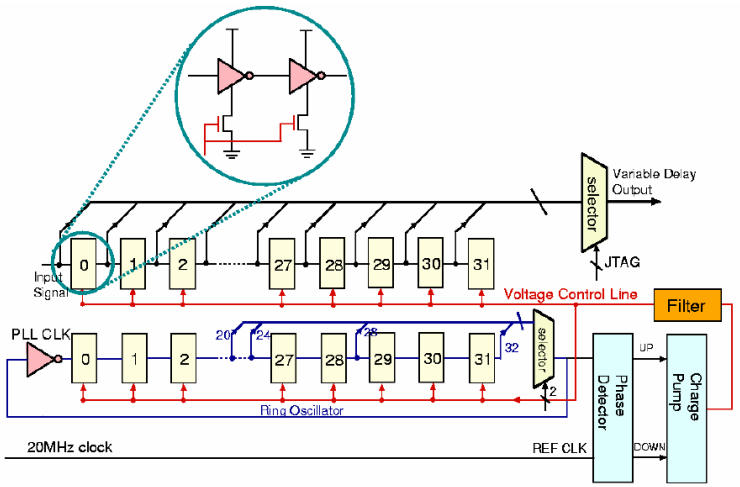




- All fiber length difference is absorbed in TTCrx chip.

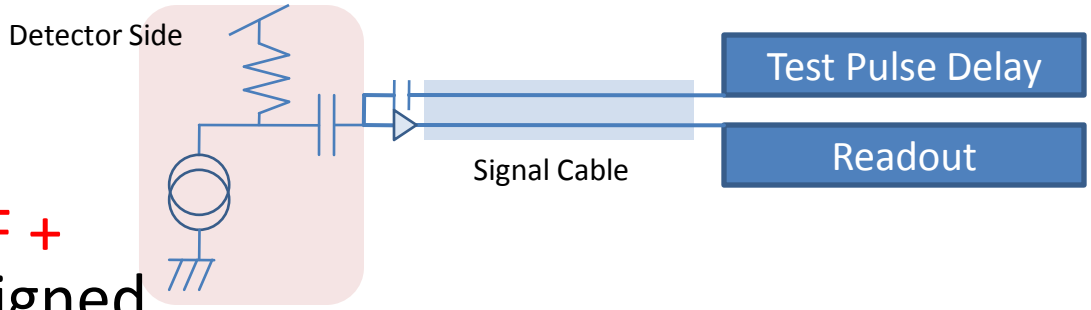
Signal Delay Alignment

- Raw signal from detectors should be aligned before synchronization to LHC clock (40MHz).
- Signal Delay with 1nsec (25nsec/28) Step
  - Dividing 25ns (40MHz) into 28 with PLL circuit.



32 step variable precise delay with PLL circuit (1Step=25ns/28)

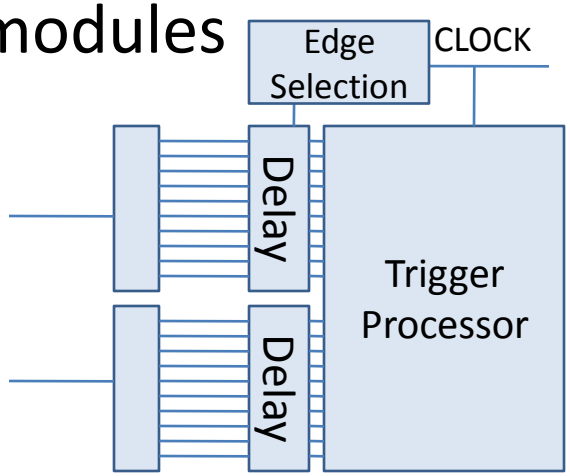
- All the cable delays have been measured with test pulses.
  - MAX 116.0 n sec
  - MIN 65.3 n sec



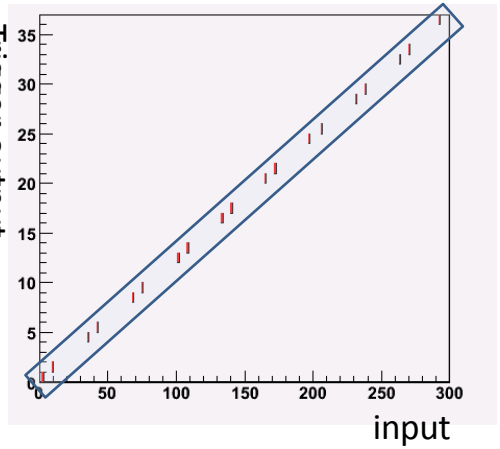
- All the signal timings (TOF + cable delay) have been aligned.

Delay alignment in serial links cables.

- Alignment of propagation delay between modules
  - Delay with unit of 25ns at receiver side.
  - Clock edge selection for input to Trigger Processor



- All the Trigger cablings have been tested with 2100 track patterns generated from test pulses.
  - Confirmation of delay adjustment
    - All information in trigger line (12,096 bits/clk) is checked to have good agreement with input track pattern.
  - Confirmation of connections of all the cables.
    - Swap and mis-connection are fixed.



Synchronization Procedure for G-Link

Synchronization process in sending all 0 data would cause mis-alignment due to failure in header bit identification.

C-Field			
c0	c1	c2	c3
1	1	0	1
0	0	1	0
1	0	1	1
0	1	0	0

	w Field	c Field	w Field (inverted)	c Field
Correct	0000 0000 0000 0000	1101	1111 1111 1111 1111	0010
Incorrect	0000 0000 0000 0001	1011	1111 1111 1111 1110	0100
Idle mode	1111 1111 0000 0000	0011	1111 1100 0000 0000	0011

All 0 pattern is not good for link locking.
(Bit pattern can be interpreted in 2 ways)

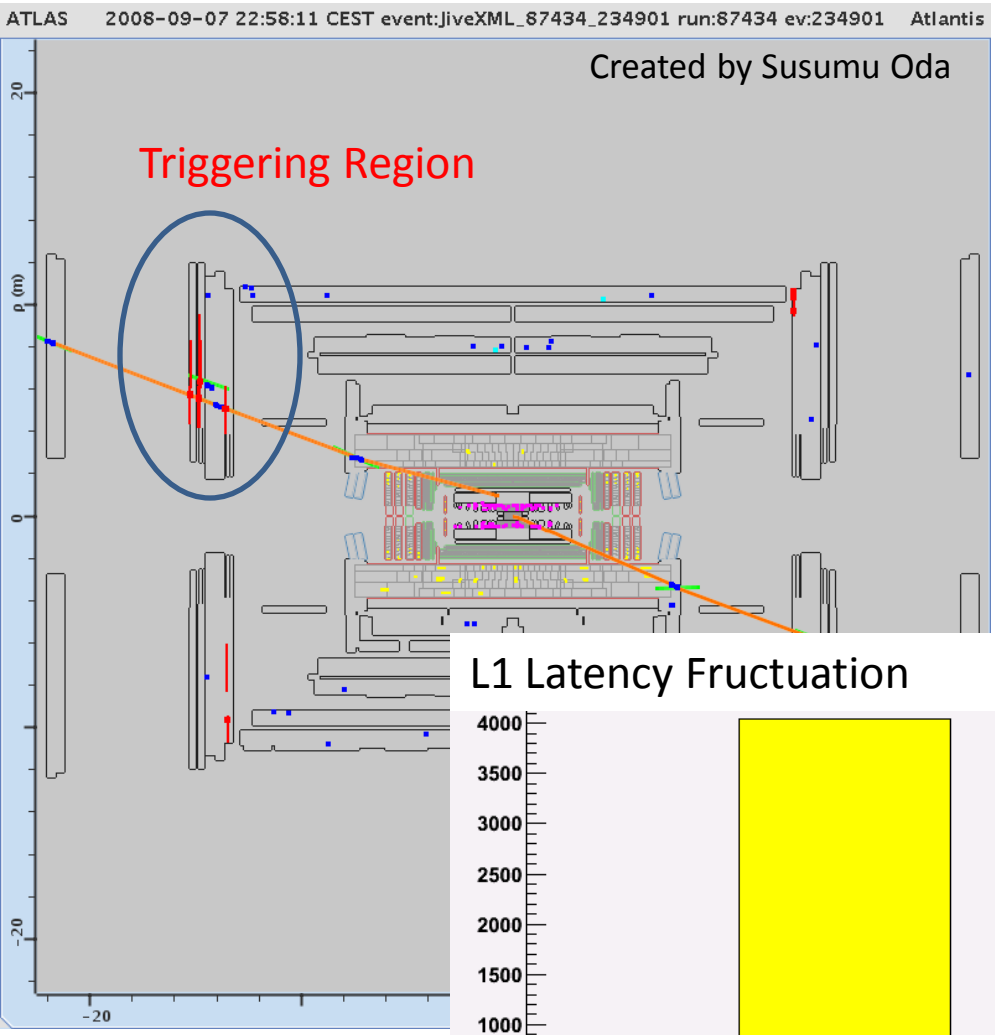
Synchronization process in sending idle words solves the problem, and the procedure has been implemented in ATLAS DAQ framework.

Establishment of Operation Procedure

- Results measured above has been stored and available in appropriate data format.

- Following items have been implemented in ATLAS DAQ operation framework.
  - TTC signals alignment
    - 196 Registers Configuration in TTCrx chips.
  - Hit signal delay Alignment
    - 9989 Registers Configuration in frontend electronics.
  - Delay alignment in serial link cable
    - Delay Registers for HPT 1632 / SL 720 input ports Configuration.
  - G-Link Initialization Procedure

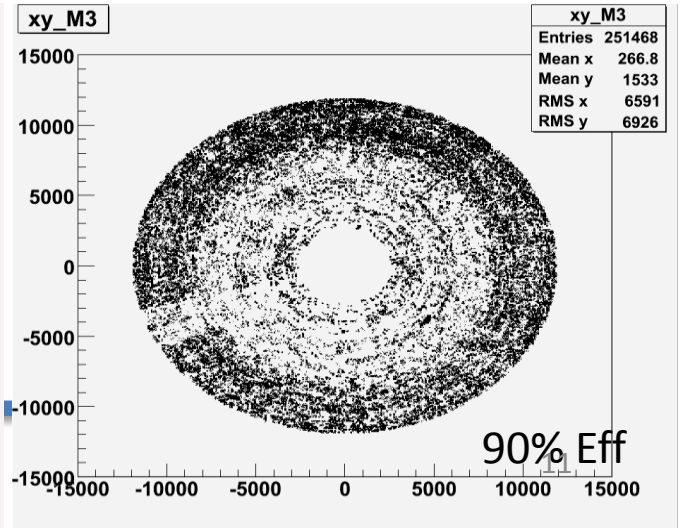
Data in Cosmic Commissioning



TGC's Triggering Cosmic Ray Event

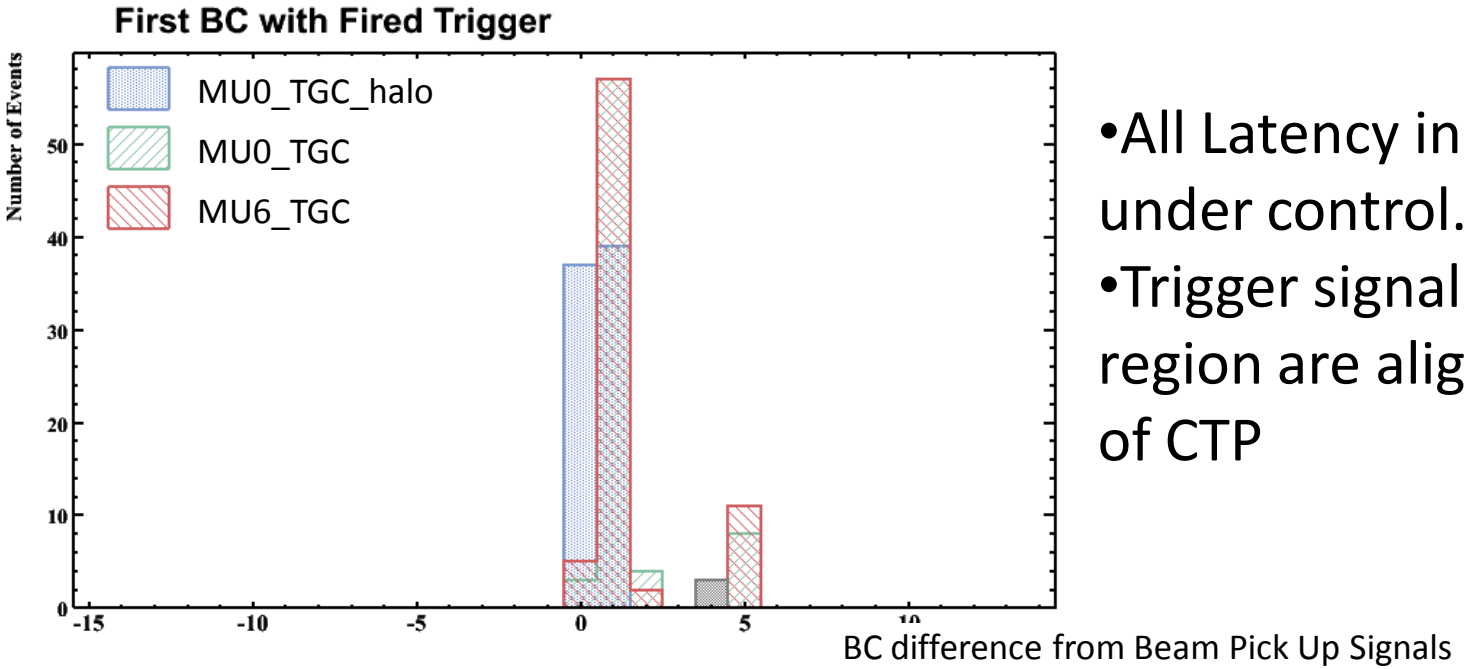
- All the 7 layers coincidence was fired with cosmic ray muon.
- Associating Track was detected

- L1Latency is stable within 2.5 μ sec.
- In all regions, muon is triggered.



First Beam @ 10th Sep.

- Trigger Timing from Endcap muon trigger against Beam pickup signals.



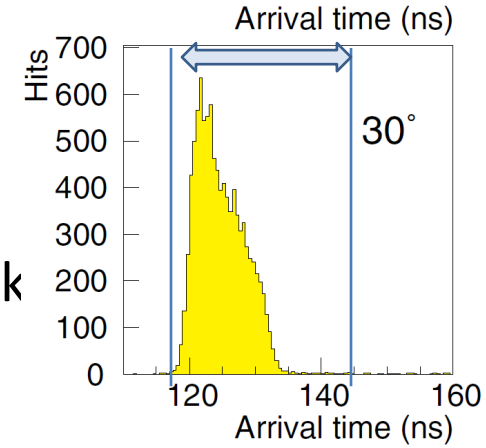
- All Latency in front end is under control.
- Trigger signal from all region are aligned at input of CTP

- ***Endcap muon trigger is ready to have synchronization with LHC collisions !***

Summary

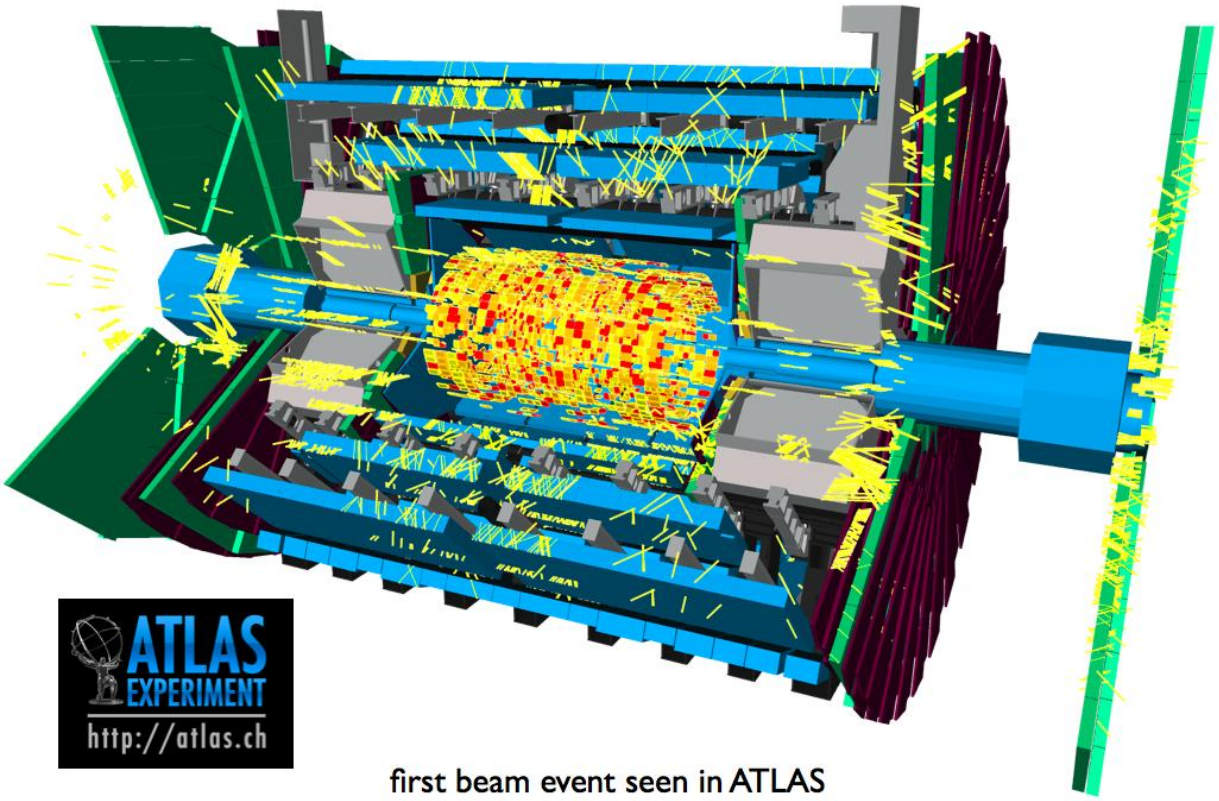
- For smooth operation in level1 muon trigger, we achieved
  - TTC signals alignment.
  - Hit signal delay (TOF + cable delay) alignment.
  - Delay alignment in serial link cable.
  - Establishment of synchronization for G-Link.

- We are ready for the first beam collision!
  - Stable Latency
  - High Efficiency
  - All procedures implemented in ATLAS DAQ framework



- ***Future plan with beam collision***
  - Optimization of phase difference between signal and clock.
  - Optimization of Gate width.
  - Optimization of HV/ Threshold in high radiation environment.

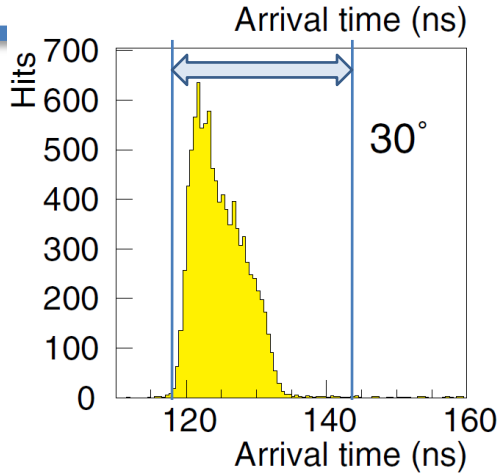
First Beam Event Display @ 10th Sep.



first beam event seen in ATLAS

We are ready for starting collision !

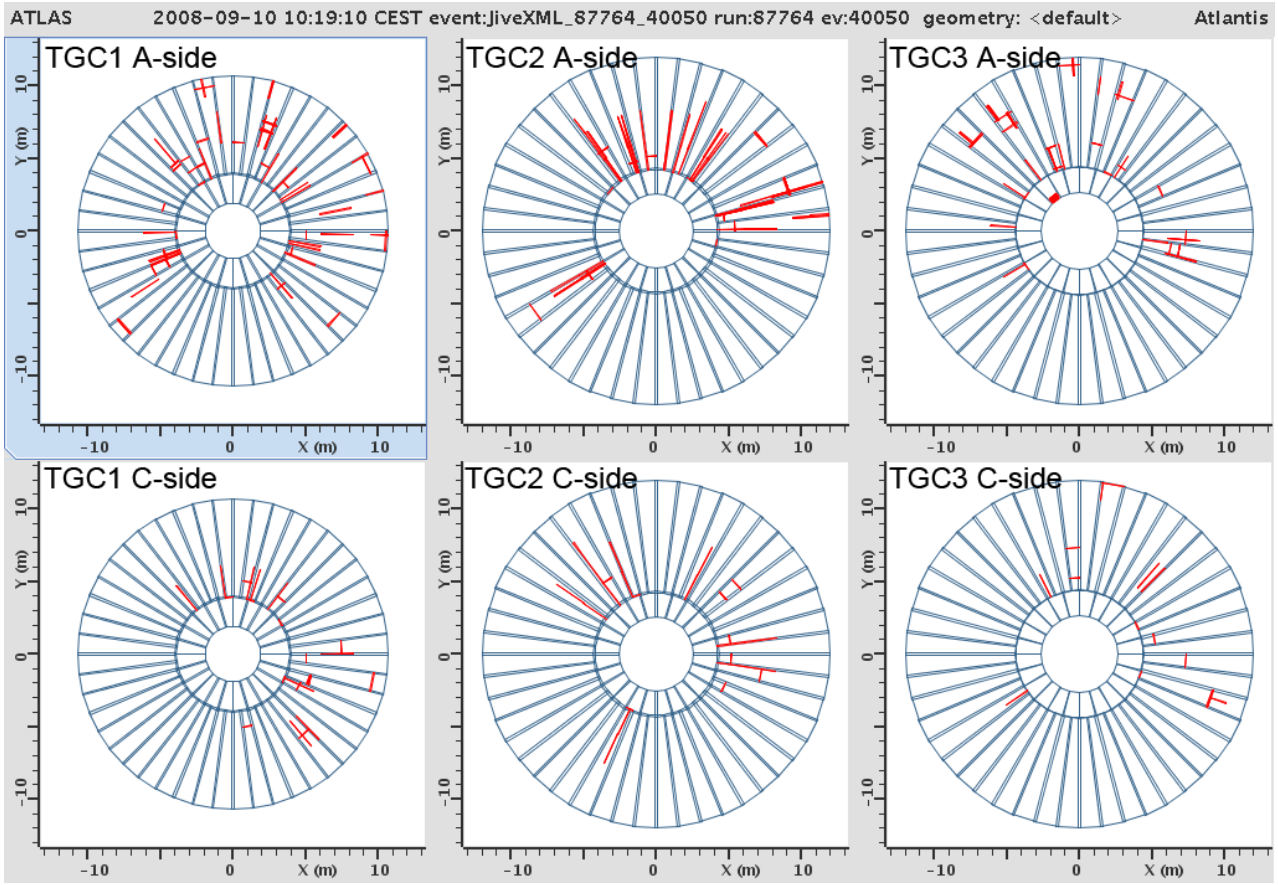
Plans for first collision

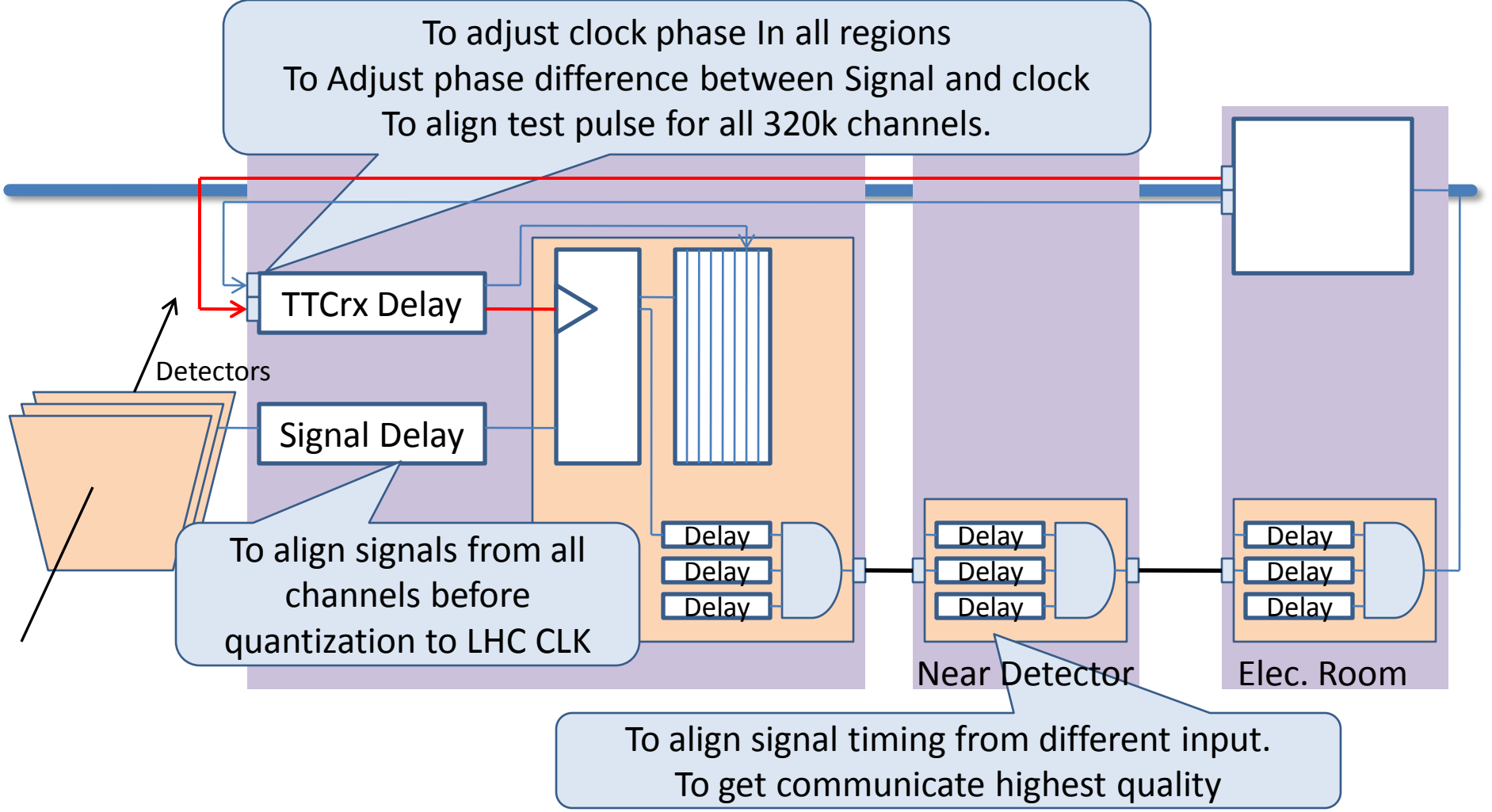


- Optimization of phase difference between hit signal and clock.
  - TTCrx delay is available.
  - Efficiency of Bunch Crossing ID gets highest.
- Gate width optimization
  - All time jitter of TGC can be absorbed by getting gate wider than 25ns.
  - It will be done by monitoring trigger rate.
  - Effective chamber efficiency will be the highest (95%)
- HV/Threshold voltage optimization

These items are under preparation,
and after first collision soon it will be done.

For First Beam @ 10th Sep.



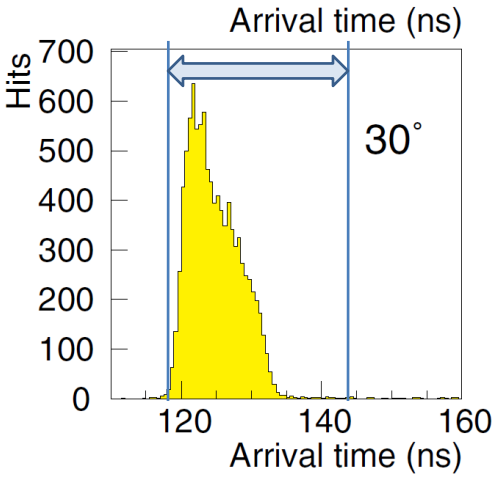


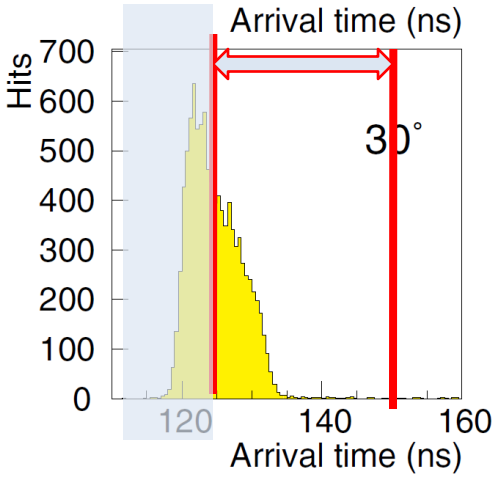
Only after these fine Adjustment, we can get the highest quality muon Trigger.

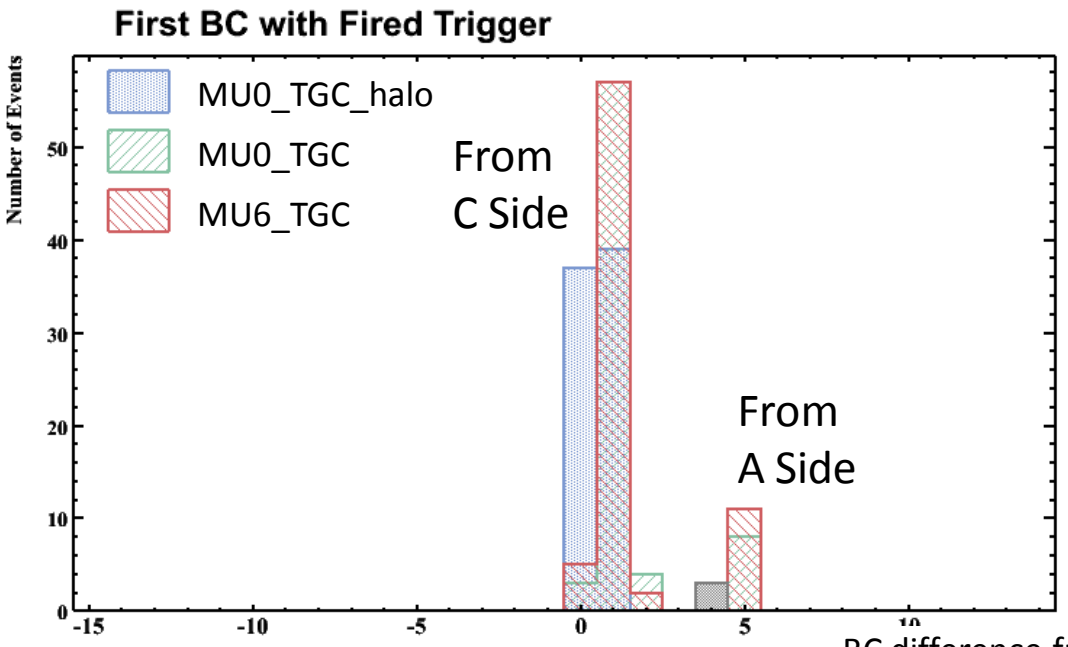
Strategy

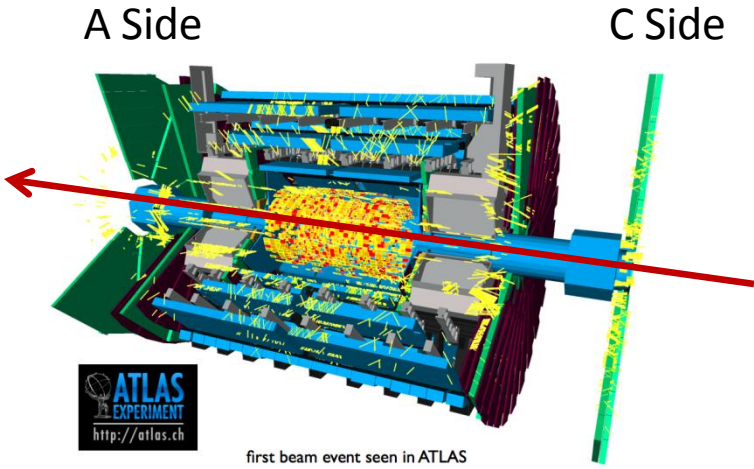
- Align Test pulse timing, clock phase
- Optimize timing parameters from the upper part with test pulse

Timing for Gate to Open









BC difference from Beam Pick Up Signals