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A dual scale 1mW full flash ADC for the ILC vertex detector

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The resolution needed in the CMOS sensors of the ILC vertex detector implies a digitization of each pixel by a small, 4-5 bits, dedicated ADC.
The ADC characteristics, given by the constraints of the pixel matrix and its read out are for one ADC per column : 10 MS, 25 micron width and about 1mW consumption, thank to the fact that this power could be turn off 99 % of the time.
To fit these requirements, several architectures were designed in different laboratories.
This paper describes the results of the LPC Clermont Ferrand R&D witch is a two scales, 20 MS,1mW, 47 µm width, full flash ADC sharing two columns.

Summary

The resolution needed in the CMOS sensors of the ILC vertex detector implies a digitization of each pixel by a small, 4-5 bits, dedicated ADC. The CMOS sensor chip MIMOSA designed at IPHC Strasbourg, is line column organized and read out column by column at 10MHz to avoid dead time. The pitch between columns is 20 to 30micron for a column number of several hundreds to thousand. The available area for the ADC is then 20 to 30micron width by 1.2 mm length.

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First, the choice of the flash architecture for these particular features is discussed, and the concept of a non regular interval between comparators is introduced. Compare to the others architecture, the flash ADC exhibits the fastest response time, a poor differential linearity, a high number of comparators, and a high consumption. In the particular goal of pixel digitization, the fast response time is an advantage, and a good differential linearity is not mandatory at all.

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