The Level 0 Pixel Trigger System for the ALICE experiment: implementation, testing and commissioning

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On behalf of the ALICE Silicon Pixel Detector Team

1CERN, European Organization for Nuclear Research
Outline

- ALICE Silicon Pixel Detector
  - Detector modules
  - Fast-OR signals

- Pixel Trigger System
  - Description
  - Features
  - Tests and qualification
  - Commissioning

- First operation
The ALICE experiment at LHC

- Heavy ions collisions
  - Quark gluon plasma

- **Proton-proton collisions**
  - $p_t \sim 0.6 \text{ GeV}/c$
Silicon Pixel Detector

- 120 detector modules (*half staves*)

![Diagram of a Silicon Pixel Detector showing dimensions: 39 mm, 76 mm, 400 mm.](image)
Each half stave (120):
- Si pixel sensors (pixel size 425x50 um$^2$)
- 10 readout pixel chips (32x256=8192 pixels)
  - 10 MHz
- Readout Multi Chip Module
  - 40 MHz
  - Provides 10 MHz to pixel chips
Fast-OR signals

- Pixel chip prompt Fast-OR
  - Active if at least one pixel hit in the chip matrix
  - 10 on each of 120 optical links (1200)
  - Transmitted every 100 ns

- Low latency pad detector
  - 1200 pads of 13x14 mm$^2$
Pixel Trigger System

- Overall latency: **800 ns**
- Space occupancy (1 crate)
- Bottleneck: data deserialization and Fast-OR extraction
  - Processing time < 25 ns

120 G-Link

To DAQ

1200 bits @ 10 MHz

CTP

Optical splitters

Fast-OR extraction

Processing

Pixel Trigger electronics

Spatial occupancy (1 crate)

Processing time < 25 ns

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Pixel Trigger system electronics

- 9U VME size processing board (BRAIN)
  - Main processing FPGA (960 user I/O pins, 1513 BGA)

- 2x5 receiver boards (OPTIN) connected as mezzanine boards

- High speed optical interfaces
  - Alice Detector Data Link
  - Timing Trigger

- Data flow parallelism (~1000 lines)
  - 800 impedance matched lines
  - Digitally Controlled Impedance
  - Double Data Rate
OPTIN receiver board

- 12 channels
  - Parallel optical receiver module
  - 12 closely packed G-link deserializer ASICs
BRAIN and OPTIN boards

OPTIN boards

Optical fan-in cable

Processing FPGA

DDL SIU

Control FPGA

400 mm
Pixel Trigger system crate
Interconnection test and power consumption

- Electrical interconnects
  - Full JTAG testing
  - Dedicated tests for
    - lines non accessible by JTAG
    - high speed differential lines

- Heat sinks on all regulators and deserializers
  - Peak board temperature: 45 °C (measured)
  - Peak junction temperature: 72 °C (thermal model)

- Currents overestimated in design phase
  - Thermal model was *too conservative*

<table>
<thead>
<tr>
<th></th>
<th>$I_{5V}$ [A]</th>
<th>$I_{3.3V}$ [A]</th>
<th>$P$ [W]</th>
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</thead>
<tbody>
<tr>
<td>OPTIN</td>
<td>2.8</td>
<td>0.375</td>
<td>15.3</td>
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<tr>
<td>BRAIN</td>
<td>7.9</td>
<td>1.6</td>
<td>45</td>
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<tr>
<td>Total PIT</td>
<td>36.1</td>
<td>5.4</td>
<td>198</td>
</tr>
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</table>
Clock distribution

- Measurement of phase distribution
- Processing FPGA clock
  - Phase correction in order to place it at the centre of the distribution
  - Digital Clock Management
- Measured signal propagation delay
  - Design: 7.8 ns/m
  - Measured: 6.95 ns/m
Optical link BER tests

- Full Fast OR data path Bit Error Rate test
  - 12 channels in parallel, each OPTIN tested sequentially
  - Pseudo random data
  - Link optical power: $-18.5 \text{ dBm}$, 0.5 dBm margin

<table>
<thead>
<tr>
<th></th>
<th>Duration</th>
<th>$N_{\text{bits}}$</th>
<th>Errors</th>
<th>BER (99% c. l.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical</td>
<td>1.5 hrs</td>
<td>$5.7 \cdot 10^{12}$</td>
<td>0</td>
<td>$&lt; 8.1 \cdot 10^{-13}$</td>
</tr>
<tr>
<td>Max</td>
<td>17.8 hrs</td>
<td>$7.7 \cdot 10^{13}$</td>
<td>0</td>
<td>$&lt; 6 \cdot 10^{-14}$</td>
</tr>
</tbody>
</table>
Fast OR data path integrity

- Fast OR dedicated lines (600) Bit Error Rate test
  - 10 OPTIN boards, 120 channels simultaneously running
  - On board generation of User Defined data functionality (pseudo random sequences)

- Duration: 15 hrs
  - \( N_{\text{bits}} = 6.48 \cdot 10^{14} \)
  - Errors = 0
- BER < \( 7.1 \cdot 10^{-15} \) (99% c.l.)
Pixel Trigger system control

- Custom control interface
  - ALICE Detector Data Link
  - On board PCI like bus
    - CONTROL FPGA acts as bus master and bridge to DDL

- Reliability
  - Transaction *acknowledgement*
  - *Parity* checking
  - *Error recovery*

- Read/write test pseudo-random data
  - Typical duration: 15 mins, $\sim 6 \cdot 10^8$ bits exchanged, 0 errors
  - Longest: 12 hrs, $\sim 3 \cdot 10^{10}$ bits, 0 errors

- See poster by *Cesar Torcato Matos*
Latency measurement

Test pulse ->

PIT output ->

- Laboratory measurement
- In ALICE
  - 768 ns (best case)
  - 793 ns (realignment)
Installation in ALICE experiment

- TTC
  - 107.6 ± 0.15 m
  - Clk
  - Serial

- C side
  - 36.6 ± 0.2 m
  - Data

- A side
  - 38.5 ± 0.2 m

- Optical splitters

- PIT main outputs

- Central Trigger Processor
  - L0 in
  - LTU

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Synchronization

- 40 MHz clocks aligned by equalizing fibers length
- 10 MHz clock phases aligned by broadcast signal on TTC
- One clock period uncertainty left -> Measure relative phases
  - Measure arrival time of trigger feedback

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OPTIN receiver board channel

- Trigger feedback arrival clock period is time stamped
- Discrete delay can be added to compensate for misalignments
- Automatic driver function to measure latencies and set delay
Frame alignment

A side

C side
Cosmic radiation in the cavern

- Pixel trigger used for cosmic data taking
  - SPD only
  - ALICE (ITS + TPC)

- Alignment data
  - 65000 events ≥ 3 clusters in SPD
  - 35000 events ≥ 4 clusters in SPD
  - Showers
Cosmic data clusters

- **Rate 0.09 Hz – 0.12 Hz**
  - Well in agreement with Monte Carlo and measured flux in the cavern

- **Cluster distribution**
  - 99.5 % of events with correct cluster distribution
The ALICE Pixel Trigger system allows to include the prompt Fast-OR outputs of the Silicon Pixel Detector in the Level 0 trigger decision

- ALICE is the only LHC experiment including the vertex detector in the first trigger decision from startup

The Pixel Trigger system

- Installed and operational
- Board level and system level challenging requirements
- Highly compact solution including original developments
- Commissioning and first operation
LHC beam injection tests

August 2008: the ALICE experiment detected “LHC related particles” during the very first injection tests.

SPD was recording data and self-trigerring with the Pixel Trigger system.
References:


Spare slides
SPD detector
Triggering with SPD Fast-OR

- Extract and process Fast-OR signals
- Generate input for the Level 0 (fastest) trigger decision
  - 1200 Fast-OR signals on 120 optical links every 100 ns

- Proton-proton
  - Minimum bias
  - High multiplicity studies
  - Topological selection (jets)

- Heavy ions
  - Selection of impact parameter

- Algorithms
  - Topology (Global OR, Vertex)
  - Multiplicity
  - Boolean functions of 1200 Fast-OR bits
Trigger algorithms

- Combinational (boolean AND/OR) functions of 1200 Fast-OR bits
  - Occupancy (multiplicity)
  - Coincidence trigger (topology)
- Not possible: iterative algorithms on data set

Example: vertex trigger

- Pseudo-Tracklet: one chip hit on inner and one on outer layer, in line with region +/-10 cm around vertex
- Chip map for pixel trigger electronics calculated from simulation: (L11,L21), (L12, L22), ... , (L1n, L2n)
- FPGA looks for at least 1 out of 11000 pseudo-tracklets
  - Processing time 12.4 ns (Xilinx ISE)
  - 4% of FPGA resources (Xilinx ISE)
- FPGA counts how many out of 11000 tracklets are present
  - ~27 ns processing time (Xilinx ISE)
  - 5% of FPGA resources (Xilinx ISE)
Multiplicity trigger

![Graph showing charged multiplicity distribution](image)

- Inelastic
- nFO inn. layer > 30
- nFO inn. layer > 60
- nFO inn. layer > 90

Domenico Elia
### ALICE trigger parameters

<table>
<thead>
<tr>
<th></th>
<th>Level 0</th>
<th>Level 1</th>
<th>Level 2</th>
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</thead>
<tbody>
<tr>
<td>Last trigger input at CTP (μs)</td>
<td>0.8</td>
<td>6.1</td>
<td>87.6</td>
</tr>
<tr>
<td>Trigger output at CTP (μs)</td>
<td>0.9</td>
<td>6.2</td>
<td>87.7</td>
</tr>
<tr>
<td>Trigger input at detectors (μs)</td>
<td>1.2</td>
<td>6.5</td>
<td></td>
</tr>
<tr>
<td>Rate (Hz)</td>
<td>1000</td>
<td>40-800</td>
<td></td>
</tr>
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</table>
Angular resolution

\[ \Delta \theta = 26 \text{ mrad} = 1.5^\circ \quad |\Delta \eta| = 0.10 \]
\[ \eta = 2.0 \]

\[ \Delta \theta = 192 \text{ mrad} = 11^\circ \quad |\Delta \eta| = 0.19 \]

\[ \Delta \theta = 42 \text{ mrad} = 2.4^\circ \quad |\Delta \eta| = 0.09 \]

\[ \eta = 1.41 \]
Radiation effects

- Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances, iROC report, 2004

- Failure In Time (FIT) := errors in 10^9 hours with neutron flux of 14 cm^{-2} hr^{-1}
  - SEFI: Single Event Functional Interrupt
  - SEU: Single Event Upset (configuration)

- Neutron max fluence: 2.0 \times 10^8 cm^{-2} (10 y)
  - Morsch, Pastircak, Radiation in ALICE Detectors and Electronic Racks, ALICE-INT-2002-28

- Central Trigger Processor using SRAM based ALTERA Cyclone EP1C20

<table>
<thead>
<tr>
<th>FIT</th>
<th>SEFI</th>
<th>SEU</th>
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<tbody>
<tr>
<td>Altera EP1C20</td>
<td>453</td>
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<tr>
<td>Xilinx XC3S1000</td>
<td>320</td>
<td>1240</td>
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<tr>
<td>Xilinx XC2V3000</td>
<td>1150</td>
<td>8680</td>
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<table>
<thead>
<tr>
<th>Errors in 10 years</th>
<th>SEFI</th>
<th>SEU</th>
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<tbody>
<tr>
<td>Altera EP1C20</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Xilinx XC3S1000</td>
<td>5</td>
<td>18</td>
</tr>
<tr>
<td>Xilinx XC2V3000</td>
<td>17</td>
<td>124</td>
</tr>
</tbody>
</table>
Developments

- Advanced 12-channel parallel optical fiber receiver modules
  - Devices customized by Zarlink
  - 1310 nm, single mode
  - Experimentally validated
  - Space saving

- G-Link protocol deserializers on programmable hardware
  - Implemented and tested with advanced FPGAs
  - Not fulfilling latency requirement

- Dedicated deserializer ASIC
Latencies of processes

- Serialization, deserialization, processing latency
- Hardware emulator of the Silicon Pixel Detector as data source
- Overall latency: 800 ns
Control and configuration

- Status monitoring and control on ALICE DDL communication layer
- User selection of different processing algorithms
  - Download of configuration file into local SRAM memory
  - Reconfiguration of the processing FPGA
- Interfaces to several ALICE subsystems

Experiment Control

Silicon Pixel Detector Control

Central Trigger Processor Control

Pixel Trigger servers (control room)

DDL

User selection of different processing algorithms

- Download of configuration file into local SRAM memory
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Interfaces to several ALICE subsystems