

The Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector: implementation, testing and commissioning

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Abstract

The ALICE Silicon Pixel Detector transmits 1200 Fast-OR signals every 100 ns on 120 optical readout channels. They indicate the presence of at least one hit in the pixel matrix of each readout chip. The ALICE Level 0 Pixel Trigger System extracts them, processes them and delivers an input signal to the Central Trigger Processor for the first level trigger decision within a latency of 800 ns. This paper describes tests and measurements made on the system during the qualification and commissioning phases. These included Bit Error Rate tests on the Fast-OR data path, the measurement of the overall process latency and the recording of calibration data with cosmic rays. The first results of the operation of the Pixel Trigger System with the SPD detector in the ALICE experiment are also presented.

I. INTRODUCTION

The Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment at the LHC [1][2][3]. The SPD is a double layer barrel pixel detector [1][4], constituted of 120 modules (half staves). The half staves are staggered on a carbon fiber support structure, 40 on the inner layer ($r = 39$ mm) and 80 in the outer one ($r = 76$ mm). Each half staff includes two 200 μm thick silicon pixel sensors with 160×256 pixels of $425 \times 50 \mu\text{m}^2$. The two sensors are bump bonded to 10 front end pixel chips operating at $1/4$ of the LHC bunch crossing frequency, i. e. at ~ 10 MHz. Each of the 1200 SPD readout chips has a prompt Fast-OR output. The Fast-OR signal is asserted within 300 ns from a particle hit in any of the 32×256 (8192) pixels read out by the chip. The readout chips of each half staff are connected to a Multi Chip Module (MCM) [5].

The MCM includes four custom ASICs and one custom optical transceiver module. The MCM implements the communication interface to the off detector electronics in the control room and provides bias and control signals for the pixel chips. Two optical links are used to transmit the LHC 40.0786 MHz bunch crossing clock and serial control to the MCM. The MCM uses a third optical fiber to transmit information to the readout electronics in the control room and to the Pixel Trigger System in the ALICE cavern. All optical fibers are single mode and the operating wavelength is 1.3 μm . The MCM transmits status and control feedback signals and the ten sampled Fast-OR bits every 100 ns. The pixel hit data are transmitted only during a readout sequence. The readout and transmission of hit data are initiated and controlled by the MCM upon receiving a positive trigger decision via the serial control.

The Fast-OR data are used in the ALICE first level (Level 0)

trigger decision to improve background rejection in pp interactions and event selection in heavy ions runs. Various trigger algorithms based on topology or multiplicity of Fast-OR signals have been investigated [6]. All of them can be implemented as boolean logic functions of the 1200 SPD Fast-OR signals on field programmable devices.

The Pixel Trigger System (PIT) extracts the Fast-OR signals from the 120 SPD output data links and process the selected pixel trigger algorithm. It has to provide the result to the ALICE Central Trigger Processor (CTP) where it contributes to the Level 0 decision. The total time from the particle collision to the transmission of the result to the CTP should be less than 800 ns. The system is independent from the SPD readout electronics located in the control room and is located in the experimental cavern, where a limited space of one 9U crate is available for the electronics boards. The design, earlier developments and implementation details of the Pixel Trigger System have been previously published [7][8][9]. In the following we review the system as it is presently installed in ALICE. Laboratory integration tests and measurements made before the installation are presented in detail. Finally, we discuss the commissioning and the first operation of the Pixel Trigger System with the SPD in the ALICE experiment.

II. THE ALICE PIXEL TRIGGER SYSTEM

Fig. 1 shows a diagram of the connections between the SPD, the readout electronics, the Pixel Trigger System and the CTP. The main clock and the trigger commands are distributed to all subsystems by the CTP via the local Timing Trigger and Control (TTC) distribution network [10]. The SPD readout electronics is located in a control room ~ 100 m far from the detector. The CTP and the PIT crates are in the experimental cavern, close to the ALICE apparatus. The 3×120 clock, serial control and data fibers are routed separately for the modules on the two symmetric halves (side A and side C) in which the SPD is divided by the plane orthogonal to the detector axis and passing by its center. The readout data fibers coming from the detector are connected to 120 passive optical splitters. One of the output branches forwards data to the readout electronics while the second one is connected to the Pixel Trigger System. The ten outputs of the PIT are connected to dedicated CTP inputs.

Following a collision in a bunch crossing, particles traverse the SPD and Fast-OR signals are transmitted to the PIT. The results of the Fast-OR processing are transmitted to the CTP for the trigger decision that is based on inputs from all the trigger detectors. In case of a positive decision a trigger command is transmitted to the readout electronics by the TTC link. A read-

out sequence is then initiated by the MCM. The pixel hit data are transmitted to the readout electronics on the data fibers.

The SPD on-detector electronics takes 350 ns to transmit the Fast-OR signals, the propagation delay on the fibers from the detector to the PIT is ~ 200 ns and the transmission of the results to the CTP requires 25 ns. Because of the 800 ns constraint on overall latency, only 225 ns remain to the PIT electronics to extract and process the Fast-OR signals.

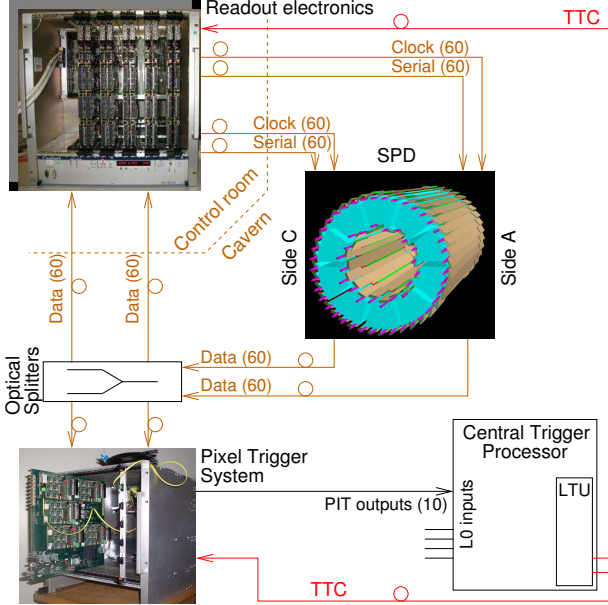


Figure 1: Simplified diagram of the control, readout and trigger connections between the Silicon Pixel Detector, the SPD readout electronics, the Pixel Trigger System and the Central Trigger Processor in the ALICE experiment.

The Pixel Trigger System electronics is constituted by ten optical receiver boards (OPTIN) and one processing motherboard (BRAIN). The ten OPTIN boards deserialize the received data and extract the 1200 Fast-OR signals from the data flow. The OPTIN board contains an FPGA¹ and is equipped with a custom 12-channel parallel optical fiber receiver module and twelve G-Link deserializer ASICs [11]. Each OPTIN board receives data fibers from 12 SPD half staves. The components are densely arranged on a 160×84 mm² 12-layer printed circuit board. The BRAIN electronic board (400×360 mm², 9U) hosts the Processing FPGA², a device with 960 user I/O pins and 110592 logic cells. The ten OPTIN boards connect as mezzanine boards on the BRAIN, five on each side. Fig. 2 shows a photograph of the BRAIN board with OPTIN boards plugged on two of the five locations on the visible side of the BRAIN. Fig. 3 shows the Pixel Trigger electronics partially inserted into the hosting crate.

The 1200 Fast-OR signals extracted every 100 ns in the OPTINs are transferred to the Processing FPGA on 600 striplines using $2 \times$ time multiplexing (Double Data Rate transfer). The Digital Source Impedance control feature of the FPGAs is used to impedance match these lines. Several processing algorithms can be implemented in parallel in the Processing

FPGA and the maximum number is limited only by their complexity and by the available logic resources. Ten LVDS lines are available to transmit the results to the CTP, limiting to ten the number of pixel algorithms that can be used in parallel by ALICE. All algorithms implemented in the firmware up to now complete in one clock cycle.

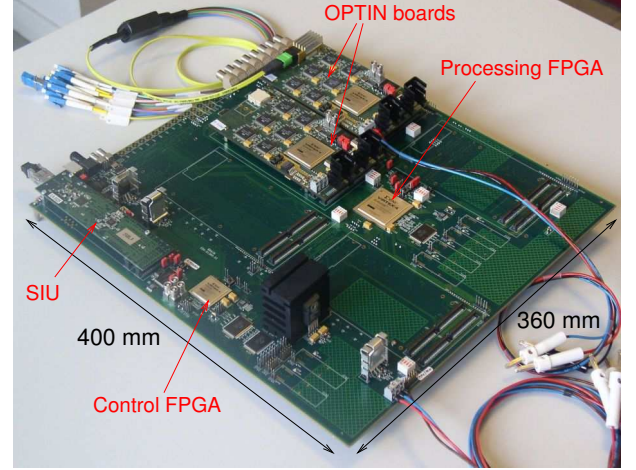


Figure 2: A photograph of the BRAIN board. The Processing and Control FPGA are indicated. OPTIN boards are connected on two of the five visible locations. Five other locations are on the other side of the BRAIN board. The ALICE DDL-SIU mezzanine board is also visible.

The Control FPGA on the BRAIN board provides the control and communication functionalities. It manages a 32-bit shared bus that allows intercommunication between all the FPGA devices of the system. The custom bus protocol is a simplified version of the PCI protocol. The Control FPGA acts as the bus master, while the OPTIN boards FPGAs and the Processing FPGA are the target devices answering to the read and write transactions governed by the Control FPGA. Parity checking and transaction acknowledgement are performed in the hardware.

The Pixel Trigger System is remotely controlled by a custom software driver executing on a dedicated computer [12]. The ALICE Detector Data Link (DDL) is used as communication layer between the computer and the electronics [13]. The DDL Source Interface Unit (SIU) front-end board is the DDL interface on the BRAIN board. It is connected to the Control FPGA that acts as a bridge between the the DDL link and the board shared bus. The driver uses the hardware functionalities to detect any failure of the parity checks or any mismatch between the requested and the actual length of the transferred data blocks. The state machines in the hardware recover safely in case of errors and return to an idle state, ready for subsequent read or write accesses.

The system gets the main clock from the TTC by the TTCrx and QPLL chips. USB and JTAG interfaces provide local access for hardware testing and debugging. Auxiliary high speed serial lines and optical transceivers are available for future upgrades requiring high bandwidth communication with the control room.

¹Xilinx Virtex 4 LX60.

²Xilinx Virtex 4 LX100.

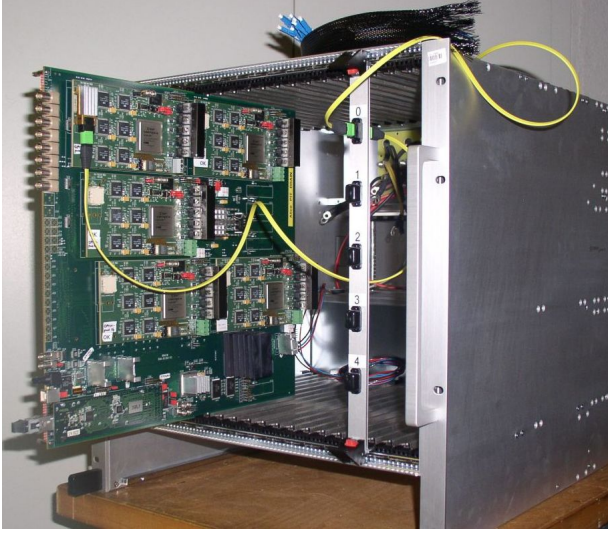


Figure 3: The Pixel Trigger System crate. The electronics board are partially extracted from the crate. Five OPTIN boards are connected on the visible side of the BRAIN board. One of the ten optical fiber fan-in cables and one optical patch panel are also shown.

III. LABORATORY TESTS AND MEASUREMENTS

A. Electrical tests and clock distribution

The current consumptions of the boards are given in Table 1. Power demand was lower than the design expectations because the FPGA operating currents had been overestimated. The total power of 200 W is a small fraction of the power that can be safely dissipated in a cooled 9U electronic crate. A peak temperature of 45 °C was measured on the boards. According to the thermal model used in the design phase, the voltage regulators of the OPTIN boards were the components reaching the highest temperature and therefore they were equipped with large aluminium heat sinks. Considering the temperature measured on the heat sinks during operation and the junction-ambient thermal conductivity, the junction temperature of the voltage regulators resulted of 72 °C, safely below the maximum rating of 125 °C for these devices.

Table 1: Current absorptions from the two supply voltages (5 V and 3.3 V) and power needs of the OPTIN board, BRAIN board and full Pixel Trigger System.

	I_{5V} [A]	$I_{3.3V}$ [A]	P [W]
OPTIN	2.8	0.375	15.3
BRAIN	7.9	1.6	45
Total PIT	36.1	5.4	198

Complete JTAG interconnect tests were performed on all the boards to detect missing connections or short circuits. Up to three JTAG chains were simultaneously driven and read during these tests, with the OPTIN board under test connected to one of the slots on the BRAIN. All the OPTIN boards and all the slots were tested in turn. The signal lines that are not accessible by JTAG were stimulated by driving circuitry inside the FPGAs and tested with a scope. The signal propagation delay measured on the boards was of 6.9 ns/m, slightly lower than the

value of 7.8 ns/m estimated in the design phase. The phases of the clock signals of all the OPTIN FPGAs relatively to those of the Processing and Control FPGAs were measured. The resulting distribution showed an average shift of ~ 3 ns and a RMS spread of ~ 1 ns. Subsequently the internal clocks of the Processing and Control FPGAs were phase adjusted to compensate for the average shift and their transitions moved to the middle of the distribution of those of the OPTIN FPGAs.

B. Fast-OR data path Bit Error Rate tests

Bit Error Rate (BER) tests were done on the full data path of Fast-OR signals to qualify the integrity of the communication and processing chain. In general BER tests [14] are based on counting bit mismatches between transmitted data and data that are extracted at the receiver end of the communication channel under test. The number of mismatches counted during a transmission run allows to evaluate boundaries for Bit Error Rate, i. e. the probability that the bit received at the output is different than the transmitted one. Tests might require the transmission of very long sequences to gather sufficient statistics in a normal case with a very low error probability. An upper boundary for the BER can be determined even in case no bit mismatches are observed.

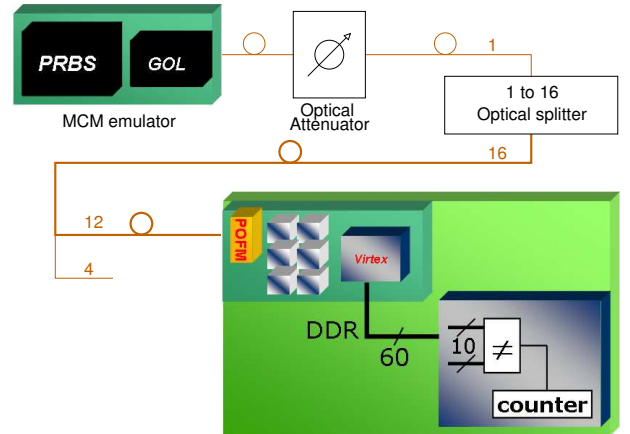


Figure 4: The experimental setup used for the Fast-OR Bit Error Rate tests.

The setup used for our tests is shown schematically in Fig. 4. A hardware emulator of one MCM was used as data source. This included a Pseudo Random Bit Sequence (PRBS) generator, a serializer GOL chip [15] and a laser transmitter. The optical signal was attenuated to operate in limiting conditions and fed into a 1×16 optical splitter. One OPTIN board was connected to one of the slots of the BRAIN. Twelve of the sixteen fibers were connected to the OPTIN using the same optical fan-in cables that were later installed in ALICE. The twelve channels of the OPTIN were therefore receiving exactly the same optical signal. The optical power at the output of each fiber was 18.5 dBm with 50% Optical Modulation Amplitude, only 0.5 dBm above the minimum operating power required by the optical receiver module on the OPTIN.

The Fast-OR signals were extracted and transferred to the Processing FPGA. A set of bit comparators were implemented in the Processing FPGA and they compared the data words re-

ceived on pairs of adjacent channels. With this approach it was not necessary to reconstruct the transmitted word at the receiver end. The test was repeated on all the OPTIN boards in turn and connecting them to different slots. Table 2 summarizes the results of the tests. In all cases no word errors and therefore no bit errors were observed. In a typical run the Bit Error Rate was less than 8.1×10^{-13} . In two longer tests this figure improved by one order of magnitude.

Table 2: Fast-OR Bit Error Rate tests results. The typical test was made on eight OPTIN boards and lasted 1.5 hours. The entry labeled with Max refers to longer tests made on two OPTIN boards. BER upper bounds are evaluated at 99 % confidence level.

	Hours	N_{bits}	Errors	BER
Typical	1.5	5.7×10^{12}	0	$< 8.1 \times 10^{-13}$
Max	17.8	7.7×10^{13}	0	$< 6 \times 10^{-14}$

Another test was realized with ten OPTIN boards simultaneously connected to the BRAIN board. In this case the Fast-OR data were generated by internal sequencers implemented in the OPTIN FPGAs. Pseudo random bit patterns were generated in all the 120 channels of the OPTINs and simultaneously transmitted to the Processing FPGA on the 600 dedicated lines. As in the previous case the bit comparators in the Processing FPGA were used to detect and count possible bit mismatches between the words received on pairs of channels. The longest test lasted 15 h with 6.48×10^{14} bits transmitted and received. No bit errors were observed, implying that the Bit Error Rate of the transmission between the ten OPTIN boards and the Processing FPGA is less than 7.1×10^{-15} with 99% confidence level. This test ensured that no degradation of the Fast-OR data transmission is introduced by coupling noise when the 600 signal lines densely routed in the region of the Processing FPGA are simultaneously driven.

C. Control Bus Bit Error Rate tests

Dedicated tests were performed to qualify the custom control architecture. The software driver wrote, read back and checked blocks of random data from all the target devices on the Pixel Trigger System bus. All the produced OPTIN boards were tested in turn. A typical test lasted ~ 15 min and more than 6×10^8 bits were transferred during these runs. For two boards the tests lasted about 12 h and a total of 3×10^{10} bits were exchanged in these cases. No bit errors were detected in all the trials. These tests qualified the reliability and robustness of the full control chain including the Alice DDL interfaces, the optical link, the communication interface blocks in the Control FPGAs and in the other eleven FPGAs of the system as well as the custom protocol of the shared bus and the Pixel Trigger System driver software.

D. Latency measurement

The integration of the SPD and of the readout electronics before their installation in the experimental cavern were done in a laboratory setup almost identical to the system installed in the ALICE experiment. This setup is currently used with spare SPD modules for the refinement of calibration procedures and

for the development of hardware and software functionalities. It was also used to measure the Pixel Trigger System latency.

The *test pulse* input on the SPD pixel chip was activated to inject charge into the front end amplifier of the readout cells. This is equivalent to the passage of a particle across the sensor and activates the Fast-OR output of the chip upon the second following rising edge of the ~ 10 MHz clock. Due to synchronization with the clock, the Fast-OR output activates upon the same clock edge no matter when the injection precisely happens within one clock cycle interval of 100 ns. In our setup the test pulse was activated in correspondence of a clock falling edge, that is in the middle of the intrinsic uncertainty interval. A latency of 733 ns was measured between the charge injection and the activation of the Pixel Trigger output.

Signal connections present in the ALICE system but not included in the laboratory setup require 41 ns of propagation delay. Further uncertainty (± 12.5 ns) is due to the phase relationship of the 120 MCM clocks with respect to the bunch crossing clock and to the PIT receiver clocks. Phase tuning of the SPD and PIT system clocks during LHC operation with particle collisions is required to minimize the previous contribution to the latency. Considering the intrinsic time accuracy of 100 ns, it follows that the latency of the Pixel Trigger System in the ALICE experiment can range between ~ 736 ns and ~ 836 ns in the worst case and between ~ 712 ns and ~ 812 ns in the best case.

IV. COMMISSIONING IN ALICE

A. Synchronization and optical fibers routing

The ~ 10 MHz clock signals of the readout chips are generated on the MCMs by $4\times$ division of the received 40.0786 MHz clock. The MCM keeps the phase of the slow clock aligned to the serial control frames received from the readout electronics. The phases of the two clocks should be, in the ideal case, equal across all the half staves so that the Fast-OR signals are activated by collision events belonging to the same set of four consecutive bunch crossings.

To synchronize both clocks across the modules it is necessary that the ~ 40 MHz clocks and the serial messages are not only synchronously transmitted from the control room electronics but also synchronously received by all the half staves. For this purpose the lengths of the relevant fiber links were equalized. The measurements of fiber lengths are listed in Table 3. Assuming that the refractive index of SiO_2 at $1.3 \mu\text{m}$ is 1.447, the propagation latencies differ by 1.45 ns at most. The relative phases of a subset of clock signals were measured at the transmitter end of the clock links and the RMS spread was of ~ 0.475 ns. It follows that the rising transitions of the ~ 40 MHz clocks in the SPD modules are confined in a 4.3 ns time interval, that is about 17% of the clock period.

In order to synchronize the transmission phases of the 120 serial control streams from which the alignment of the divided clocks depends, a dedicated broadcast command was implemented on the local TTC system. This allows the simultaneous transmission of the synchronization command to all the 120 serial control channels. The command is issued during the system configuration phase before each data taking run.

Table 3: Fiber lengths of the SPD detector. Data fiber lengths refer to the section between the SPD and the optical splitter. The uncertainty represents the minimum and maximum lengths.

Link	SPD Side	
	A	C
Clk	107.6 ± 0.15 m	
Serial	107.6 ± 0.15 m	
Data	38.5 ± 0.2 m	36.6 ± 0.2 m

The lengths of the data fibers between the SPD and the PIT were minimized to reduce the Fast-OR propagation delay and equalized to guarantee synchronous deserialization of the data stream in the PIT.

B. Data frame synchronization

The MCM transmits Fast-OR, feedback and hit data using a custom protocol [16]. Four transmission frames repeat continuously as shown in Fig. 5. The first and second frames contain the ten Fast-OR bits of the half stave and feedback signals respectively. The third and fourth frame contain the pixel hit data during a readout sequence. The clock synchronization across the 120 half staves guarantees that the frame sequences are transmitted synchronously. However, they can be decoded in different clock cycles in the Pixel Trigger deserializer stages for two reasons. The first one is that the transmissions of modules with longer data fibers suffer a longer propagation delay. The second one is that the clock phases of the deserializers can be out of optimal alignment with respect to the clock reconstructed from the received signal. The latter situation can imply a further delay of one clock period added automatically by the OPTIN receiver ASICs and increasing the overall latency.

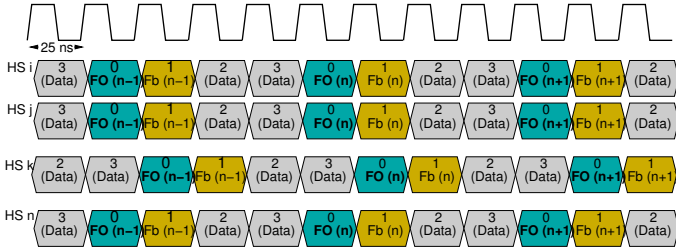


Figure 5: Timing diagram of the MCM output transmission frames. The LHC bunch crossing clock is plotted for reference. In this example the sequence of the k -th half stave is deserialized one clock period later than those of other three half staves.

The Fast-OR packets related to the same ~ 100 ns time interval must be time aligned to be processed simultaneously. A time stamping functionality was implemented in the FPGAs for this purpose. Trigger commands are received simultaneously by all the SPD modules. The MCMs immediately acknowledge them retransmitting a dedicated word in the next feedback frame of their output stream. The time stamping functionality determines for each channel the clock cycle during which the trigger feedback signal is received. The relative alignment of the deserialized data streams is therefore measured by the circuit itself. The received sequences are then delayed accordingly to the measurements and aligned to the last arriving frame. The

entire procedure is fully automated by the driver software.

After the installation in ALICE the phase of the Pixel Trigger System clock was fine tuned adjusting the length of the TTC fiber feeding the clock to the system and using the time stamping functionality previously described. As a result the received sequences were aligned across the two groups of sixty modules of each detector side. The sequences of the modules on side C were decoded one clock period earlier than those of side A, due to the different fiber lengths on the two sides (Table 3). A delay of one clock period was added to the sixty channels of side C, making the system ready for operation.

V. FIRST OPERATION IN ALICE

A cosmic ray coincidence logic was programmed in the Pixel Trigger Processing FPGA. The PIT output activated on the simultaneous presence of at least two active Fast-OR signals, one in the outer layer of the upper half barrel and one in the outer layer of the bottom half. Fig. 6 shows the SPD online monitoring display with a cosmic ray event. The trigger rate ranged from 0.09 Hz to 0.12 Hz depending on the number of active SPD modules. This was well in agreement with the results of a Monte Carlo simulation of the detector including the measured muon flux in the ALICE cavern. Cross checks of the recorded data showed that more than 99.5% of the events presented the cluster distribution required by the trigger algorithm, with at least two clusters in the detector outer layer.

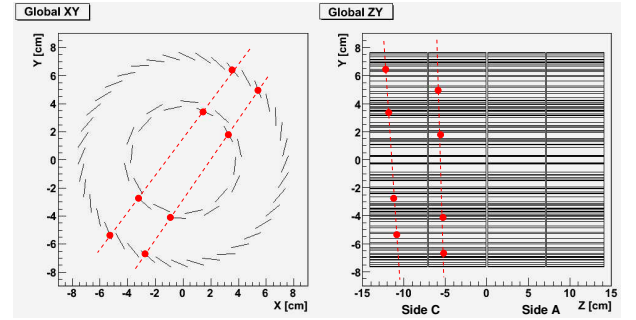


Figure 6: Cosmic ray event recorded by the SPD triggered by the Pixel Trigger System. Two muon tracks are visible, each generating four hits in the two layers.

The cosmic trigger signal was extensively used to readout the SPD detector alone or together with other ALICE detectors. The recorded cosmic ray data proved extremely useful for the commissioning of the SPD, of the Inner Tracking System combined with the TPC and for the tuning of the detectors geometry in the offline reconstruction software. More than 65000 events with at least 3 hits clusters in the SPD and more than 35000 with at least 4 were recorded to date, as well as several events with showers developing in the TPC and traversing the SPD with high occupancy.

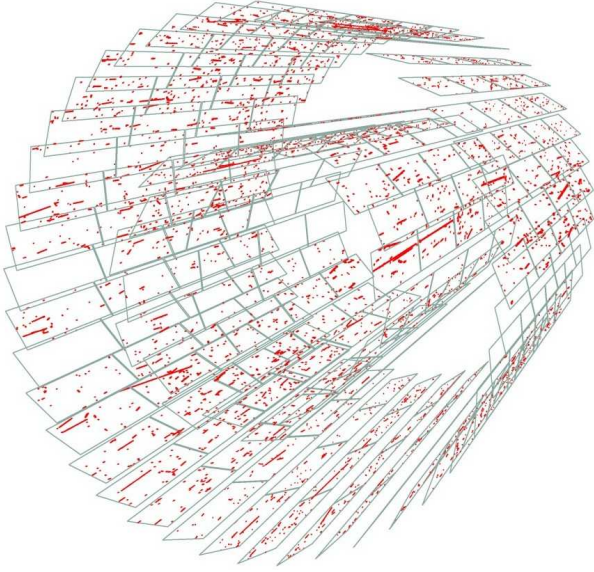


Figure 7: Event display of one of the events recorded during LHC beam injection tests. This three dimensional rendering shows the SPD silicon sensors and the recorded pixel hits.

In August 2008 beam injection tests were made at the LHC, in the collider section preceding the ALICE cavern. The beam was dumped before reaching the cavern. The SPD was operated together with the Pixel Trigger System and various large occupancy events were recorded. Fig. 7 shows an example. The recorded events contain long straight tracks developing parallel to the beam axis for several centimeters in the $200\text{ }\mu\text{m}$ thin active volume of the silicon sensors. These were attributed to the muons originating in the beam dump. Some tracks in these events cross the gaps between adjacent sensors and adjacent readout chips. Finally, beam-gas interaction events were recorded during further LHC tests when the first beams were continuously circulated for several minutes in the LHC on 11 September 2008.

VI. CONCLUSIONS

The ALICE Pixel Trigger System allows to include the prompt Fast-OR outputs of the ALICE Silicon Pixel Detector in the first level (Level 0) trigger decision of the experiment. The Pixel Trigger System is a very compact electronic system with a large, parallel data flow architecture. It includes original developments and satisfies challenging requirements at the board level and at the system level. The system has been thoroughly qualified after production with several laboratory tests that were described in this paper. The fulfillment of the stringent constraint on the overall process latency has been experimentally verified as well as the reliability of the system operation. The Pixel Trigger System has been fully installed, commissioned and already operated in the ALICE experiment. The SPD equipped with the Pixel Trigger provided a reliable and extremely useful cosmic trigger during the commissioning of the ALICE detectors. Events related to beam dumping or beam-gas interactions were recorded during the first LHC injection and beam circulation tests. ALICE is the only LHC experiment that will include the vertex detector in the first trigger decision from startup.

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