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The Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector: implementation, testing and commissioning.

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The ALICE Silicon Pixel Detector transmits 1200 Fast-OR signals every 100 ns using its 120 optical readout channels. They indicate the presence of at least one hit in the pixel matrix of each readout chip. The ALICE Level 0 Pixel Trigger system extracts, processes them and delivers an input signal to the Central Trigger processor for the first level trigger decision within a latency of 800 ns.

This contribution will describe the tests and measurements made during the qualification and commissioning phases of the system.
These included Bit Error Rate tests on the Fast-OR data path, the measurement of the overall process latency and the recording of calibration data with cosmic rays.
Furthermore, the first results of the operation of the Pixel Trigger system with the SPD detector in the ALICE experiment will be presented.

Summary

The ALICE Silicon Pixel Detector (SPD) data stream includes 1200 digital signals (Fast-OR) promptly activated on the presence of at least one pixel hit in each of the detector readout chips. This information is used in the ALICE first level (Level 0) trigger decision to improve background rejection in pp interactions and event selection in heavy ions runs. Various trigger algorithms based on topology or multiplicity of Fast-OR signals have been investigated.
All of them can be implemented as boolean logic functions of the 1200 SPD Fast-OR signals on Field Programmable devices.

The Pixel Trigger system receives the entire SPD data stream on 120 optical input channels. It extracts the Fast-OR signals, processes them and delivers the result to the ALICE Central Trigger Processor for the Level 0 trigger decision. The design and the development of the Pixel Trigger system have been previously published. The Pixel Trigger system is now installed in the ALICE experiment.

This contribution will describe a set of tests and measurements realized on the Pixel Trigger system during its qualification and commissioning. Bit Error Rate measurements were made on the complete Fast-OR data path from the detector to the system processing unit.
Several tests were done on the system operated together with the SPD detector.
These allowed the measurement of the overall processing latency and the acquisition of cosmic ray data for calibration purposes, using the Pixel Trigger system to self-trigger the SPD on its Fast-OR outputs.
The results of the first months of operation of the Pixel Trigger system with the SPD detector in the ALICE experiment will be presented.

The output of the Fast-OR processing algorithm must be provided to the Central Trigger Processor within 800 ns from the interaction. A large fraction of this time is needed for the generation, serialization and transmission of the Fast-OR signals. Only 225 ns

are available for the extraction and processing of the signals in the Pixel Trigger system.

The Pixel Trigger system is based on ten optical receiver boards (OPTIN) and one processing board (BRAIN). All boards are equipped with field programmable devices (FPGA). The ten OPTIN boards connect as mezzanine boards on the processing board.

The 1200 Fast-OR signals are extracted in the OPTIN boards, time multiplexed and transferred to the processing board. The processing FPGA processes them and transmits the results to the Central Trigger Processor. Different algorithms can be implemented and executed in parallel.

A secondary FPGA on the BRAIN board communicates with all the processing devices of the Pixel Trigger system and interfaces them to the control computers by the ALICE optical Detector Data Link (DDL).

The Pixel Trigger system architecture supports various user selectable algorithms. The selection of a different algorithm is allowed in between data taking runs and might require the reconfiguration of the processing device. This procedure is executed remotely via the control FPGA, capable of reconfiguring the processing FPGA by its JTAG interface.

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