

The ABCN front-end chip for ATLAS Inner Detector Upgrade

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Abstract

We present the design of the ABCN front-end chip implemented in a CMOS 0.25 μm technology and optimized for short silicon strip detectors as foreseen for the ATLAS Silicon Tracker Upgrade.

A primary aim of this project is to develop an ASIC with full functionality required for readout of short silicon strips in the SLHC environment in a cost-effective and proven technology. Design efforts have been focused on optimizing noise and power performance of the front-end circuit for low detector capacitance, minimizing power consumption in digital blocks and on compatibility with new power distribution schemes being developed for future tracker detectors.

The architecture of the chip as well as critical and novel design aspects are discussed in the paper. The ABCN ASIC will serve as a basic test vehicle in an extensive program on development of sensors and modules for the ATLAS Silicon Tracker Upgrade.

I. INTRODUCTION

A primary challenge of tracking detectors being developed for the SLHC environment is a high occupancy, which affects directly the granularity of sensors and the number of electronic channels, to be about 10 times higher compared to the present SCT. As a result, power consumption in the readout ASICs is one of the most critical issues on top of usual requirements concerning noise and radiation resistance. These requirements have to be considered taking into account present and expected trends in development of industrial CMOS processes. In order to address all these aspects an R&D proposal has been initiated to develop a new ASIC for the ATLAS Silicon Tracker Upgrade [1].

Because of increased number of electronic channels in the Silicon Tracker Upgrade and the constraints on the space available for the power cables and other services an efficient power distribution scheme appears as one of the critical problems to be worked out. A scheme like the one employed in the present ATLAS SCT detector with each detector module being powered by an individual set of cables is not feasible at all. Various schemes for power distribution, like serial powering of modules or DC-DC step-down converters on the detector, are under investigation in the frame of another R&D project [2]. Thus, the new ASIC architecture has to be compatible with whatever power distribution scheme will be adopted in the future.

The basic concept and architecture of the ABCN follows the architecture of the ABCD3T ASIC implemented in BiCMOS DMILL technology and used in the present ATLAS SCT detector [3]. The basic features of this architecture are: binary front-end, pipeline for first level trigger latency, derandomizing buffer, zero suppression and data compression logic.

A new front-end circuit is based on the prototype developed earlier in a CMOS 0.25 μm technology [4] but it has been now optimized for readout of short strips. A primary goal was to reduce the power consumption while maintaining the required noise and timing performance of the circuit.

The architecture of the readout circuitry has to address two other aspects related to a new concept of the basic detector module. A new scheme for readout electronics assumes two additional stages of data concentration and multiplexing on the detector between the front-end ASICs and the off-detector electronics [5].

The ABCN prototype ASIC has been designed and manufactured in the IBM CMOS 0.25 μm technology, however, this is considered as an intermediate step towards implementation of this readout architecture in a more advanced process for the final design. Reasons for implementing the present prototype in the 0.25 μm technology were partially economical and partially technical concerning availability of a design kit allowing for using advanced design techniques for the digital part of the ABCN. Nevertheless, all critical aspects of the new architecture have been implemented in the present prototype and the ASIC will be used as a basic test vehicle in the program to develop detector modules for the ATLAS Silicon Tracker Upgrade.

II. ASIC ARCHITECTURE

A block diagram of the ABCN chip is shown in Figure 1. The ABCN ASIC follows the concept of binary readout of silicon strip detectors as implemented in ABCD3T ASIC [3]. It comprises 128 channels of preamplifier/shaper/comparator circuits with two memory banks, one used as a pipeline for the trigger latency and another one used as a derandomizing buffer. The front-end has been optimized for 5 pF detector capacitance (2.5 cm long silicon strip detector) and it is compatible with either detector signal polarity. The shaper is designed for 25 ns peaking time providing 75 ns double pulse resolution and comparator time walk less than 15 ns compatible with 25 ns BCO clock.

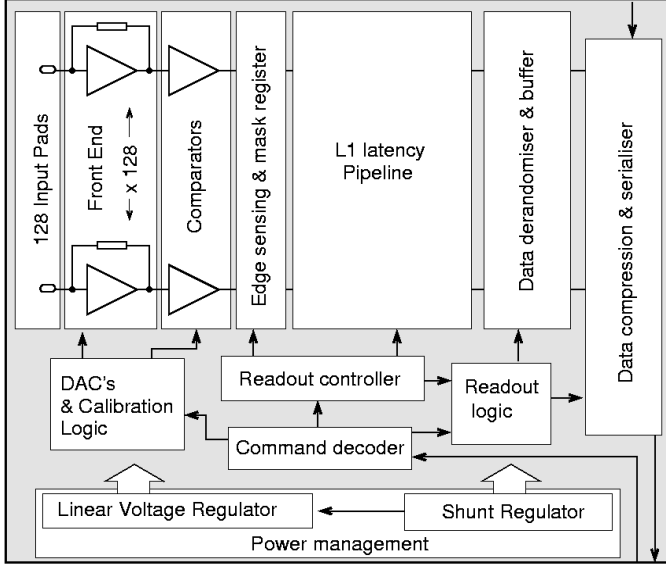


Figure 1: The block diagram of the ABCN chip

The power management block comprises two alternative prototype circuits of the shunt regulators needed if a scheme with serial powering module will be adopted, and a linear regulator, which delivers a clean and stable supply voltage for the analog front-end circuits. This linear regulator will be particularly important if a power distribution scheme with DC-DC step-down converters on the detector is adopted. Therefore, the design of the regulator is optimized for high rejection ratio so that it can operate with a noisy input power supply.

Since the ABCN chip will be used for the ATLAS Silicon Tracker Upgrade module development program, one of the basic requirements is the tolerance to ionizing radiation. For the IBM 0.25 μm process used, radiation tolerance up to a level of 100 MRad TID has been already demonstrated, provided that all NMOS devices are in enclosed geometry layout. In order to improve the immunity of the chip to Single Event Upsets (SEU) all configuration registers and the fast

command decoder are designed with triple vote logic and auto correction. The SEU event flag can be read out from the STATUS register.

A. Design methodology

The analog blocks including the front-end circuits, Digital to Analog Converters, Calibration Circuit as well as RAM memory banks have been designed using full custom techniques, both for the schematic and the layout. After positive LVS verification, the post-extracted simulations were performed in order to check possible degradation of performance due to parasitic capacitances.

A significant reduction of the overall power consumption of the front-end part has been achieved by reducing the bias currents in the buffers, shaper and discriminator stages, which undesirably pronounced the influence of the parasitic capacitances on the overall shaping function of the front-end. The final adjustment of capacitances in the filtering stages was done with Spice simulations, taking into account all parasitic capacitances extracted from the layout of the chip.

The digital part was fully described in the Verilog HDL except pipeline and derandomizing memories, which were used as macro cells with well defined digital description. Verilog code was synthesized first time with the default timing library wireload model. In the following iterations the wireload model generated in the last step of the place and route (P&R) procedure was used. The scan chain was added to improve testability of the chip.

The P&R starting from the Verilog gate netlist was done using the First Encounter tool. The floorplan definition was highly constrained by the design and area of the memory blocks (they consume significant amount of the total area of the digital part). After each consecutive step of the P&R, clock tree synthesis (CTS), routing timing verification and set-up/hold optimization was performed. There are two independent clock trees, one slower for control and second one faster for data readout. Also the reset signal tree was built in the CTS phase.

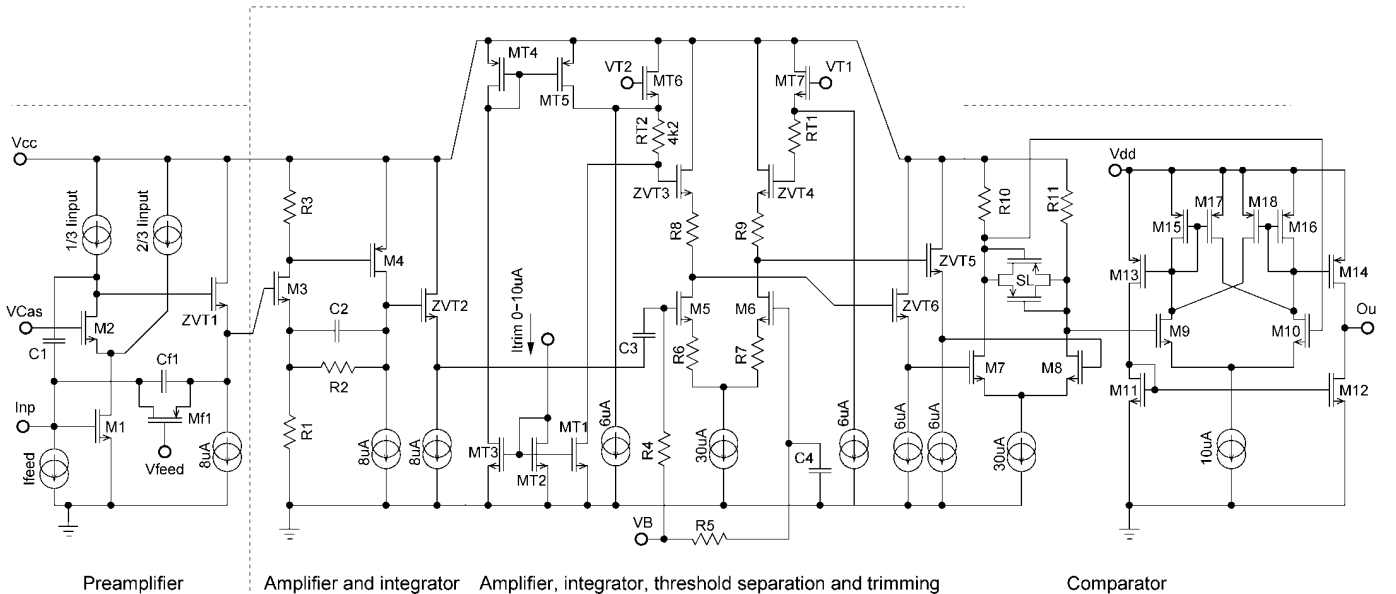


Figure 2: The schematic diagram of the preamplifier, shaper and comparator stage.

After routing of connections the physical verification was preformed. In principle the routing procedure should comply with the DRC rules automatically, however, the rules get sometimes violated due to e.g. routing problems. If such errors could not be corrected manually next run of P&R sequence with different parameters or a different floorplan definition was performed. The procedure was repeated several times until satisfactory performance was achieved.

Generation of the output files was the last step of the P&R procedure. The Verilog gate netlist changed during optimizations and CTS with SDF including delays were used for post-P&R Verilog simulations. The GDS file describing the layout of the digital part and wire load models were then used for next synthesis iteration.

The top level was assembled in semi-automatic way with the First Encounter used for routing and pad ring definition. The final DRC and LVS verification was performed on the complete design.

B. Front-End design

The schematic diagram of the front-end amplifier and comparator is shown in Figure 2. The preamplifier stage is built as a classical cascode stage with NMOS input transistor biased nominally with 140 μA and an active feedback circuit employing PMOS transistor working in saturation and biased with a current of 300 nA. Dimensions of the input transistor, width equal to 320 μm and channel length of 0.5 μm , are optimized for an input capacitance of 5 pF using the EKV model parameterization. A 90° phase margin for nominal bias conditions and input capacitances up to 15 pF is maintained by two, each of 70 fF, feedback capacitors.

The first section of the shaper consists of two stage voltage amplifier in common source configurations enclosed with a resistive feedback stabilizing the gain and together with feedback capacitance C2 defining the integration time constant. The pulse gain at the output of this stage is in a range of 34 mV/fC and peaking time is about 20 ns. The DC voltage at the output is controlled by the voltage Vfeed applied at the gate of preamplifier feedback transistor and it is optimized for positive or negative input signal polarity using one of the internal biasing DAC.

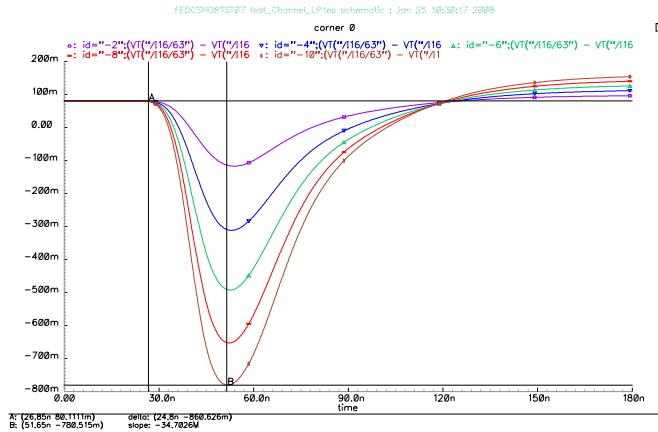


Figure 3: Differential signal as seen at comparator input for charges ranging from -2 to -10 fC. The peaking time for 10 ns charge collection is in the order of 25 ns. The differential gain is around 100 mV/fC.

The second stage of the shaper is an AC coupled differential voltage amplifier with resistive load serving for two purposes. First, it amplifies, integrates and converts to differential mode the single-ended signal from the precedent section. Furthermore, it interfaces the threshold voltage of the comparator, which is applied differentially to the gates of the NMOS source followers. The offset correction voltage is generated as a voltage drop across the load resistor due to the trimming current. The ranges of five-bit trimming DACs are programmable and can provide the trimming steps from 0.5 mV to 3 mV (0.005 to 0.03 fC) depending on the threshold offset spread

The gain at the differential discriminator input is 100 mV/fC and the intrinsic peaking time of the circuit is 22 ns what ensures 25 ns peaking time including the charge collection time in the detector. The simulated responses of the preamplifier-shaper-comparator stage to signals ranging from -2 to -10 fC are shown in Figure 3.

The front-end circuit can accept input signal of any polarity and provides good linearity (Integral Non Linearity less than 3%) for input charges up to ± 10 fC. For the nominal power consumption of 0.7 mW per channel, the calculated ENC for 5 pF detector capacitance is below 800 e^- , which allows using this front-end with heavily irradiated silicon detectors. The ENC as a function of the input capacitance for the nominal bias condition and the maximum expected detector leakage current of 600 nA is shown in Figure 4.

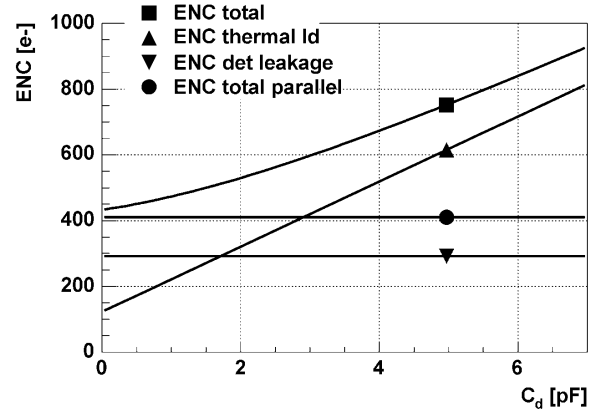


Figure 4: Estimated ENC for 140 μA nominal bias of the input transistor and 600 nA detector leakage current.

The last stage of the signal processing chain is a leading edge comparator with the input stage built of NMOS differential pair loaded with resistors and PMOS transistors serving as swing limiters. This stage is supplied from analog power rails. The following two-stage CMOS amplifier with hysteresis providing amplification and differential to single-ended full swing signal conversion is supplied from the digital power supply lines. This solution ensures good separation between the analog and the digital part of the front-end chain. The simulated attenuation of interferences from digital power supply to the comparator input is better than 56 dB.

The time walk of the comparator depends only on the amplifier peaking time and for input charges from 1.25 fC to 10 fC is less than 15 ns for a threshold of 1 fC.

C. Digital part of the ABCN

The functionality of the digital part of the ABCN is very similar to the ABCD one used in the present ATLAS SCT detector. Some changes have been made to accommodate a simpler redundancy schema, which costs less in number of tracks on the hybrid, and is compatible with different readout rates. SEU detection and correction circuitry have been added. Because the power consumption of the digital part is becoming dominant, special features have been implemented to measure and control the power consumed by the digital blocks.

III. ON CHIP POWER MANAGEMENT AND DISTRIBUTION

The new design includes on-chip power management circuitry to make it compatible with recent developments in the area of power distribution for the Inner Detector Upgrade, namely DC-DC conversion schemes and serial powering scheme.

A. Compatibility with serial powering of detector modules

Serial powering of detector modules offer, in principle, an elegant solution to the power distribution problem, however, it introduces new aspects that have to be addressed in the front-end ASIC. The scheme requires that each module comprising 20 to 40 ABCN ASICs, depending on the module design, have to be powered through a shunt regulator. The shunt regulator can be either an external device, one per hybrid, or can be a distributed structure, i.e. each ASIC contains a shunt regulator, which are then connected in parallel on the module. Each solution has some advantages but none is free of difficulties. Furthermore, neither scheme has been used so far in particle physics detectors. Advantages of the distributed shunt regulator system are:

- power dissipated in the shunt regulators is distributed uniformly across the hybrid,
- no very high current devices are required,
- single point of failure is eliminated, compared to solutions with one regulator per hybrid,
- the hybrid design can be fully scaleable with respect to power distribution.

The ABCN design comprises two prototype circuits, which can be used alternatively. One circuit is a full shunt regulator. Another circuit comprises only shunt transistors, which are foreseen to be controlled by an external regulator, common for all ASICs connected in parallel on the module.

The conceptual schematic diagram of the developed shunt regulator suitable for connecting several shunt regulators in parallel on the hybrid is shown in Fig. 5. In addition to the conventional shunt regulator, the design comprises circuitry responsible for limiting the current flowing through the shunt transistor at a preset level and adjusting the reference voltage and so the output voltage of the regulator. The current of the shunt transistor is sensed and compared with six different reference currents. If the sensed current exceeds the given reference current a correction current source gets connected to the input of the auxiliary transresistance amplifier, which corrects the reference voltage such that it limits the shunt

current in the corresponding shunt device. Simultaneously, other shunt devices connected in parallel sink more current.

It is worth noting that this is a one-step operation and after this operation the correction current source remains connected while the feedback loop between the shunt transistor and the correction circuit is interrupted. Such a solution ensures that the output impedance of the shunt regulator is not affected by the correction circuit.

The current threshold I_{TH} in one of the six stages is set high, about 100 mA corresponding to maximum expected switching current. This stage works like an over current protection circuit in cases when no digital switching current is drawn by the ABCN chip and it has to be taken by the shunt device. The threshold is set by an internal resistor. Three resistors with terminals connected to external pads allow selecting an appropriate threshold according to the digital current draw.

Other five stages work according to the same principle, but their role is to redistribute the current between shunt devices in normal steady-state operation so that the shunt currents and the output impedances of the shunt devices connected in parallel are of the same order of magnitude. The nominal current thresholds I_{th1} to I_{th5} in the five stages are scaled with the following pattern: $\times 1, \times 2, \times 3, \times 4, \times 5$. When the shunt current in the device exceeds given threshold the corresponding correction current is switched on and the reference voltage is adjusted accordingly.

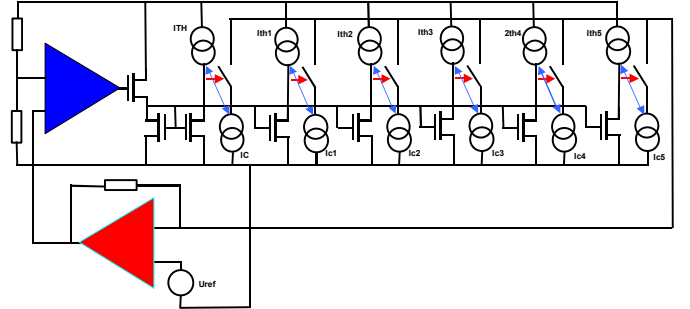


Figure 5: Conceptual schematic diagram of the shunt regulator with auxiliary correction amplifier.

B. On chip linear voltage regulator

The on-chip any-capacitor stable linear voltage regulator provides the voltage supply for the sensitive front-end part of the chip. It is optimized for a high power supply rejection ratio, achieving 33 dB at 30 MHz with 100 nF decoupling capacitor. It provides immunity against the switching noise in case of the DC-DC converter power source is used and separates the analog power supply voltage from the common power supply provided for both the analog and the digital circuits by the shunt regulator in the case of serial powering.

IV. SUMMARY AND PERSPECTIVE FOR CMOS FRONT-END IN 130 NM PROCESS

Analog specifications, functionality, as well as new power management features make ABCN a suitable test vehicle for SCT upgrade R&D program. The front-end circuit of the ABCN is expected to be radiation resistant with respect to TID due to intrinsic radiation hardness of the CMOS

process and by using NMOS transistors with enclosed gates. The architecture of the digital circuitry and its immunity to SEE is a compromise between the requirements for the error rate and power consumption increased by using triple vote logic with auto correction. Therefore its application is limited to most important part of the logic i.e. configuration registers and fast command decoder.

A final choice of the ASIC technology for the Atlas Silicon Tracker Upgrade is not decided yet. However, taking into account the LHC upgrade schedule and present trend for CMOS technology scaling, the final front-end chip for the Upgrade will be manufactured in a technology with the feature size below 250 nm. The two following figures illustrate expected numbers for the ENC and power consumption for the front-end circuits implemented in currently available 130 nm CMOS process from IBM.

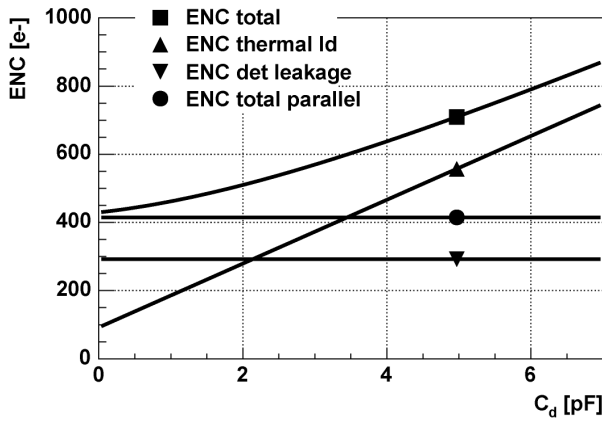


Figure 6: The expected ENC performance of the front-end implemented in IBM 130nm process optimized for short, 2.5 cm, silicon strip detectors. The input transistor bias is equal to 80 μ A, the feedback transistor is biased with 300 nA and assumed detector leakage current is 600 nA.

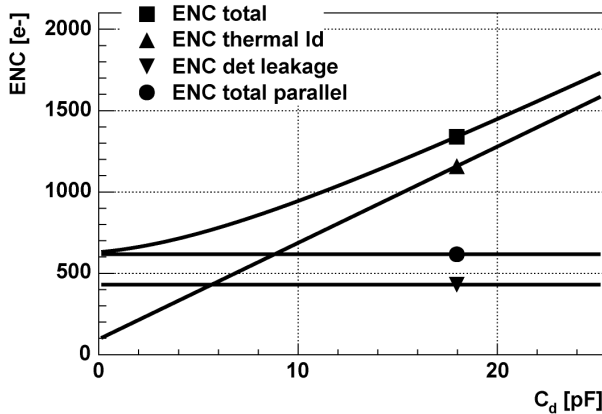


Figure 7: The expected ENC performance of the front-end implemented in IBM 130 nm process and optimized for long, 10 cm, silicon strip detectors. The input transistor is biased with 200 μ A, the feedback transistor is biased with 700 nA and assumed detector leakage current is 1.3 μ A.

From Figure 6 with Figure 4, the latter one obtained for 250 nm process, one can see that a comparable ENC performance can be achieved at significantly lower bias current used in the input stage of the circuit implemented in the 130 nm technology. There are three basic reasons for that. First one is a lower slope factor n , which decreases from 1.45

in the 250 nm process to 1.25 in the 130 nm process. As a result, the transconductance of NMOS devices biased in weak inversion region is only 25% lower than the transconductance of bipolar transistors biased with the same current. In parallel to this, moving from the 250 nm to the 130 nm process the transconductance parameter K_{pNMOS} increases from 300 μ A/V to 750 μ A/V, allowing for biasing of relatively small input devices closer to weak inversion region, which is more optimal from the noise performance standpoint of view. Another important factor taken into account is the level of the excess noise usually present in transistors manufactured in submicron technologies with very short channels. Several measurements done for 130 nm IBM process confirm [6] that there is no excess noise for devices with channel length equal to or longer than 250 nm (for NMOS transistors in IBM 250 nm process excess noise Γ factor was around 1.3).

Further savings of power consumption for the 130 nm design can be expected in the shaper, buffers and comparator stages due to the availability of high value, 1.7 k Ω /square, polysilicon resistors providing low stray capacitances. The expected numbers on power, assuming 1.2 V supply voltage, are 160 and 300 μ W for front-end optimized for short and long strips respectively.

A prototype demonstrator chip comprising the front-end circuits optimized for short and long strips will be manufactured next year in the 130 nm IBM process.

V. ACKNOWLEDGEMENTS

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