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The ABCN front end chip for ATLAS Inner Detector Upgrade

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We present the design of the ABCN front end chip implemented in CMOS 0.25um technology and optimized for short, 2.5cm, silicon strip detectors intended to be used for the upgrade of ATLAS Inner Detector tracker. A primary aim of this project is to develop an ASIC with full functionality as required for readout of short silicon strips in the SLHC environment in a cost-effective and proven technology. Efforts have been put on minimization of the power consumption and compatibility with new power distribution schemes being developed for future tracker detectors. The architecture of the chip as well as critical and novel design aspects will be presented. The ABCN ASIC will serve as a basic testing vehicle in extensive programs on developments of sensor and modules for the upgrade of Inner Detector.

Summary

A primary challenge of the trackers being developed for SLHC environment is the high occupancy, which affects directly granularity of the detectors and the number of electronic channels, to be about 10 times higher compared to the present SCT. As a result, power consumption in the readout ASICs is one of the most critical issues on top of usual requirements concerning noise and radiation resistance. Optimizing the ASIC design with respect to power consumption is by itself not sufficient to solve the problem of power dissipation in the detector and alternative power distribution schemes are being investigated. The ABCN chip is a silicon strip binary readout chip which follows the architecture of the ABCD3T design implemented in BiCMOS DMILL technology and used in present ATLAS SCT detector.

A new front-end circuit optimized for short strips has been developed with a primary goal to reduce the power consumption while maintaining the required noise and timing performance of the circuit. The preamplifier stage is built with a classical cascode stage with NMOS input transistor and an active feedback circuit employing PMOS transistor working in saturation and biased in moderate inversion region. Dimensions of the input transistor, 320um/0.5um, are optimized for an input capacitance of 5pF using the EKV model parameterization. The significant reduction in the overall power consumption of the front end part has been achieved by compromising the bias currents in the buffers, shaper and discriminator stages, which undesirably pronounced the influence of the parasitic capacitances on the overall shaping function of the front end. The final adjustment of capacitances in the filtering stages was done with Spice simulations, taking into account all parasitic capacitances extracted from the layout of the chip. The analogue gain at the discriminator input is 100mV/fC and the intrinsic peaking time of the circuit is 22ns what ensures 25ns peaking time including the effect of charge collection. The front end circuit can accept input signal of any polarity and provides good linearity up to +/-10fC input charges. For the nominal consumption of 0.7mW per channel, the calculated ENC for 5pF detector capacitance will be below 800e-, which allows the use of this front end with heavily irradiated silicon detectors having low charge collection efficiency and high leakage current.

The functionality in the digital part of ABCN is very similar to the ABCD3T one, used in the present ATLAS tracker. Changes have been made to accommodate a simpler redundancy schema, which costs less in number of tracks on the hybrid, and different readout rates. SEU detection and correction circuitry have been added. Because the power consumption of the digital part is becoming dominant, special features have been implemented to measure and control the power consumed by the functional parts.

The new design includes on-chip power management circuitry to make it compatible with recent developments in the area of power distribution for the Inner Detector upgrade, namely DC/DC conversion schemes and serial powering scheme. On the ABCN chip we have implemented two prototypes of shunt regulators with scalable architecture capable to generate local power supply in case of serial powering of the detector modules. The on-chip any-capacitor stable linear voltage regulator provides the voltage supply for the sensitive front end part of the chip. It is optimized for high supply rejection ratio, achieving 33dB at 30MHz with 100nF decoupling capacitor. It provides immunity against the switching noise in case of the DC/DC converter power source, and separates the analogue voltage from the common voltage provided for both the analogue and digital circuits by the shunt regulator in the case of serial powering.

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