

Noise Analysis of Radiation Detector Charge Sensitive Amplifier Architectures

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Abstract

In this work, a detailed comparison of four equivalent charge-sensitive, folded-cascode amplifiers in terms of noise performance is presented. A couple of complementary structures, one with a noise-optimised input nMOSFET and the other with a noise-optimised input pMOSFET were designed in 0.35 μm CMOS process by Austria MicroSystems (AMS). Another couple of complementary structures consisting of a noise-optimised input npn with a pMOSFET cascode, and the respective structure having a pMOS as input device, were developed in a 0.35 μm SiGe BiCMOS process (AMS). The structures' comparison is performed through simulation, after careful selection of the parameters that remain constant in all four variations.

I. INTRODUCTION

High Energy Physics Experiments (HEPE) have given a great boost to the analogue VLSI for front-end devices applied to Solid State Detectors, the main reason being the large number of channels required for such experiments. The charge generated by the X-rays – Sensors interaction is very small and has to be amplified in a low noise circuit before any further signal processing. The growing number of channels, more in multi-detector systems, sets different problems. Regarding the power dissipation-noise limitations, it is better to put the detector and the front-end amplifier as close as possible. However the heat transferred from the amplifier to the detector can create problems of drift and make its resolution worse. Concerning the active occupied area the segmentation of the multi-detector systems is mainly limited by the preamplifier size and finally regarding the total cost, the price of a preamplifier depends on the technology involved. A VLSI preamplifier costs much less than a hybrid one or a preamplifier unit.

While literature is available on the noise behaviour of the front end stages [1]-[2], contrary few studies have been performed regarding the used process configuring the radiation detection ASIC and the related trade offs. The main problem in the design of nuclear spectroscopy VLSI readout front ends is the implementation of low noise – low power Charge Sensitive Amplifier (CSA) – Shaper systems (figure 1) and the selection of the process (CMOS or BiCMOS) determines the total performance and generally the noise related design methodology. Non extended research has been performed comparing the use of a MOSFET or a bipolar device as the input device of the pre-amplification cell in terms of the total noise contribution setting strict comparison constraints.

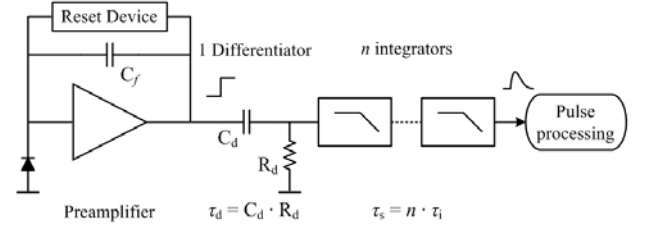


Figure 1: Preamplifier-Shaper readout front end analog processor

The folded cascode architecture is selected as the pre-amplification optimum structure due to its low noise performance, the high gain capability and its gain insensitivity to the detector capacitance variations. In this work, four equivalent folded cascode pre-amplification structures are compared in terms of the total noise contribution. Specific design constraints are applied in order the comparison to be valid and selection criteria are suggested in relation to the application specifications and the related application IC process.

II. PREAMPLIFICATION STAGE ANALYSIS – NOISE OPTIMIZATION METHODOLOGIES

A detector readout system's noise performance is expressed as the equivalent noise charge (*enc*) (ratio of the total *rms* noise at the output of the pulse shaper to the signal amplitude due to one electron charge). The noise contribution of the amplification stage is the dominant source that determines the overall system noise and is therefore, optimized. The main pre-amplification stage noise contributor is the CSA input device. The noise optimisation methodologies regarding CMOS and BiCMOS CSA implementations are provided below.

A. CMOS Implementations

The main noise contributor is the CSA input MOSFET and the noise types associated with this device are $1/f$ and channel thermal noise. The respective *encs* are given by [1]-[5]:

$$enc_{th}^2 = \frac{8}{3} kT \frac{1}{g_m} \left(\frac{n!^2 e^{2n}}{n^{2n}} \right) \frac{B(\frac{3}{2}, n - \frac{1}{2})}{q^2 4\pi\tau_s} C_t^2 \quad (1)$$

$$enc_{1/f}^2 = \frac{K_f}{C_{OX}^2 WL} \left(\frac{n!^2 e^{2n}}{n^{2n}} \right) \frac{1}{q^2 2n} C_t^2 \quad (2)$$

where B is the euler beta function, q is the electronic charge, τ_s is the peaking time of the shaper and n is the order of the semi Gaussian shaper. Capacitances C_d , C_f , C_{GS} and C_{GD} are capacitances of detector, feedback, gate-source and gate-drain of the input MOSFET respectively, and C_p is the parasitic capacitance of the interconnection between the detector and the amplifier input, which is generally considered negligible. k is the Boltzmann constant, T is the temperature, g_m is the transconductance, K_f is the flicker noise constant depended on device characteristics and able to vary widely for different devices in the same process, variables W , L and C_{ox} represent the transistor's width, length and gate capacitance per unit area respectively.

The total input stage capacitance is given by [1]-[5]:

$$C_t = C_{total.in} = C_d + C_p + C_f + C_{GS} + C_{GD} \quad (3)$$

Optimum gatewidths exist for which the respective thermal and flicker $encs$ are minimal. These optimum dimensions are extracted by minimizing the respective $encs$.

$$\frac{\partial enc_{th}}{\partial W} = 0 \Rightarrow W_{th} = \frac{C_d + C_f}{2C_{ox} \alpha L} \quad (4)$$

$$\frac{\partial enc_{1/f}}{\partial W} = 0 \Rightarrow W_{1/f} = 3W_{th} \quad (5)$$

where α is defined as $\alpha = 1 + \frac{9X_j}{4L}$ and X_j is the metallurgical junction depth. Equations (4) and (5) are valid when capacitance C_d is in the range of picofarad. When the dominant noise component is determined, the CSA input transistor type and its optimum dimensions are selected, considering that typically P-MOSFETs have less $1/f$ noise than their n-channel counterparts

B. SiGe BiCMOS Implementations

Normally, the Equivalent Noise Charge for a bipolar transistor as an input device is determined by the parallel noise and series noise contributions. For an optimized pre-amplifier design, these two contributions, mainly characterized by the base and collector current shot noise and the base spreading resistance R_{bb} , are given by an equivalent input noise voltage source and a current source with noise spectral densities [6]:

$$S_{v_n} = 4kT(R_{bb} + \frac{1}{2g_m}) \quad (6) \quad g_m = \frac{qI_c}{kT} \quad (7)$$

$$S_{i_n} = 2qI_B$$

The series noise voltage is built up from two components, the base spreading resistance R_{bb} and the transconductance of the input transistor. In order to minimize the spreading resistance which is scaled inversely by the emitter area, a large emitter area should be chosen. As mentioned above, the main radiation effect observed in bipolar transistors is the degradation of the current gain β . This effect is inversely proportional to the current density in the base area and from

this point of view a small emitter device is preferable. In order to keep the lowest base spreading resistance, multiple base contacts should have been used and the width of the emitter region is set to minimum that gives a minimal distance between the base contacts and the emitter. From Equations an important fact can be found that there is an optimum collector current I_c where the total noise contribution is minimum. With a CR-RC type of shaper, the approximate expression for enc referred to the input is given below:

$$enc = \sqrt{3.67 \frac{kTC_T^2}{q^2 \tau_s} \left(R_{bb} + \frac{kT}{2qI_c} \right) + 1.83 \frac{\tau_s I_c}{q\beta}} \quad (8)$$

where τ_s is the shaping time and $C_T = C_D + C_{in} + C_f$, C_D the detector capacitance, C_f the feedback capacitor and C_{in} the input capacitance of the input bipolar transistor of the CSA. It can be observed that noise performance of an electronic frontend depends on the shaping time of the preamplifier-shaper and the capacitor C_T . For a given shaping time, the detector capacitance and current gain, an optimum collector current which gives minimum noise can be obtained:

$$I_{Copt} = \sqrt{\beta} \frac{C_T V_{th}}{\tau_s} \quad (9) \quad \text{where} \quad V_{th} = \frac{kT}{q} \quad (10)$$

In contrast to the CMOS case where optimum noise performance is achieved by choosing the dimension of the input transistor for a given detector capacitance, in bipolar devices, the optimum noise matching can be achieved by adjusting the collector current of the input transistor for any detector capacitance.

III. FOLDED CASCODE AMPLIFIER TOPOLOGIES DESIGN - COMPARISON

Four equivalent folded cascode amplifying topologies were designed. Our primary concern was the examination of noise contribution of the devices pair, firstly the input transistor and secondary, the cascoded one. The four structures were: a) nMOS as the input and pMOS as cascode, b) pMOS as input, nMOS as cascode, c) npn BJT as input, pMOS as cascode and d) pMOS as input and npn BJT as cascode. To further isolate these noise contributors, ideal bias current sources and output buffer were used, in all four designs. Feedback was implemented using a capacitance in parallel with a large reset resistor. The structures were designed in two respective processes commercially available by Austria Mikro Systeme (AMS), the 0.35 μ m CMOS process (2P/3M 3.3/5V) and the 0.35 μ m SiGe BiCMOS process (2P/3M 3.3/5V). All four folded cascode topologies are depicted in figure 2.

In order to achieve a fair comparison, the bias current of the input branch was selected by applying noise-optimisation theory on the input npn available transistor (equation 9). This bias was then kept constant for the rest implementations, where noise-optimization methodology was applied regarding the input MOS type to set its dimensions. This bias current selection, in addition to constant total power (current) consumption, leads to a constrained bias current for the cascode. This, in the case of the BJT cascode, results to a

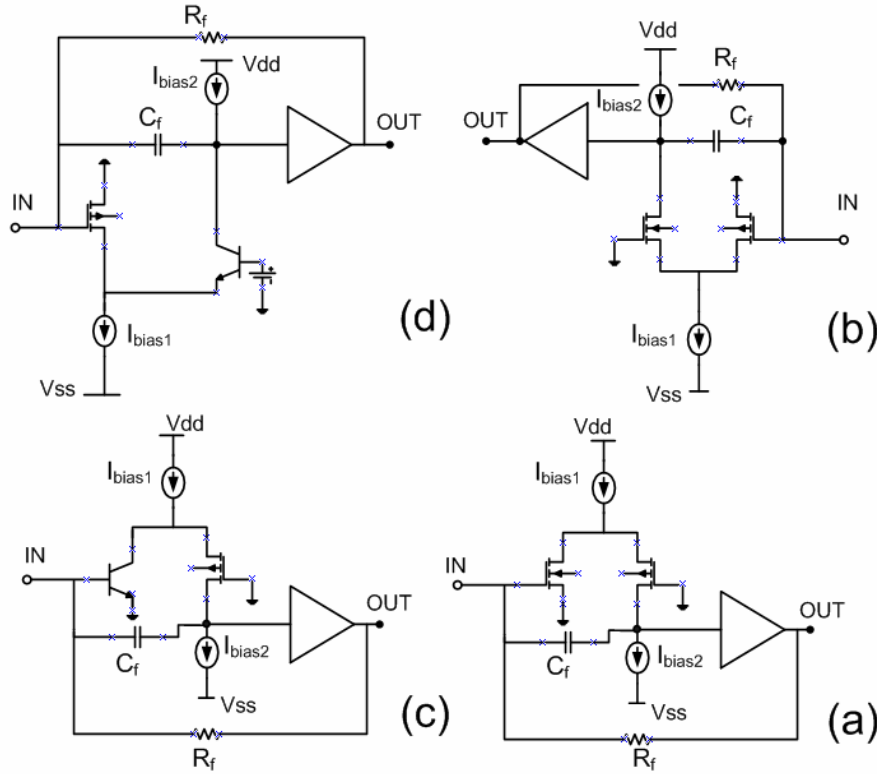


Figure 2: Four equivalent folded cascode amplifying topologies

specific transconductance value, constraining the cascode MOS dimensions in the rest cascode structures.

A table containing the comparison specifications – design characteristics is depicted below (table 1). In all these configurations the noise contributors are the input device, the cascode one and the feedback resistor.

Table 1: Design – Comparison Specifications

Application Specifications	
Detector Capacitance	2 – 20 pF
Temperature	27°C
Peaking time	100 ns
Comparison Specifications – Design characteristics	
Ibias 1	15 μ A
Ibias 2	7.6 μ A
Vdd = - Vss	1.65 V

The optimum collector current was found equal to 7.4 μ A. Regarding the optimum dimensions of the input MOS device, in the case of an NMOS the dimensions were equal to $(W/L) = (476\mu\text{m}/0.35\mu\text{m})$ and in the case of a PMOS device $(W/L) = (1428\mu\text{m}/0.35\mu\text{m})$. The AC response of the four configurations is depicted in figure 3. All the topologies provide an operating bandwidth of 107 kHz and an output gain of 130 dB. Regarding the total power dissipation, in all the topologies 36.95 μ W are consumed. The cascode parasitic transconductance is also equal for all four structures.

Regarding the output noise performance, the output noise spectral density is given in figure 4. As it is obvious the higher noise performance is observed in the SiGe BiCMOS while the lower is observed in the architectures with the

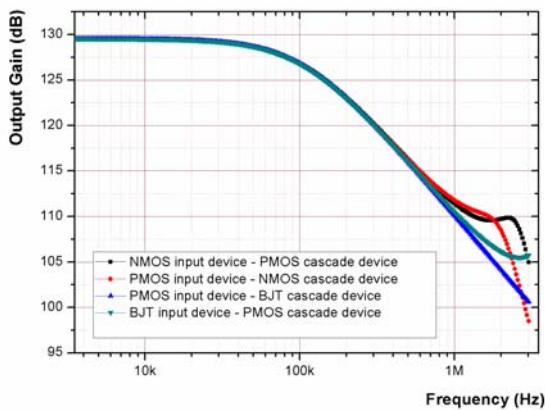


Figure 3: Folded cascode topologies AC response –output

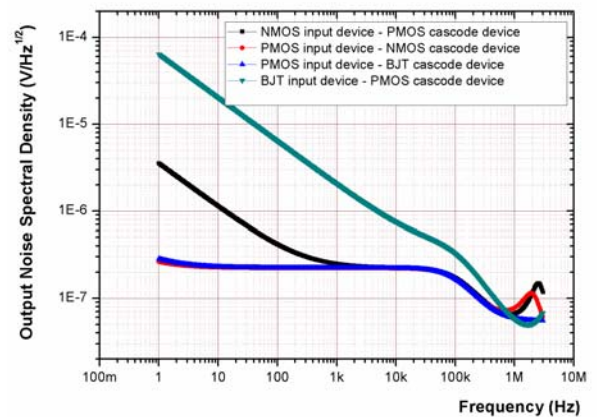


Figure 4: folded cascode topologies output Noise

PMOS input device. The respective rms noise values at the CSA topologies output is depicted below. An overall table regarding the output noise dependence in the detector capacitance value is also provided (table 2). While the implementation with the BJT input device appears to provide the higher output noise, it also provided the lower slope regarding the increment of the rms noise in relation to the detector capacitance indicating as suitable for large detector capacitance applications, as shown in fig. 5.

Table 2 : RMS Output Noise Vs Detector Capacitance

	Output Noise Vs Detector Capacitance
NMOS input – PMOS cascode	$55.23\mu\text{V} + 2.99\mu\text{V/pF}$
PMOS input – NMOS cascode	$59.90\mu\text{V} + 0.99\mu\text{V/pF}$
PMOS input – BJT cascode	$60.13\mu\text{V} + 0.98\mu\text{V/pF}$
BJT input – PMOS cascode	$240.2\mu\text{V} + 0.23\mu\text{V/pF}$

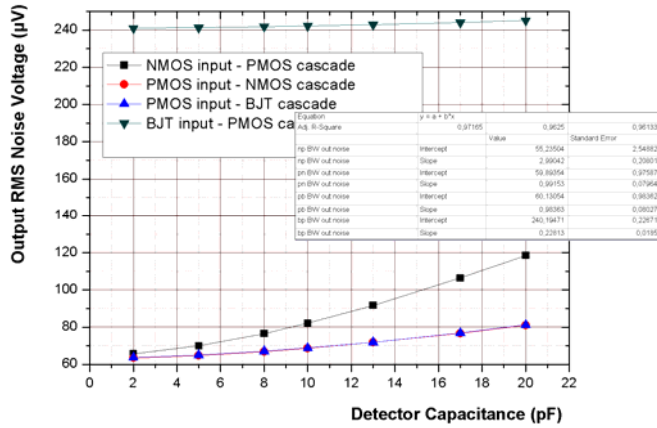


Figure 5: Output Noise vs detector capacitance

IV. CONCLUSION AND DISCUSSION

In this work a comparison of four folded cascode preamplifier topologies is presented, in order to find out the preferred topology in terms of noise performance, respecting to the technology and design specifications. PMOS input-NMOS cascode, NMOS input-PMOS cascode, PMOS input-npn BJT cascode and npn BJT input-PMOS cascode and CMOS 0.35um and SiGe BiCMOS 0.35um were used. In all the topologies consumption was kept constant while the only noisy devices were the input transistor, the cascode transistor and the feedback element. Also the capacitance seen by the input transistor was also calculated to be equal in all the implementations. Simulation results demonstrate the superiority of the PMOS transistor as input device for small or medium size of detector capacitance, while the BJT transistor could be a good candidate in case of large detector capacitance.

Regarding the future work, extra analysis should be performed regarding the noise contribution of the feedback elements and the optimum selection in terms of the related design specifications.

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