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Noise analysis of Radiation Detector Charge Sensitive Amplifier Architectures.

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In this work, a detailed comparison of four equivalent charge-sensitive, folded-cascode amplifiers in terms of noise performance is presented. A couple of complementary structures, one with a noise-optimised input nMOSFET and the other with a noise-optimised input pMOSFET were designed in 0.35 um CMOS process by Austria MicroSystems (AMS). Another couple of complementary structures consisting of a noise-optimised input npn with a pMOSFET cascode, and the respective structure having a pMOS as input device, were developed in a 0.35 um SiGe BiCMOS process (AMS). The structures' comparison is performed through simulation, after careful selection of the parameters that remain constant in all four variations.

Summary

Detailed analysis was performed for the folded cascode architecture. Our primary concern was the examination of noise contribution of the devices pair, firstly the input transistor and secondary, the cascoded one. The four structures were: a) nMOS as the input and pMOS as cascode, b) pMOS as input, nMOS as cascode, c) npn as input, pMOS as cascode and d) pMOS as input and npn as cascode. To further isolate these noise contributors, ideal bias current sources and output buffer were used, in all four designs. Feedback was implemented using a capacitance in parallel with a large reset resistor.

In order to achieve a fair comparison, the bias current of the input branch was selected by applying noise-optimisation theory on the input npn available transistor. This bias was then kept constant for the rest implementations, where noise-optimization methodology was applied regarding the input MOS type to set its dimensions. This bias current selection, in addition to constant total power (current) consumption, leads to a constrained bias current for the cascode. This, in the case of the BJT cascode, results to a specific transconductance and parasitic capacitance value, constraining the cascode MOS dimensions in the rest cascode structures.

The output noise was examined in relation to the detector's capacitance variation and the input branch's bias current. In addition, the peaking time dependence (and consequently the operating bandwidth variation) was also examined, concerning the total output noise.

The results of this work aim in proposing input device selection criteria and consequently the folded cascode structure, in relation to the output noise, detector's capacitance variations and the available process (CMOS or SiGe BiCMOS) in conjunction with fabrication cost.

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