Readout architecture of the ATLAS upgraded tracker

G. Darbo[a], Ph. Farthouat[b], A. Grillo[c,]

[a] INFN Genova, Genova, Italy
[b] CERN, 1211 Geneva 23, Switzerland
[c] UCSC, University of California Santa-Cruz, USA

Philippe.Farthouat@cern.ch

Abstract

The basic concept of the Inner Detector in the Atlas Detector upgraded for the Super-LHC is being elaborated and proposed.

The readout electronics of this new detector is based on a hierarchical architecture involving front-end chips (FEIC), Module Controller chips (MC) and Stave Controller chips (SC) and a few high speed readout links.

The design is still in a very early phase and a lot needs more detailed studies, however, some architectural issues can already be described. This article will briefly describe the proposed detector layout and its environmental conditions, the proposed readout architecture and the main parameters associated to it (mainly for the strip detector), the different options for the detector control system and the powering of the readout electronics.

I. INTRODUCTION

The basic concept of the Inner Detector in the Atlas Detector upgraded for the Super-LHC is being elaborated and proposed. It is assumed that the small radius layers will be built using pixel detector technology while the mid and large radius layers will be built using silicon strip technology. Furthermore, it is assumed that strips of different lengths will be used in the middle and in the outer layers in order to keep the strip occupancy and the detector leakage current and charge trapping due to radiation damage at acceptable levels.

The readout electronics of this new detector is based on a hierarchical system involving front-end chips (FEIC), Module Controller chips (MC) and Stave Controller chips (SC).

This document will first present the proposed detector lay-out and its environmental conditions, followed by the readout requirements and some system considerations.

The design study of the detector still in progress and very likely subject to change, some of the information given in this article might become obsolete and inaccurate.

II. UPGRADED DETECTOR

This section gives a short overview of the organisation of the detector for both strips and pixels as well as some of the environmental conditions. Some details concerning the barrel strips detector are also given.

The current straw-man layout [1] is given in Figure 1.

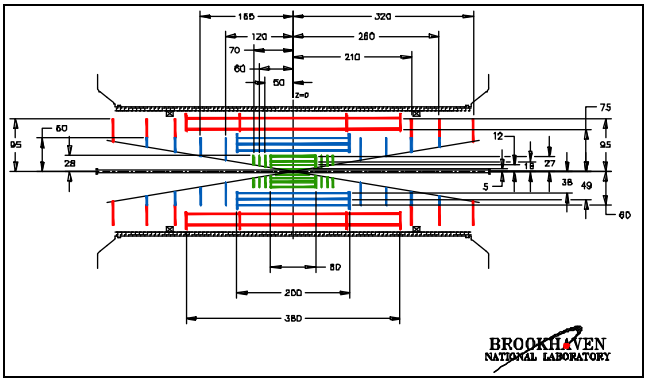

Figure 1: Current straw-man layout. There are 4 layers of pixels, 3 layers of short strips and 2 layers of long strips.

A. Pixel layers

There is not yet a design concept for the pixel detector, however, it is assumed that the most inner layer (B-layer) is made with FEICs 4 times bigger than the current one and that the pixel size is ½ the current one [2]. One FEIC would then handle about 20,000 channels. The outer layers, having lower pixel occupancy, will use a slightly larger pixel size , 250 µm x 50 µm, but still smaller than the current one.

B. Strip layers

Two types of strips are considered: the short strips (2.5-cm length, 80-µm pitch) in the inner most layers and the long strips (10-cm length, 80-µm pitch) in the outer layers. They are all based on detector modules of 10x10-cm^2; a long strips module will have 1280 channels while a short strips module will have 4x1280 channels.

The detector will be mounted in double-sided staves (Figure 2) which can be as long as 4-m for the long strips.

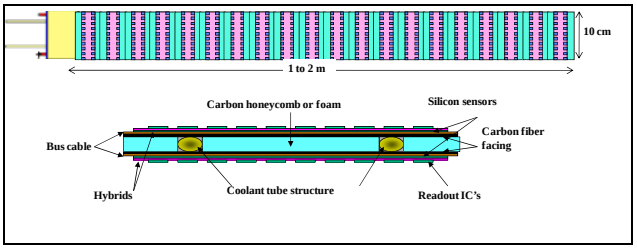

Figure 2: View of a half barrel stave. There are detector modules on both sides and all the services (electrical, cooling) are embedded in the stave. The readout hybrids are glued on the modules.

Table 1 details the barrel strips detector in number of staves, modules, 128-channel FEIC and number of channels. For comparison, the current silicon strips detector contains 4088 modules, about 50,000 FEIC and 6,000,000 channels.

Table 1: Number of elements in the barrel strips detector.

Layer	Type	Radius [cm]	Phi segment.	Modules per half single sided stave	128-ch FEIC per half single sided stave
0	Short	38	28	10	400
1	Short	49	36	10	400
2	Short	60	44	10	400
3	Long	75	56	19	190
4	Long	95	72	19	190
Total number of staves					236
Total number of modules					14,336
Total number of 128-ch FEIC					270,080
Total number of channels					34 10^6

C. *Temperature and magnetic field*

The detector will have to be maintained at low temperature (-30°C) and the magnetic field in the tracker volume will be 2T.

D. *Radiation level*

The upgraded detector will run until a 3000 fb^{-1} integrated luminosity will be obtained. The detector and its electronics have to be designed for twice as much, i.e. 6000 fb^{-1}.

The total ionising dose (TID) will be about a factor 10 higher than for the current detector and is given in Table 2.

Figure 3 gives the fluence expected in the tracker volume. At the level of the pixel detector, more than 10^{15} $n.cm^{-2}$ are expected while for the strip detector it is in the range 10^{14} - 10^{15} $n.cm^{-2}$. Note that these numbers take into account the introduction of moderators which are necessary in order to reduce the amount of high energetic neutrons which are very damaging for the sensors.

Table 2: Total ionising dose in kGy for 3000 fb-1 integrated luminosity at different radii.

Radius in cm	Dose in kGy
5.05	15800
12.25	2540
29.9	760
51.4	450
43.9	300
108	70

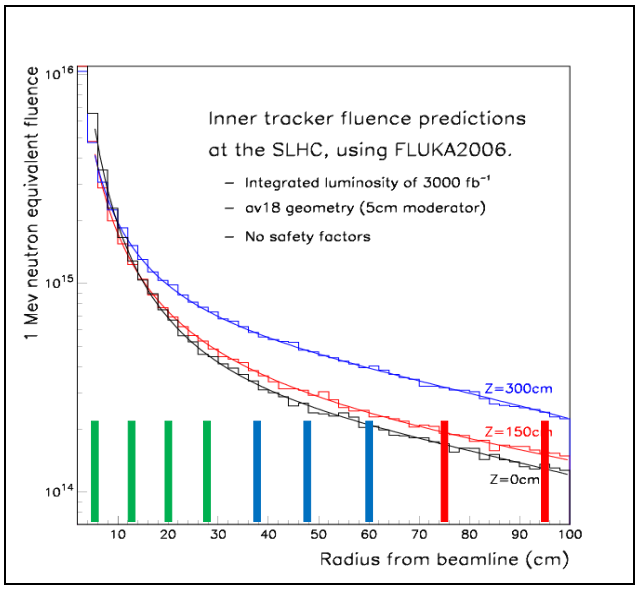

Figure 3: 1 MeV neutron equivalent fluence for 3000fb^{-1} integrated luminosity. Vertical bars show the positions of the pixel layers (4 smaller radii), short strips (3 next ones) and long strips (2 larger radii).

III. Readout Architecture

The readout of the current strips detector is organised around the modules: each of the 4088 modules is an autonomous readout entity, meaning that there are 4088 power supply channels and 4088 sets of readout and TTC optical links. Although this architecture has shown to be working, it is not usable for the upgraded tracker because of the large amount of services that it would imply.

Both the pixels and strips architecture must be changed to reduce services per readout channel. The following describes the concepts of the generic architecture for pixels and strips with specific examples for strips and some information for pixels where available.

A. *Generic architecture*

The architecture will be based on a hierarchical model and the readout electronics system will divided in three main blocks:

- The FEIC handling a number of channels (typically 128 for the strips and up to ~20,000 for the pixel detector);
- The Module Controller (MC) that distributes timing and control to the front-end ASICs of a module and receives data from them;
- The Stave Controller (SC) that distributes timing and control to the modules receives data from them and after concatenation ships the data through a Gbit link to the off-detector electronics.

The MC and SC should also contain the necessary electronics to handle the slow control of the detector, either directly (i.e. including ADCs, DACs, temperature sensors) or interfacing to a separate DCS chip.

Figure 4 shows a schematic view of this generic architecture as described in [1].

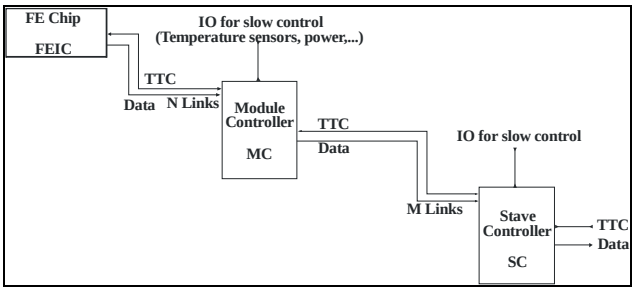

Figure 4: Generic view of the readout electronics.

B. *Readout unit*

The detector is organised in staves regrouping either 10 (short strips) or 19 (long strips) modules. Each stave is made of two layers in order to have a double-sided detector. These two layers will be treated separately from the readout point of view. The data of a single-sided stave will be collected at the level of a stave controller (SC). Each module on the stave has either one (long strips) or two (short strips) readout hybrids. In both cases, the readout unit is the hybrid. The hybrid will host n FEICs (n=20 in the case of the short strips and n=10 in the case of the long strips) and a so-called module controller (MC) which will gather the data of the hybrid FEICs and transmit them to the SC.

Figure5 is a sketch of a single-sided stave of short strips.

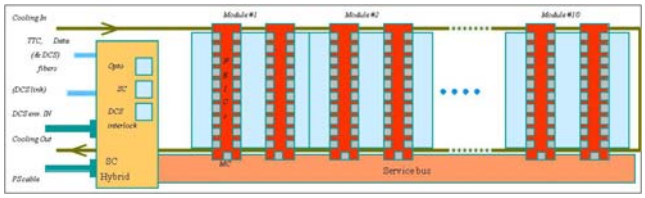

Figure 5: Sketch of a single-sided stave of short strips. 10 modules are readout by 2 hybrids of 20 FEICs each. A stave controller gathers the data from all module hybrids and interfaces to the off-detector electronics. Each hybrid houses a module controller which interfaces the FEICs to the SC. The DCS data can either be sent together with the readout data or be sent on a dedicated link.

C. *Working assumptions*

It is assumed that the current ATLAS binary readout will be used and that the interface to the ATLAS TDAQ system will remain the same although an increase of the level-1 latency is anticipated.

In the current system, the L1A rate does not exceed 100kHz. An increase of this rate would have a dramatic effect on the readout system. For instance doubling this rate would mean either to double the amount of data to be extracted or to perform a selective readout.

However, when defining the needed bandwidth at different places (on modules, from modules to end of staves and from staves to off-detector electronics) some safety margin should be taken. This will allow a bit of flexibility on the L1A rate (and also on the maximum luminosity the machine can reach).

The amount of energetic hadrons (more than 20MeV) susceptible of generating SEU will be very high and hence SEUs will appear everywhere. The following policy will be adopted:

• The static registers holding thresholds, masks, etc. will be implemented with triple redundant logic;

• The "physics data" themselves will not be protected, as a SEU acts as a small excess of noise and because the data do not stay for a long time in the FEICs;

• Level-1 identifier (L1ID) and Bunch Crossing identifier (BCID) will not be protected as they stay a very short time in the front-end. In addition an error is very easily detected in the off-detector electronics and the policy of periodic resets will be maintained (there is a Bunch counter reset every 90 μs and an Event counter reset at a relatively high frequency [order of Hz] which can be used to reconfigure the front-end);

• Special care will have to be taken for the transmission to the front-end of the trigger and control (TTC) as the receiving PIN diodes are very sensitive to SEU;

• Complex logic in the front-end, very likely sensitive to SEUs, will be avoided as much as possible.

There are several different possibilities to organise the readout of the tracker elements and definitely not a unique solution. Each time choices between different options are to be considered, the following criterions will be applied to select one:

• The readout architecture should be as identical as possible for the strips and the pixels so that one can avoid extra design diversity and share as much as possible design efforts and costs. This common approach is to be applied from the front-end electronics up the off-detector electronics. In particular the Readout Drivers (ROD) for the strip and pixel detectors are assumed to be identical (as they are in the current design);

• The material budget is a key element for the upgraded tracker and hence the solutions which minimise the amount of material are always preferred;

• The radiation environment of the front-end electronics will be extremely harsh. In particular a high level of single event upsets can be expected. The readout architecture should be kept as simple as possible and in particular complex tasks such as partial event building, data integrity check, etc. requiring extra buffers in the front-end should be avoided;

• The amount of services connected to the tracker should be kept as low as possible, not only to maintain an overall low material budget (the services located at large radius are less damaging to the calorimeter resolution) but also because the available volume for services routing is severely limited. This will also ease the installation process.

D. *Quantity of data*

Simulations of the strips barrel part [3], based on worst SLHC scenario (50 ns BC period, 400 pile-up events per BC), worst part of the detector (short strips) and a 1.2 to 1.35 safety

factor on the number of hits, have been made. The current readout data format has been used.

Figure 6 shows the distribution of a short strips module event size. The mean number of bits for 40 FEICs is 1554, i.e. 777 for a readout hybrid. A 100kHz L1A would lead to a mean readout speed of 77.7Mbits/s.

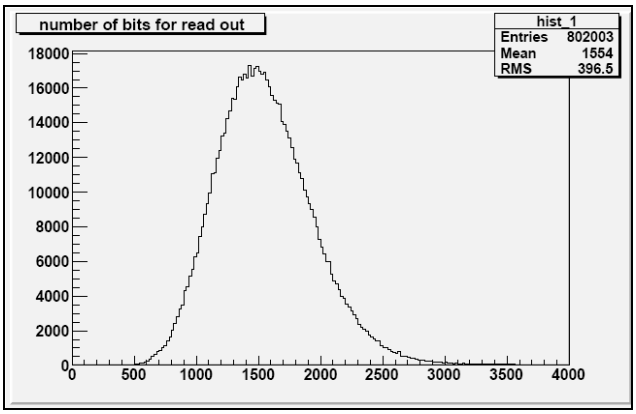

Figure 6: Event size for a short strips module (40 128-channel FEICs). The coding scheme is the same as the one used in the current ATLAS SCT detector. The luminosity is 10^{35} cm-2 and the beam crossing period is 50ns (worst case). A safety factor of 1.35 on the occupancy is applied, however, in the case a DC balanced code is needed, this safety factor is only 1.2.

An 80Mbits/s link between the 20 FEICs of a readout hybrid and the MC would be acceptable as long as sufficiently large derandomising buffers are available in the FEICs. However, as already mentioned, the safety factor used for the simulation is not very large and some uncertainties remain concerning the actual L1A rate which can be obtained and also about the ultimate machine luminosity. In addition, it is anticipated that the pixel detector will require higher bandwidth and hence it is deemed reasonable to implement a 160Mbits/s readout speed per readout hybrid (i.e. for 20 FEICs).

The MC-to-SC links will also have to run at 160Mbits/s and as up to 10 modules (i.e. 20 readout hybrids and hence 20 MC) can be connected to a SC, the output bandwidth of the SC must be at least 3.2Gbits/s. Figure 7 shows the bandwidth requirements in different places.

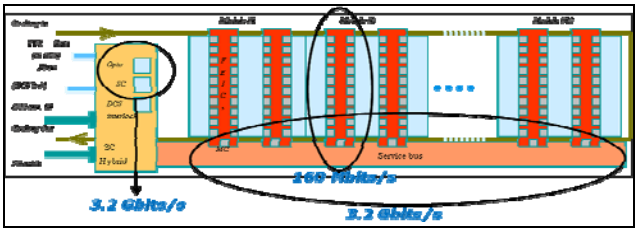

Figure 7: Bandwidth requirements on the readout hybrids, the stave service bus and the optolinks.

E. Trigger, timing and control (TTC)

The TTC links are used to transmit to the front-end a clock synchronised with the beam (either the LHC clock or a multiple of it), the L1A, fast commands such as the bunch counter reset (BCR) or the event counter reset (ECR), control data to be stored in the FEICs, MCs and SCs (e.g. threshold, masks, …) and slow commands allowing reading the contents of registers in the different ICs. In order to limit the amount of material, these links will be unidirectional: when reading a register, the command is transmitted on this link but the data will be transmitted on the readout data link. The necessary TTC links bandwidth is dictated by a number of parameters, such as the clock frequency to be transmitted, the need for transmitting simultaneously the L1A and other commands (e.g. Bunch Counter Reset [BCR]), the necessity for transmitting some information with the L1A (e.g. a trigger type), the need for DC balanced codes, etc. The bandwidth of these links should be greater than or equal to 80 Mbits/s.

F. Links

All the links on the staves and hybrids will be electrical. Some studies are on-going in order to assess what is achievable in different places. It is in particular important to select the proper protocols (single high speed data-clock encoded links versus multiple low speed links for instance) and to know whether multi-drop links can be safely used.

The optical links connecting the staves to the off-detector electronics have to run at a reasonable speed but are to be very radiation hard. The project relies heavily on the on-going development of the Versatile Link [4].

G. Data format

The data format used in the current detector is highly optimised in size. The drawback of this optimisation is that the front-end chips have to analyse the transmitted data “on the fly” in order to decide what to do. This might be a problem when large amounts of SEU are expected as complex state machines can be disturbed anytime. It could be better to consider the system as a network and to push packets of data from the FEIC up to off-detector electronics and let the off detector electronics make the necessary work to separate the different types of data (physics data, control data, register contents,...) and to assemble sub-parts of an event. That would simplify the on-detector electronics (very likely at the expense of higher bandwidth for the data transmission) and use efficiently the high power of FPGA in the off-detector electronics.

H. Redundancy

Redundancy can have a large impact on the readout architecture as it could add some complexity and increase the number of devices to be installed (e.g. doubling all the opto-electronics devices if one wants to be fully protected against an optical link failure). Some work is still necessary to evaluate the impact of losing a FEIC, a readout hybrid or a half single sided stave. After that step and based on the expected failure rate of the different components of the system, the need for redundancy can be assessed.

IV. Power

The power consumption of the FEIC is still unknown but it is deemed very reasonable to assume it will not be higher

than 1 – 1.5mW per channel. Based on this assumption and assuming a (pessimistic) 1.3V Vdd, 100 – 150mA per 128-channel FEIC is needed. The total current for the barrel and end-caps strips detector would then be in the range 33 – 48.5kA. The current ATLAS SCT and TRT detectors (occupying the volume of the future strips detector) are fed with about 12kA. If we take this amount of injected current as an upper limit, a powering scheme allowing a 5 – 6 saving factor on the current one has to be used.

There are on-going developments on serial powering [5] and DC-DC conversion [6]. Both schemes can easily reduce the current to be supplied by the required factor.

At the system level, DC-DC converters offer some very interesting flexibility as they allow easy switching on and off of different elements (e.g. stave controller, readout hybrids) as well as a full separation of analogue and digital supplies leading to some potential saving in overall power. However, there is not yet a viable device today. A serial powering scheme is capable of potentially large saving in current (powering 10 to 20 devices in series is feasible) but some system issues have still to be addressed. Both options must be kept opened for the time being and the readout system must be able to accommodate both.

V. On-going developments and next steps

A working document on the readout architecture [7] is available since about a year. It has been reviewed and presented to the collaboration and is going to be updated. Two working groups (one for the pixels and one for the strips) are in place to try and define more precisely the specifications of the different components. These specifications will be used for the design of the different components but also as an input to the "common projects" teams (e.g. for the Giga Bit Transceiver [GBT] project [8]).

Common solutions with other experiments are mandatory for some of the components. The proposed readout architecture involves (for the strips) about 350,000 FEIC but only about 20,000 MC and 5,000 SC. A production of only 5,000 parts in a very high speed technology is absolutely not economically viable.

A full 0.25 μm CMOS readout chip (ABCn [9]) has been developed to be used as a test vehicle for sensor and different power and readout scheme studies. Preliminary study of the front-end part (preamplifier-shaper-discriminator) in 0.13 μm CMOS technology have shown very good power performances (<200μW per channel).

The schedule for the detector and its readout electronics developments is not yet fully understood but looks already very tight: in order to be ready for a full replacement in the year 2017 (to start data taking in 2018) one has to start the staves assembly in the year 2013 with all the final components available...

VI. Conclusion

The readout architecture of the ATLAS upgraded tracker has to be different from the current one. The detector will be organised in staves and a hierarchical readout scheme will follow this segmentation. One consequence will be the use of fewer but higher speed readout links.

Some elements of the readout electronics are not to be produced in very large quantity. This points towards common solutions with other experiments.

The power distribution requires special efforts to maintain a reasonable amount of current to be supplied to the detector and consequently a manageable volume of services. A saving factor of the current in the range 5 - 10 has to be achieved.

VII. Acknowledgements

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