Development of a Front-end Pixel Chip for Readout of Micro-Pattern Gas Detectors.

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Abstract.

With growing importance of Micro-Pattern Gas Detectors in high-energy physics there is a need to develop a dedicated front-end read-out chip. The new chip should secure high spatial resolution provided by the gas-filled pixel detector and be able to operate at high track rates. In addition, it is highly required to keep power consumption as low as possible.

A number of prototype IC's have been submitted in order to demonstrate the performance of the new front-end circuit (preamplifier and comparator) and the feasibility to implement a high resolution TDC per pixel.

In line with the present results we discuss system requirements and a list of specifications for a final large size chip.

I. Introduction

With the invention of Micro-Pattern Gas Detectors (MPGD), in particular the Gas Electron Multiplier (GEM) and the Micro-Mesh Gaseous Structure (Micromegas), the Integrated Grid on chip offers the potential to develop new gaseous detectors with unprecedented spatial resolution, high rate capability, large sensitive area, operational stability and radiation hardness. Modern wafer post-processing techniques allow the integration of gas-amplification structures directly on top of a pixel readout chip. Thanks to these recent developments, particle detection through the ionization of gas has a large field of applications in future particle, nuclear and astro-particle physics experiments with and without accelerators [1].

A CMOS pixel chip can be assembled directly below the GEM or Micromegas amplification structure (see Fig.1) and serve as an integrated charge collecting anode. With this arrangement electrons generated in an avalanche, are collected on the top metal layer of the CMOS chip; every input pixel is then directly connected to the amplification, digitization and sparcification circuits, integrated in the underlying active layers of the CMOS technology. Using this approach, gas detectors can reach the level of integration density typical of solid-state pixel devices.

A number of research groups have expressed interest in exploring the potential of the pixel readout of gas detectors. At the same time there is interest in the High Energy Physics tracking community and in the Medipix Collaboration for a general purpose readout chip with similar characteristics. All users require a pixel cell providing simultaneously both energy and hit time information and a readout architecture which would allow the chip to be triggered externally. Given the resources needed for such a development it is beneficial that a chip could be designed that satisfies as many users as possible.
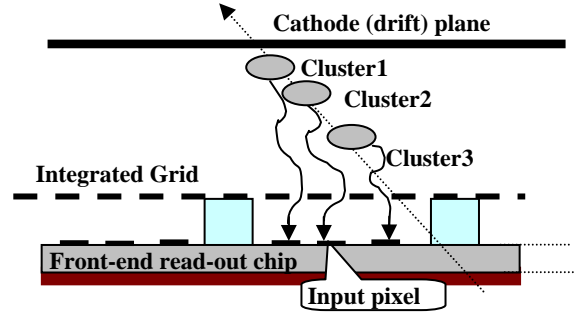

Figure 1: Layout of the micro-pattern gas detector with the amplification structure based on an integrated grid.

II. Prototypes: experimental results.

A number of prototypes of the front-end readout chip have been developed with the purpose to demonstrate performance of MPGDs and to characterize the basic circuits.

A. The Timepix chip.

The Timepix is a full size chip designed at CERN in 0.25μm CMOS technology [2]. Detection area of the chip is a matrix 256 by 256 pixels with a pitch of 55μm. This circuit allows for measurements of charge arrival times for each pixel individually with 10-ns accuracy. This feature makes 3D track reconstruction possible. Figure 2 demonstrates spiral tracks of low-energy electrons in a magnetic field taken with the Timepix chip.
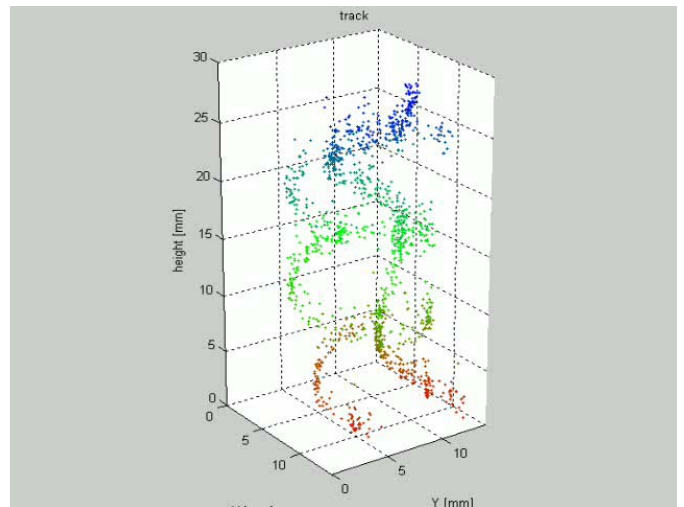

Figure 2: Spiral tracks of low-energy electrons in a magnetic field.

B. GOSSIPO-1 chip.

GOSSIPO-1 chip [3] was developed at NIKHEF in 2005 in 0.13μm CMOS technology and it contained the prototype of the front-end circuit. The main goal was to demonstrate that a detector with low parasitic capacitance (~20fF) and no sensor leakage current would let us design a fast response time (less than 40-ns peaking time), low-noise (ENC is 70-e$^-$ RMS) and low-power (2-μw per channel) front-end circuit.

C. GOSSIPO-2 chip.

Gossipo-2 chip (see Figure 3) was a small-area pixel readout array consisting of 16 by 16 pixels with a pitch of 55μm [4]. The main goal of this chip was to prototype a high resolution and low-power TDC-per-pixel architecture, based on a switched local oscillator running at 600MHz. The circuit uses an external 40MHz clock as time reference. For detail characterization a separate TDC block and an oscillator circuit have also been placed on the chip.
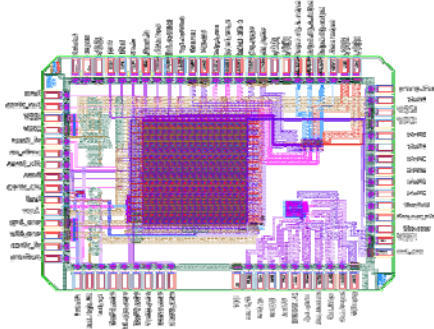

Figure 3: Layout of GOSSIPO-2 chip.

III. Characterization of basic blocks.

A. Time-to-digital converter.

The TDC consists of a local oscillator circuit, a 4-bit fast clock counter and a 4-bit (system) clock synchronous counter (see Figure 4).
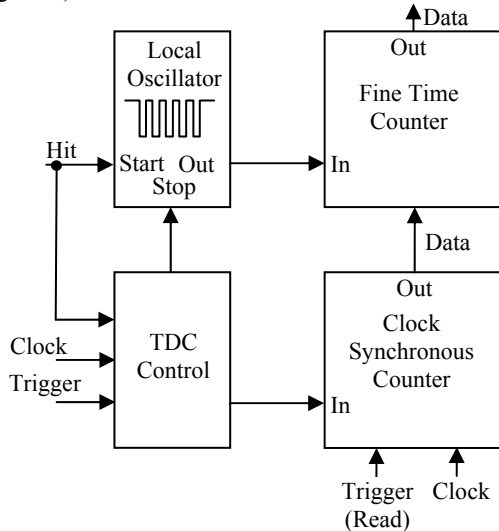

Figure 4: Block diagram of the TDC circuit.

The local oscillator (F^{fine} = 560MHz) will be started by the Hit signal and will be stopped by the coming leading edge of the clock signal (F^{coarse} = 40MHz) (see Figure 5). The number of the "fine" clocks will be counted as well as the number of "coarse" clocks until the trigger signal appears. The data is two 4-bit words representing the final state of the counters.
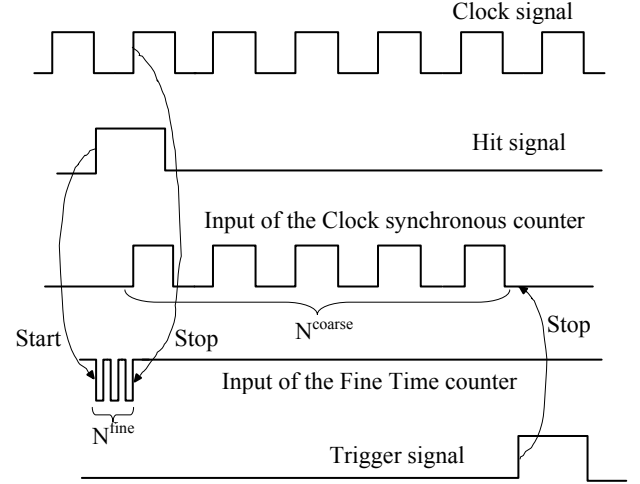

Figure 4: Signals in the TDC circuit.

The converter output code as function of the Hit signal delay is in Figure 5. The time resolution of the TDC (1.8ns) is determined by the frequency of the local oscillator. The dynamic range is set by the frequency of the clock signal and the length of the clock counter. The average TDC power consumption depends on the rate of the Hit signal. For the rate of a 100kHz (for LHC experiments) it is about 0.4μW.
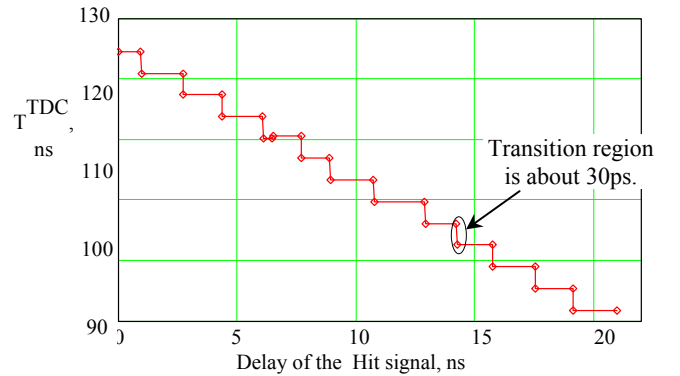

Figure 5. The output of the TDC circuit as function of the delay of the Hit signal.

B. Local oscillator.

The local oscillator circuit includes a NAND gate with a chain of inverters in the feedback (see Fig.6). A positive signal at the input triggers the logic and the circuit will start to oscillate at the frequency determined by the delay in the feedback. The oscillation frequency (560MHz) is 14 times higher than the clock frequency (40MHz). This means that 14 oscillator cycles are within one clock period and that the position of the leading edge of the input pulse can be determined with an accuracy of 1.8ns.
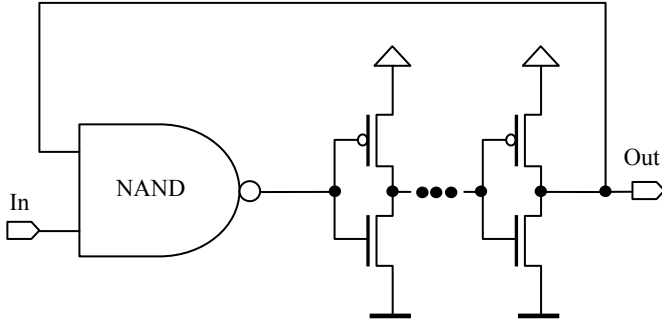
Figure 6. Schematic of the local oscillator circuit.

The gate delay of the CMOS inverters is very sensitive to variations in the temperature, power supply voltage. We have carried out a careful study of the stability of the oscillator frequency. Measurements show that the period of the oscillations is directly proportional to the temperature, with a slope of 2% per 10ºC, and inversely proportional to the power supply voltage, with the slope of -12% per 100mV. This is in agreement with simulations. We conclude thus that variations over temperature within 30ºC or variations over power supply voltage within 50mV will lead to a 6% shift of the frequency. This is tolerable as it results in less than one oscillator cycle within one clock period (25ns) and, therefore, is not visible in this type of TDC.

Transistor mismatch will lead to spread of the value of the delays across the channels. Any tuning solutions are usually unwelcome. In the present design the channel-to-channel spread of the value is 4% which is less than the width of the bin of one TDC. It is possible to reduce the spread by means of resizing of the transistors. However it will lead to the increase of power consumption and the area on the chip.

C: Experimental results; time resolution under various conditions.

In order to estimate time resolution of the complete read-out chain (see Figure 7) we measured the time interval between the Test- and the Trigger (Read) signal. Figure 8 represents results of the measurements of this time interval as function of the threshold value at different input signal sizes. In order to get the best time resolution we should position the threshold just above the noise (350e$^-$). Under this condition the time jitter will be 4 bins of the TDC (7.2 ns) for small signals (1200e$^-$). For larger signals (3000e$^-$) the jitter will be lower 2 bins (3.6ns) and for signals as large as 12000e$^-$ the jitter will be kept within 1 bin (1.8ns).
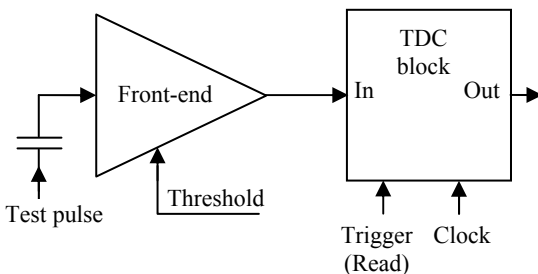

Figure 7: Block diagram of the complete readout chain, including the front-end circuit and the TDC block.
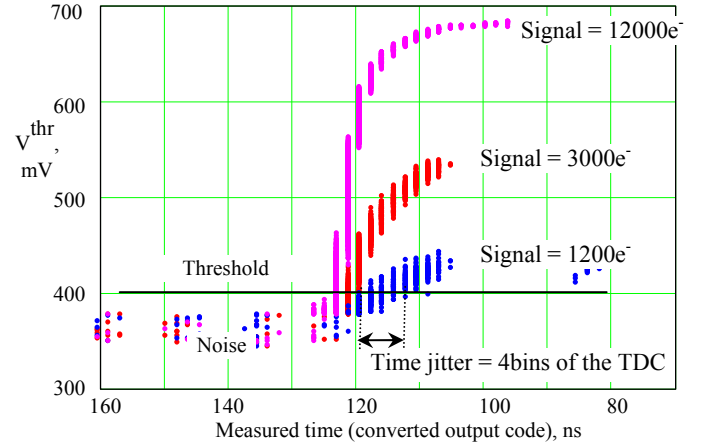

Figure 8: Measured time (converted output code) as a function of the threshold value at different input signal.

We also did a time scan in the complete read-out chain that covers the dynamic range of the TDC. We shifted the Hit signal in respect the Trigger and monitored the output code. Figure 9 presents result of the measurement under the following conditions: signal size is 4000e$^-$ and the threshold is 350e$^-$. In this case the transition region (from one TDC bin to the next) is quite narrow (1ns) and less than 1 TDC bin.
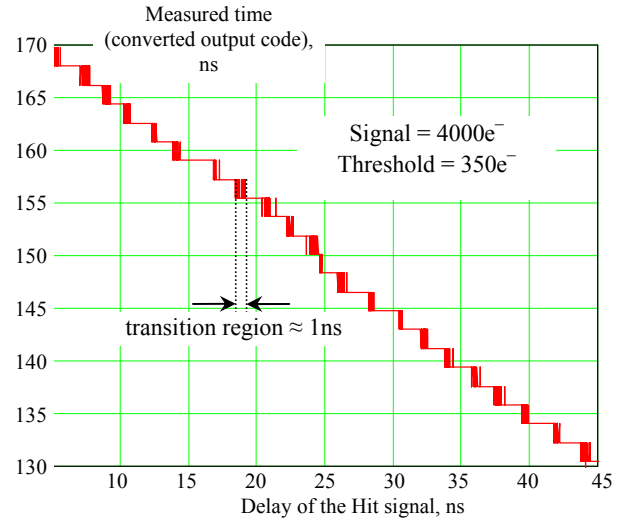

Figure 9: Measured time (converted output code) as function of the delay of the Hit signal.

IV. Main specifications for Timepix2 - general purpose readout chip for micro-pattern gas detectors.

It has been proposed within the RD51 collaboration that a new general purpose front-end chip is required for readout of micro-pattern gas detectors. The chip should meet requirements imposed by the groups developing TPC's (time projection chambers), GOSSIP (gas on slimmed silicon pixel

detectors) and the large-area drift chambers. Moreover the chip should be suitable for readout of silicon-sensor based detectors. The chip would be developed in 0.13μm CMOS technology. Designers from CERN, NIKHEF (Amsterdam), Bonn and Saclay have expressed their interest in this work. The chip would have sensitive area of a 14mm by 14mm (1.98cm^2). It will be a matrix of 256 by 256 pixels with the pitch of a 55μm. Only single pixel operation is foreseen. There should be low input referred noise level (70e$^-$) which will allow for low threshold operation (350e$^-$). Every pixel will be equipped with a high resolution TDC making possible the measurement of the arrival time with an accuracy of about 2ns. The dynamic range of the TDC is not defined yet. It is also required to deliver information on charge deposited to the pixel.

There should be a local (on-pixel) memory for storing data generated by multiple hits in the time until the trigger signal arrives.

The following readout modes are required:

- all pixel readout (time frame based) with zero suppression

- readout of the data associated with a trigger (for LHC like experiments)

- event driven readout .

Data taking and data readout should be independent and run in parallel driven by a 40MHz external clock. For readout a fast serial link (≥1Gb/s) is needed.

V. Summary

A new front-end chip is required for readout of micro-pattern gas detectors (MPGDs).

It should be also suitable for detectors employing Silicon sensors.

A number of prototypes have been fabricated successfully in order to verify the performance of the basic circuits.

The TDC per pixel with local oscillator satisfies the design requirements: low power consumption (0.4μW/channel with 100kHz hit rate), high time resolution (1.8 ns bin) and simplicity. It demonstrates low crosstalk to the sensitive inputs.

Low threshold (350 e$^-$) and fast peaking time (20 ns) enable for high quality drift time measurements (jitters 1.8 ns) at large input signals (>4000 e$^-$) and after accurate threshold equalization.

Work on the technical specifications and the definition of the structure for a new MPGD chip has started.

VI. References.

[1] Maxim Titov, "New developments and future perspectives of gaseous detectors", Nucl. Instr. and Methods, A581 (2007), pp. 25-37

[2] X. Llopart et al, "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements". Nucl. Instr. and Methods, A581 (2007), pp. 485-494

[3] V.Gromov, R.Kluit, H. van der Graaf, "Prototype of the Front-end Circuit for the GOSSIP (Gas On slimmed Silicon Pixel) Chip in 0.13μm CMOS Technology", Proceedings of the Twelfth Workshop on Electronics for LHC and Future Experiments, Valencia, Spain, 25-29 September 2006.

[4] R.Kluit, V.Gromov, H. van der Graaf, "Development of a Small-scale Prototype of the GOSSIP chip in 0.13μm CMOS Technology", Proceedings of the Topical Workshop on Electronics for Particle Physics, Prague, Czech Republic, 3-7 September 2007.