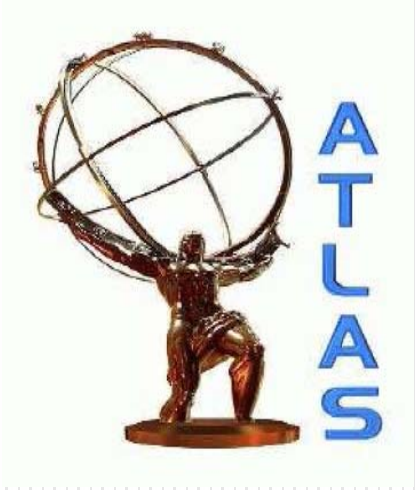
SLHC Upgrade Plans for the Atlas Pixel Detector



TWEPP 2008 Naxos, Greece

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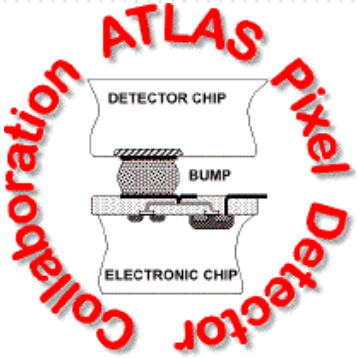
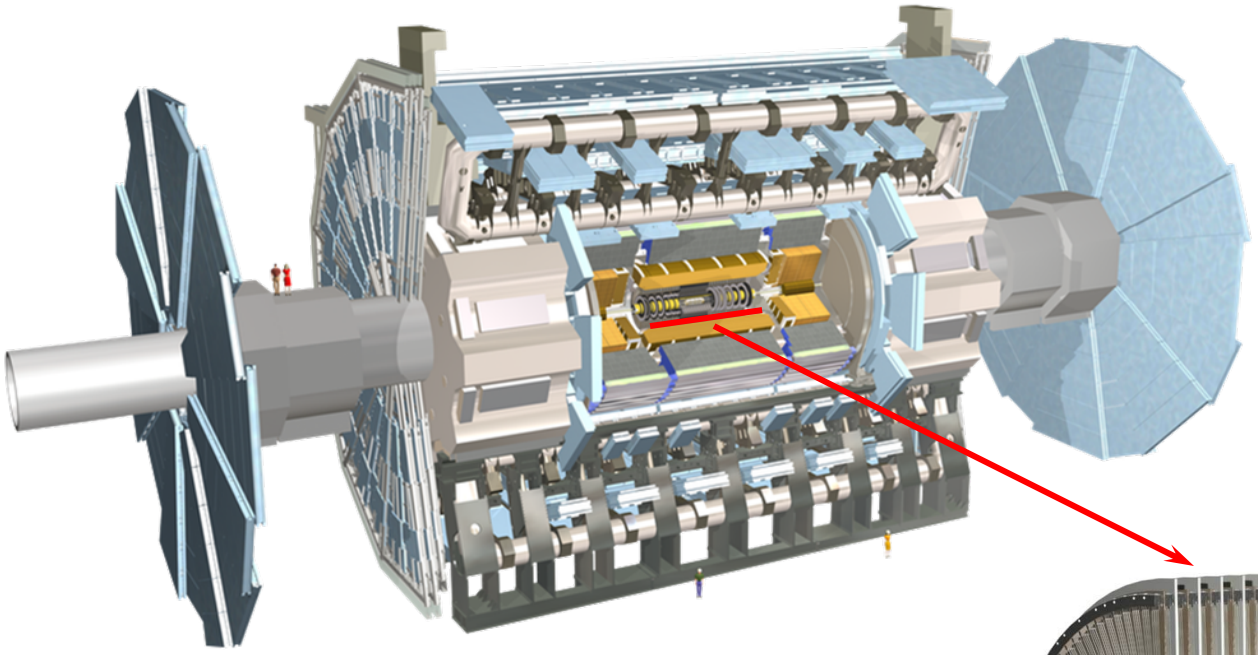
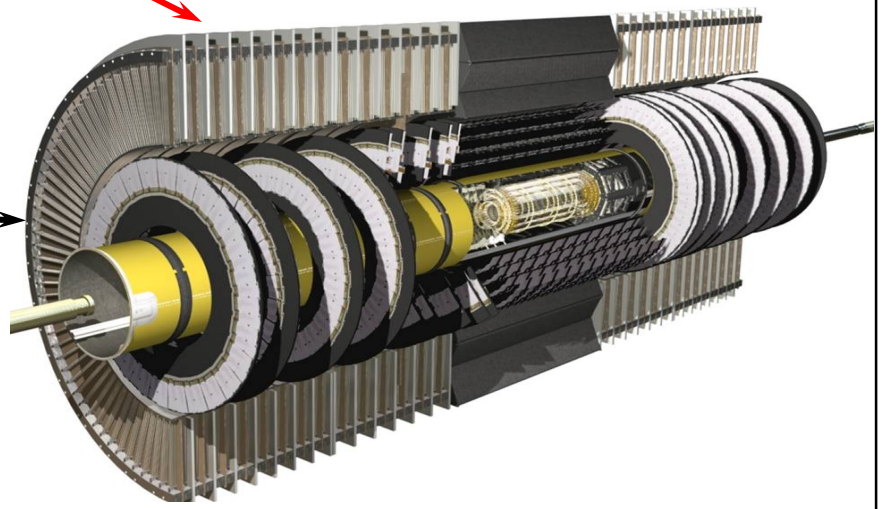


Pixel detector in the heart of Atlas



Atlas Detector

- Length 46m
- Φ22m
- 7000 tones
- ☺ ***First beam circulation 10th September 2008!***



Inner Detector of Atlas

(to be replaced completely for SLHC)

(7m long; Φ2,3m)

- TRT
- SCT
- Pixels

Pixel Package and the Pixel Detector

Pixel package

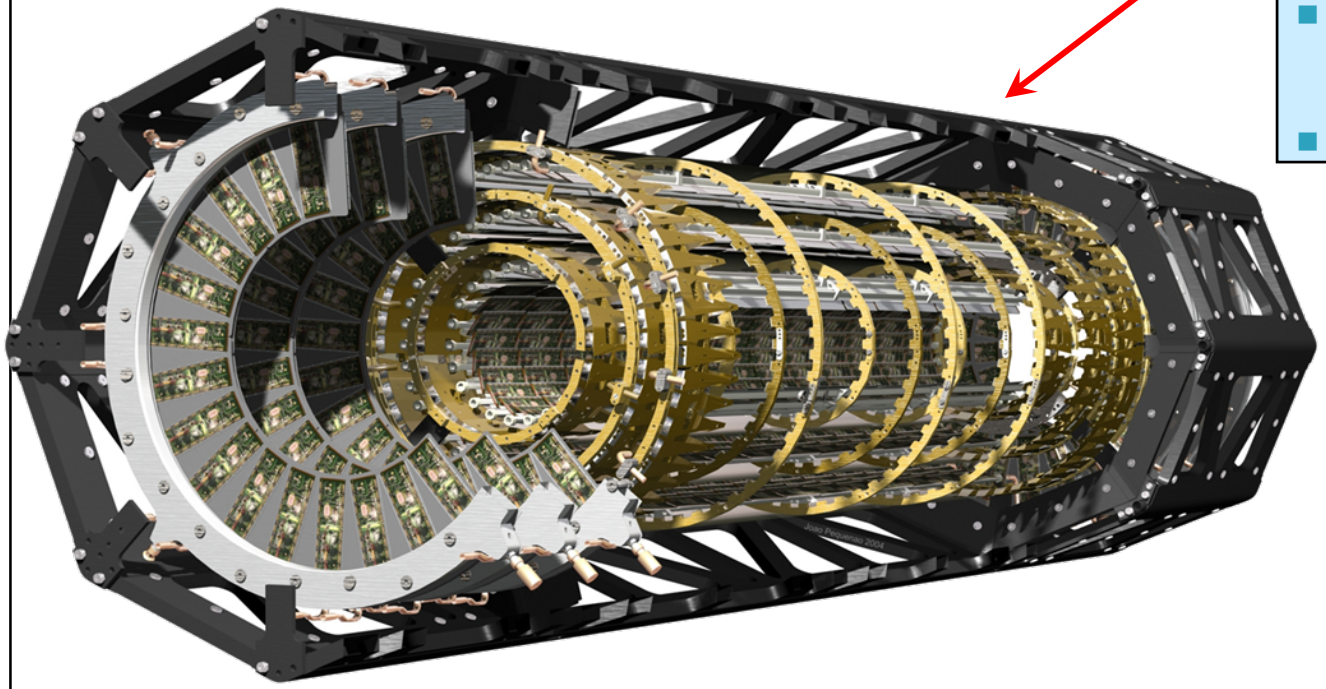
- Full length 7m, (includes services)

SQP + Beam Pipe Support Structure

Pixel Detector

SQP + Beam Pipe Support Structure

Connection of cables and pipes (PP1)



Pixel detector

- *3 barrel layers* at R5, 9, 12cm from IP
- *3 disks* at each side

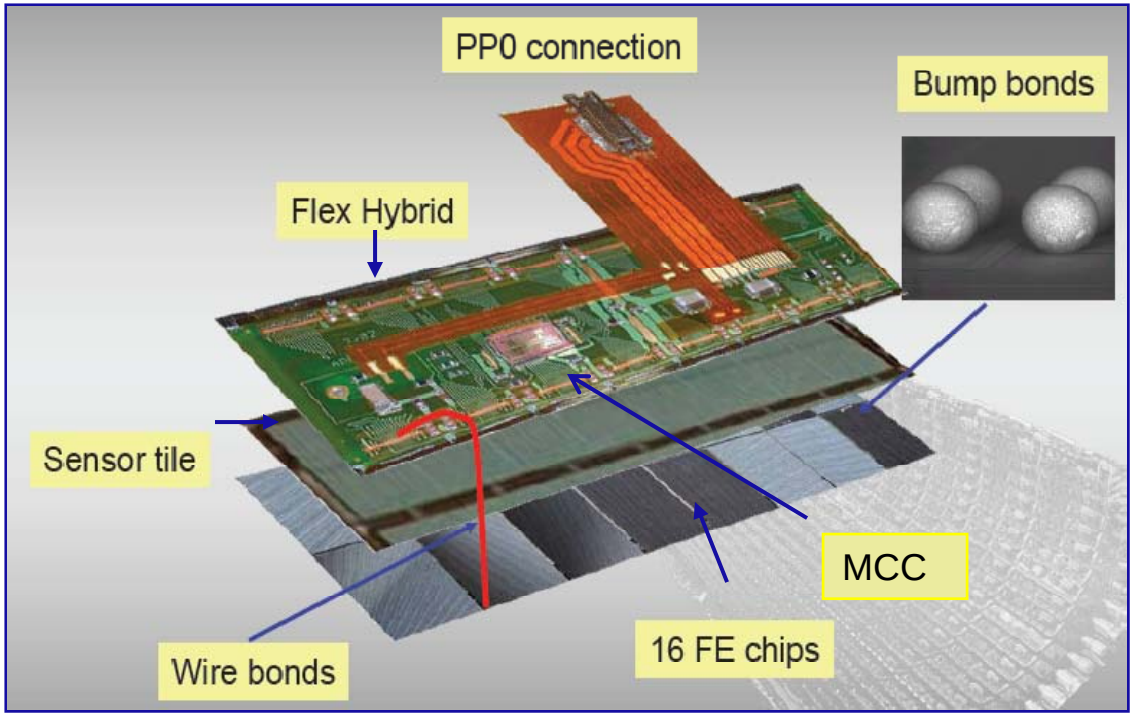
- Tracking volume: 1.6m long, 0.2m radius 1.8m^2 of silicon in total
- 1744 modules

  ~ 80 millions channels
- Good d_0 and z_0 resolution *(12μm and 70μm)* crucial for physics program
- Use evaporative cooling to remove 10 kW of power and operating temperature ~ -5°C

Pixel module – basic element of Pixel Detector

Pixel Module – short description:

- Each module has 46080 pixels in an area of ~10 cm^2 (1.6 x 6 cm)
- Sensors tile are arrays of pixel diodes (***n+*** on ***n*** substrate)
- Pixel size is 50 x 400 μm
- Silicon sensors bump-bonded to 16 FE chips (~12 μm bumps)
- FE chips are connected to one controller chip via wire bonding and flex hybrid
- Micro-cable (~1m) connected to service patch panel (PP0 connection)
- Modules are placed on carbon fiber cooling/support structure
- Data transmission trough optical links



What is the implication for the Pixels at SLHC?

What are Super Luminosity LHC highlights?

- SLHC ($\sqrt{s} \approx 14$ TeV, $L \approx 10^{35}$ cm^{-2} s^{-1}) would allow to extend significantly the LHC physics aims whilst keeping the same tunnel, machine dipoles and large part of "existing" detectors.
- Note please - Integrated luminosity at SLHC will reach ~300 fb^{-1} per year!

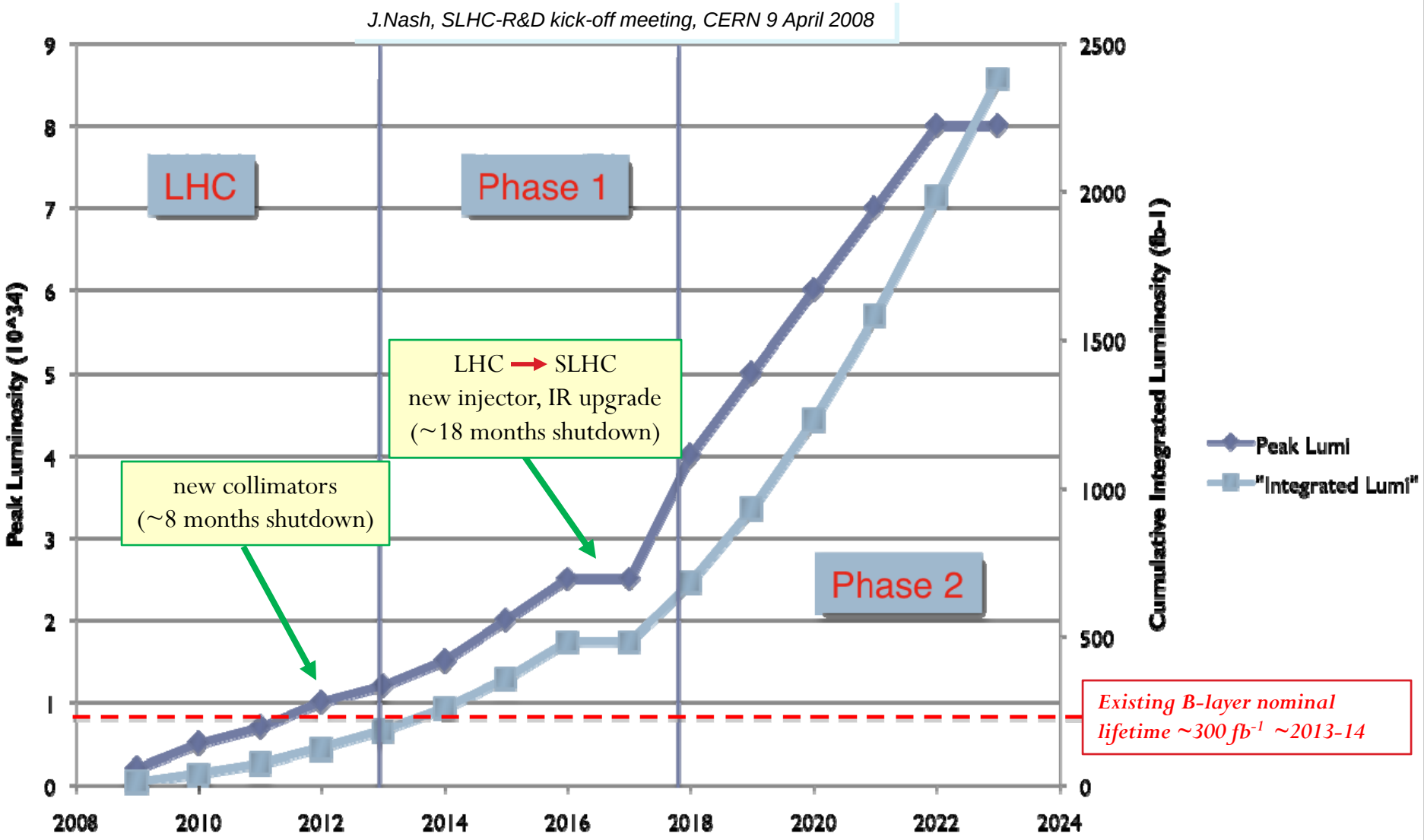
What are requirements for trackers?

- SLHC - Entire Inner detector has to be replaced by new one
- Trackers need more channels to achieve the same performance with much higher occupancy. Higher Granularity needed! . Expectation of 5-10ktracks/event, pile-up up to 400events / BC!
- Trackers need improved radiation hardness for electronics and especially for sensors !
- Generally, inner/forward parts of LHC detectors must be changed-hardened-upgraded
  - Electronics (FE chips)– able to cope with very high data rate. Certainly more channels are needed (80M – 160M) - pixel size must be significantly decreased, threshold must be further decreased !
  - Radiation hard sensors needed to survive at fluence well above 10^{16} n_{eq}/cm^2
- Substantial R&D in many different areas is required, keeping in mind LHC detectors development, production and qualification time. We have to say – time schedule for SLHC tracker upgrade is very aggressive!
- Obviously simulation will play an important role in design definition
- SCT and Pixel commonalities should be explored and used whenever possible; (example "Architecture of the Read-out Electronics for the ATLAS Upgraded Tracker" ATL-P-EN-0001; G. Darbo, P. Farthouat, A. Grillo)

Schedule?

- LHC needs to do a major replacement of quadrupolest in interaction regions after an integrated luminosity of ~600 fb^{-1} (2016/2017), detectors to be upgraded same time….

LHC → SLHC Luminosity upgrade scenario



Which parts of Pixel detector are concerned? Goals?

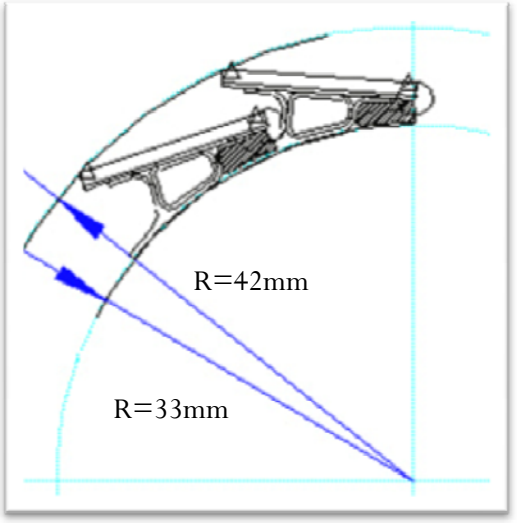
Primary items

- ***Sensors*** *(more details on next slides)*
- ***FE chips*** *(more details on next slides and also see for details talk of M.Karagounis)*
- ***Detector Layout*** - overall ID layout changed – 100m^2 of silicon in total - Pixels about 6,5m^2. There are many challenging discussions and proposals last moths…, it looks that we converge to a 4 hit system for $|\eta| \leq 2.5$ with 4 barrel layers (2 inner layers likely insertable) at radii ~3,7 to ~20cm and 3 disks at each side.
- ***Module architecture*** – if sensors with active edges are available there is no reason to have multichip module for inner layers (significant cost reduction), module size with reduced inactive edges (wire bonds only at one side of the module). The outer layers with 2x2 chips on the module likely. The general aim isto reduce material budget further – thinner FE-chips and sensors, reduced cabling… Module Control Chip not considered – likely to be replaced by Stave Control Chip (Stave end Card)
- ***Powering scheme*** to be changed, is not realistic keeping about the same amount of recent services for detector with double number of channels, material budget issue (DC-DC or serial powering, both options are investigated) – *for more details see talk of M. Weber*
- ***R/O Architecture*** (common issue with SCT)
- ***Optical links*** (higher data transmission speed)
- ***DCS*** (Detector Control System, local DCS control chip at stave/sector level)
- ***Mechanics***
- ***Cooling*** (recently ~ -5degr.C, for SLHC tracker regions considered coolant temperatures even up to -35degr.C, general trend is to replace C3F8 system with CO2)

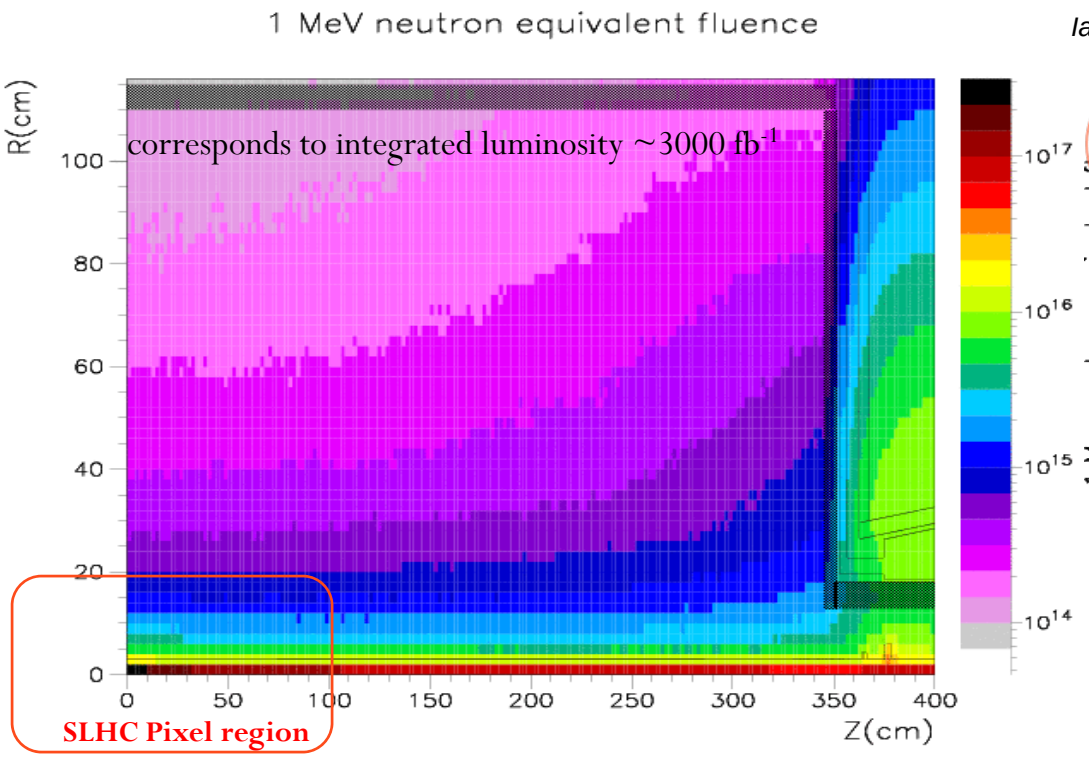
Innermost Pixel B-physics layer replacement – intermediate step on the way to SLHC

- LHC will increase substantially (~2x) its nominal luminosity even before upgrading to SLHC
- The innermost pixel layer (B-physics layer) very probably would not survive with reasonable tracking efficiency until the LHC/SLHC upgrade (expected 2016-17)
- Present B layer is not designed for luminosities above $L \approx 2 \cdot 10^{34}$ cm^{-2} s^{-1}
  $\Rightarrow$ granularity issue – deteriorating of efficiency is starting
- Present B-layer is designed to survive NIEL fluence ~10^{15} neq/cm^2 and Ionizing Dose = 500 kGy (corresponds to LHC integrated luminosity ~300 fb^{-1})
- There is a proposal to upgrade present B layer even before SLHC upgrade, probably during shutdown 2012/2013 (6-8 months)
- Certainly given short time does not allow to remove complete "pixel package" to the surface and then replace B-layer (long cool down time expected!)
- The idea is to insert additional new B-layer together with new beam pipe of reduced size without removing pixels package out of Atlas (of course, old beam pipe to be removed before!)
- There are not yet final decisions concerning B-layer upgrade/replacement, expected in coming weeks ….

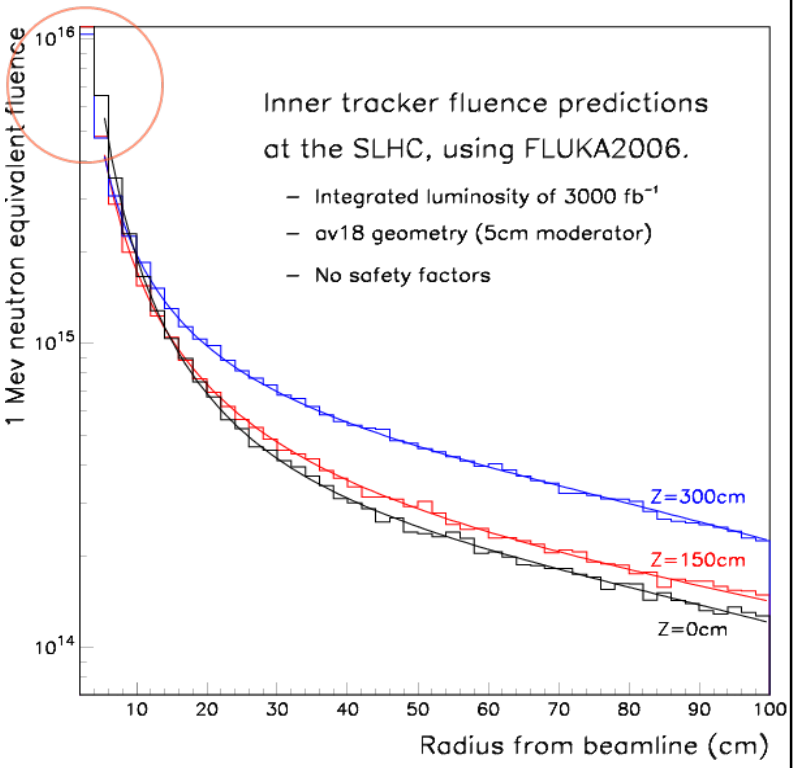
New B-layer
(16 staves, not shingled)



Expected Radiation levels in ID region



Ian Dawson, Valencia Tracker Upgrade Workshop Nov, 2007

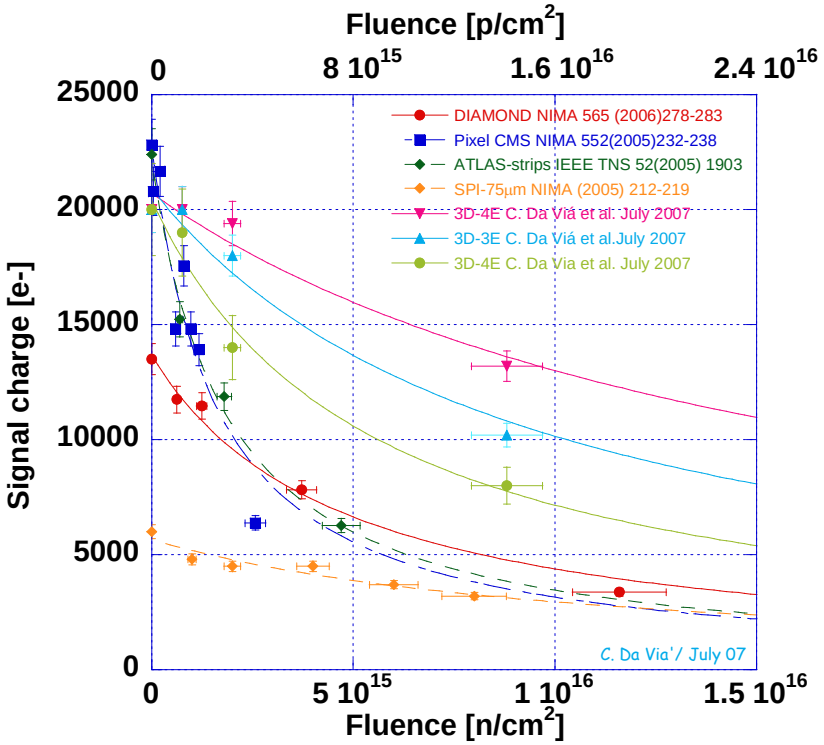


- Fluences at small radii dominated by particles from interaction point - mainly pions, (no shielding possibility)

Sensors - the most critical parts for SLHC trackers

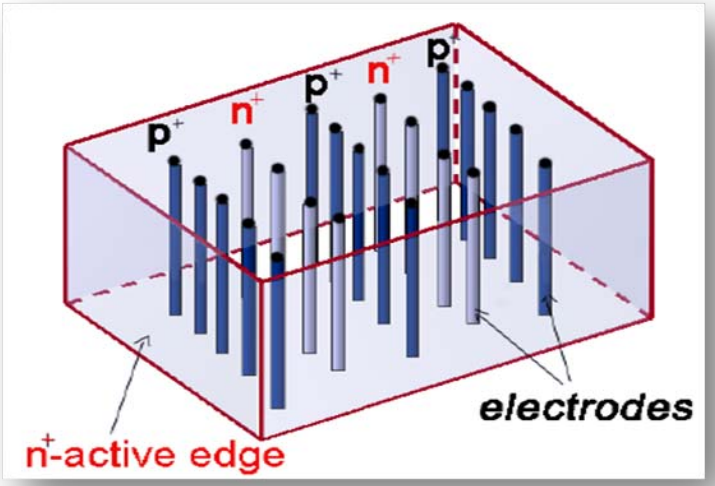
What are issues of present silicon pixel sensors?

- SLHC resulting fluence for innermost layer is expected up to $2 \cdot 10^{16}$ n_{eq}/cm^2
- Resent n-in-n pixel detector is proved to be radiation hard up to $2 \cdot 10^{15}$ n_{eq}/cm^2, behind this fluence sensor gives still some charge however charge trapping plays significant role and deteriorating of CCE is dominant
- Huge leakage current – risk of thermal runaway
- Increase of full depletion voltage (>1000V) – under-depleted operation to be considered (lower efficiency, worsening of resolution,..)
- We may consider for the innermost Pixel layer(s) extremely high radiation sensors as 3D or diamond and for larger radii improved n-in-n ("our standard sensor") or more likely n-in-p (probably the cheapest sensors…)
- Total Pixel are about 5-6m^2
- There are also other options a thin sensors, Gossip,…



R&D on Silicon Sensors for SLHC – 3D sensors

- Firstly introduced ~1995 (S.Parker), however this new detector concept was not proved that time to be seriously considered for Atlas Pixel detector at LHC..
- Tiny highly doped p+ and n+ electrodes (~ Φ10μm) are processed (etched) inside the detector bulk instead of being implanted on the wafer's surface (SINTEF, Stanford lab, recently more labs involved - CNM/Valencia Spain, ,ICEMos, Ireland, IRST Italy)
- Up to recent 3D technology was quite challenging, many technological issues have been solved, and possible large scale production can be considered…



- The 3D collaboration is growing up and the plans are very ambitious but realistic. 3D pixel module is in production recently, should be ready for testbeam in Nov 2008, pixel stave is planed for 2009!
- Extensive testbeam activity (test beam June, November 2008 – focused to active edge, modules, samples from different companies, samples with design modification 2E, 3E, 4E, etc)
- "The primary goal is the development, fabrication, characterization, and testing, with and without the front-end readout chip, of Full-3D – active-edge and Mod-3D silicon pixel sensors of extreme radiation hardness and high speed for the SLHC ATLAS upgrade and, possibly, the ATLAS B-layer replacement. A secondary goal is to start design work for a reduced material B-layer detector module using these sensors" *Cinzia Da Via, 2008*

R&D on Silicon Sensors for SLHC - 3D sensors (2)

3D active edge silicon sensors – main features, constraints *(ref. Cinzia Da Via Barcelona Apr 2008, APU workshop, CERN,June 2008)*

☺ Tiny highly doped p+ and n+ electrodes (~ Φ10μm) are processed inside the detector bulk instead of being implanted on the wafer's surface

☺ The edge of sensor is an electrode, dead volume at the edge < 5 microns!

☺ Short collection distance, high average E field at low bias, long charge deposition distance

☺ Layout with alternating rows of p+ and n+ columns produces very fast charge collection reducing the impact of charge trapping

☺ Extreme radiation hardness: S/N >20 and collected charge >13ke$^-$ at fluence close to $2 \cdot 10^{16}$ neq/cm2

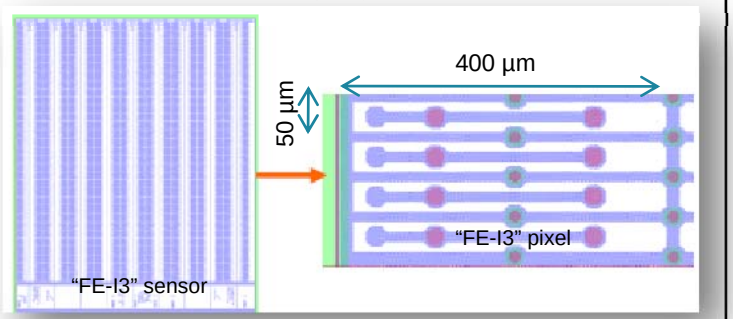
☺ 3D pixel module in production recently, should be ready for testbeam in Nov 2008, stave planed for 2009

☹ Technical challenges of building detectors, production yield, cost??

☹ Efficiency in low field areas (highly doped columns)

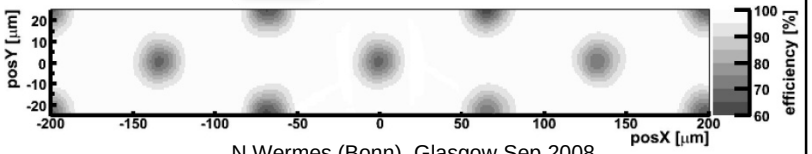
☹ Higher capacitance – greater demands on FE electronics

2 electrodes of n-type, p-substrate (2E design)



R&D on Silicon Sensors for SLHC - 3D sensors (3)

➢ Some impressive processing images and testbeam plots provided by 3D Pixels ATLAS collaboration



N.Wermes (Bonn), Glasgow Sep 2008

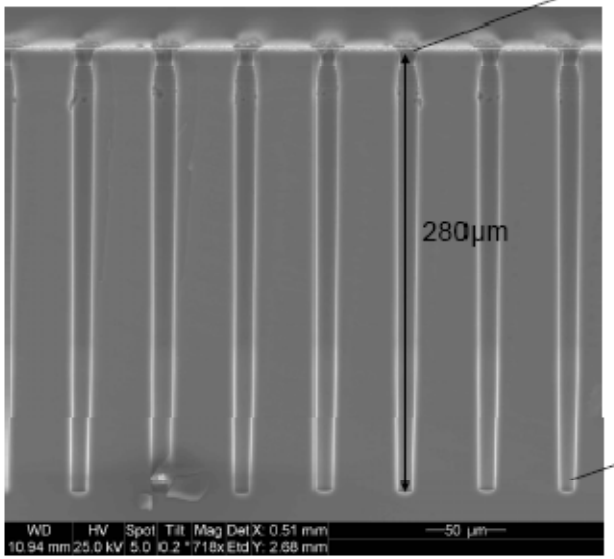
✓ Deep Reactive Ion Etching (DRIE) results at SINTEF

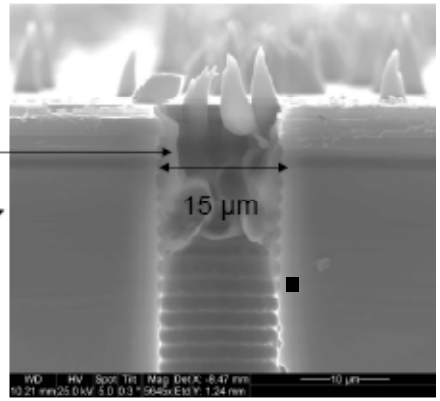
SINTEF 3D

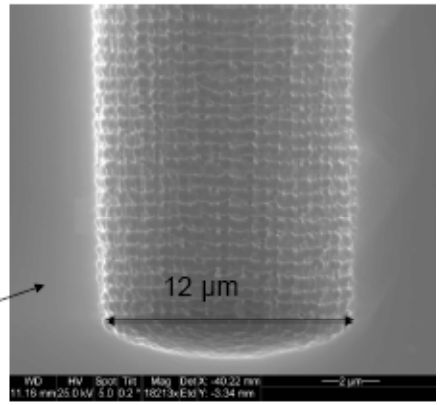
Latest DRIE results from the new Alcatel I-Speeder etcher

Etch rate 7µm/min

Polymer after etching



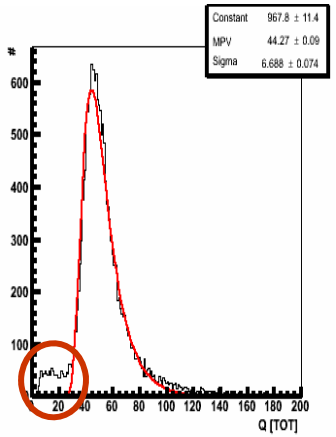




Testbeam data analysis (2006)

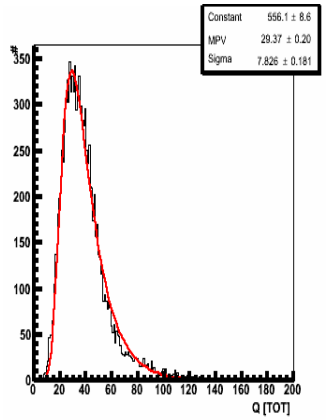
beam → 0°

ε = (95.9 ± 0.1) %



beam → 15°

ε = (99.9 ± 0.1) %



Testbeam data 2006,
M. Mathes, M. Cristinziani (Uni Bonn)
S. Watts (Manchester) and others...

R&D on Silicon Sensors for SLHC

Planar Pixel sensors R&D for the Atlas Upgrade

- There are still many options and many open questions…
- Bulk material? n-type or p-type? n-bulk is proven technology of recent Atlas pixel sensors
  p-bulk (designated for SCT upgrade) does not invert with high radiation therefore processing is much easier and less costly due to one side processing only, the price will have certainly high impact to final decisions…
- Thin sensors of about 75μm thick (standard thickness 250μm) either n-in-n or n-in-p
  After a fluence of $5 \cdot 10^{15}$ n_{eq}/cm^2 U_{fd} ~150V vs ~1600V of standard sensors 250μm thick, the charge about the same, bulk reverse current reduced, charge collection faster, charge trapping effects reduced. Also Si material budget advantage is not negligible. Disadvantages: More costly processing of thin wafer, low signal from the beginning of operation (~3300e^- @ 75μm) *(ref. Michael Beimforde, Valencia 2007)*
- New design of detector edges is required to reduce inactive areas (GR areas). Active/Slim edges are desired - inactive edges have to shrink from ~1100μm to ~100μm, also trying to avoid crystal damaging cutting methods
- Planar p-bulk (n-in-p) sensors would be probably very cost attractive solution, but for outer layers likely…

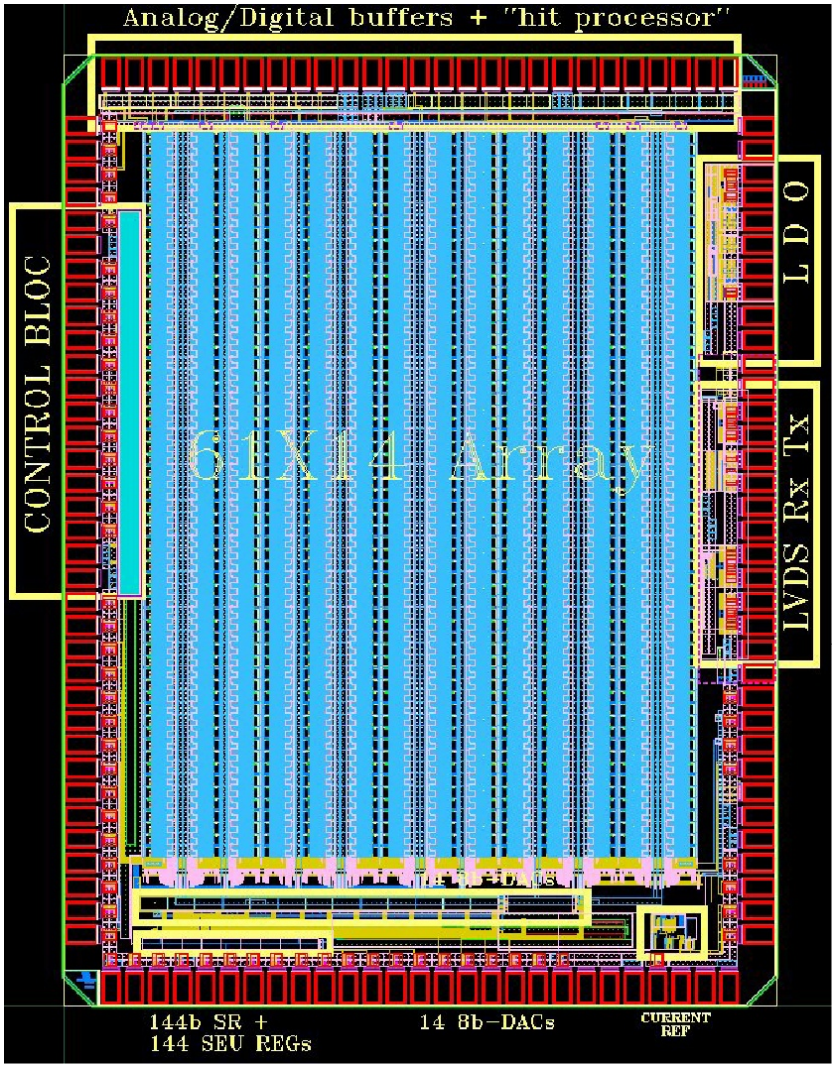
New Atlas Pixel FE-I4 chip – goals and issues

- IBM 0,13µm CMOS technology (CMOS8RF)
- Increase the chip size (7,6 x 10,8mm at FE-I3 to 16,8 x 20,2mm at FE-I4)
- Improve active area over inactive area (74% to 89%)
- Cope with high hit rate. The digital architecture logic is completely redesigned, not based on End-of-Column data buffering (FE-3) but on local pixel logic and local pixel data storage.
- Reduce the pixel size (50x400 µm to 50x250 µm)
- We are keeping the same pitch of 50 µm considering sensor issues (3D, insulation implants etc)
- Reduce power (385 to 240mW)
- New analog pixel chain tuned for low power and higher detector input capacitance (3D sensors, under depleted sensors, etc.)
- Serial data output rate of the chip - design target value is 160Mb/s
- Radiation hardness does not look as serious issue (Vt shift seems to be much lower at 0,13 µm comparing with 0,25 µm of present FE-I3 chips). Samples of ProtoI FE-I4 irradiated to 2MGy are tested recently
- Before starting with design of full size FE-I4 (80r x 336c) following things have to be taken into account:
  - System architecture including DCS, ROD and Opto-links
  - Testing (wafer level, irradiation and test beam)
  - Sensors design issues…

FE-4 ProtoI chip (3x4mm)

Ref .Roberto Becherle PGUM June 2008

- Submitted in March, should be delivered in July (MPW run through Cern contract with MOSIS)
- Analog measurements and logical functionality of all the blocks should give substantial answers to open questions before proceeding to the full size chip FE-I4 (16,2 x 18,7mm)
- Chip is suitable for doing radiation measurement and SEU test
- FE-I4 Proto I chip - Array of 61 x 14 cells



FE-I4 Main features

Pixel size	50um x 250um
Number of rows	324
Number of columns	64
Edge bumps to physical edge	125um
Bottom of chip	2.4mm
Maximum operating voltage	1.5V
Nominal (max) analog current /pixel	10 (18) uA
Nominal (max) digital current /pixel	10 (15) uA

LHC – BLR - SLHC transition

- In spring 2008 submitted 3 test chips in IBM 0,13um techn. Through MOSIS (received back in July), in particular:
  - Analog pixel array, 60 rows x 13 columns
    - Contains also digital command decoder and power circuits
  - LVDS transceiver chip
  - SEU register test chip
- Next step is submission of full size FE-I4 (recently used FE-I3 in Atlas)
  - LHC →FE-I3 organized as matrix 18 columns x 160 rows, cell size 50x400µm
  - BLR →FE-I4 organized as matrix 80 columns x 336 rows, cell size 50x250µm
  - SLHC→FE-I5? Likely further cell size reduction; 50x200µm is small enough??
- We tried to optimize the FE-4 size (16,2 x 20,2mm) with the respect to overall coast per module (considering 6" sensor wafer with 6 module tiles, flip chipping), already close to vendor limits!
- EOC buffers have to spread out over the pixel area (certain number of pixels sharing buffers)
- No MCC planned for BLR (some functionality moved to FE chip)

FE-4 main parameters

Chip size	16,2 x 20,2	mm
Array size	80 x 336	Pixel (col x row)
Pixel size	50 x 250	μm^2
Bump pad diameter	12	µm
Input	DC couple negative signal	
Pixel inp cap range	300-500 (450-700 long pixels)	fF
Two hit discr. time (same pixel hit)	400	ns
In time threshold with 20ns gate	4000	e
Tuned threshold dispersion	100	e
DC leakage curret tolerance	100	nA
Single channel ENC sigma (400fF)	300	e
Operating voltage range	1,2 – 1,5	V
Total analog supply current (400fF)	10	µA/pixel
Total digital supply current (100kHz)	10	µA/pixel
Average hit rate	200	MHz/cm^2
Data driven with time stamp (8 bit res.)		
Single chip data output rate	160	Mb/s
Maximum Trigger rate (readout initiation)	200	kHz
Charge resolution	4	bit

Serial output date rate at LHC and SLHC

Radius (cm)	Ev./BC	Hits/FE-I3 Module	Pix Size	Hits/FE	Bit/Hit	FE-I3 (Mb/s)	FE-I4 (Mb/s)
3.7	24	38.7	50x250	2.42	26	6.3	25.2
3.7	50	77.0	50x250	4.81	26	12.5	50.1
3.7	400	572.0	50x250	35.75	26	93.0	371.8
5.05	24	20.5	50x400	1.28	26	3.3	13.3
5.05	400	*300.0*	50x400	18.75	26	48.8	195.0
8.85	400	*122.0*	50x400	7.63	26	19.8	79.3
12.25	400	*74.0*	50x400	4.63	26	12.0	48.1
Module Size:	~60x16 mm2		Simulated 50x250 µm2 pixels @ 3.7 cm				
FE-I3/module:	16		Simulated 50x400 µm2 pixels @ 3.7 cm				
FE-I4/module	4						
No.bit/hit:	26						

Roberto Becherle Vertex August 2008

Pixel FE design group

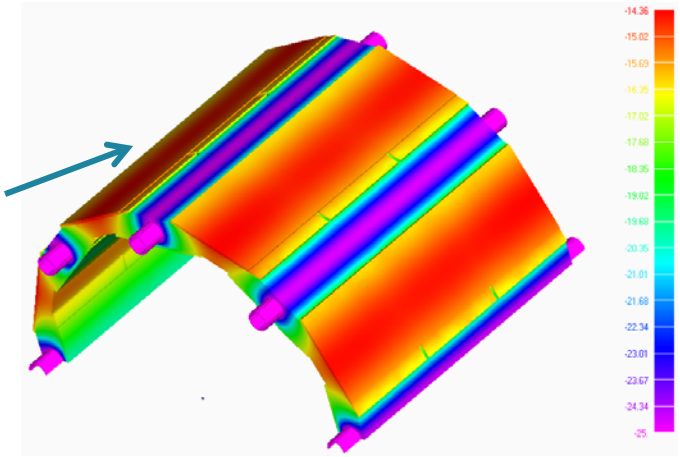
- All: New architecture development
- LBNL: Analog FE, Pad frame, DAC's, Integration,...
  - Abder Mekkaoui, Dario Gnani
- Bonn: LVDS, Linear regulators, DAC's, ...
  - Marlon Barbero, Michael Karagounis, David Arutinov, Tomasz Hemperek
- CPPM: Analog pixel, SEU latches,...
  - Mohsine Menouni
- Genova: Data I/O, Simulation,...
  - Roberto Beccherle
- Nikhef: Voltage reference, slow control,...
  - Ruud Kluit.

Monolithic and single sided stave based designs

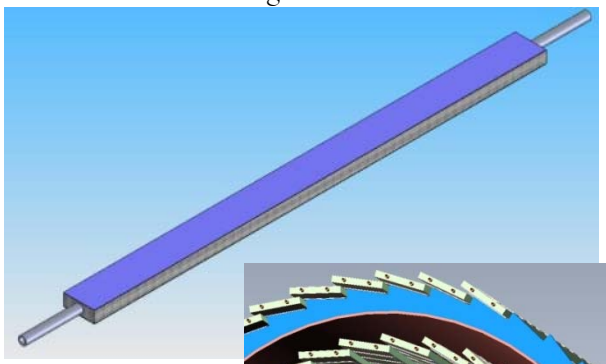
- there is huge design and prototyping effort focused on the use of carbon low-density thermally conducting foam + very thin "skins" of carbon-fiber laminate with Al cooling pipes inside *(M.Gilchriese, LBNL)*
- Why to use a foam? Versatile and low-mass. Compatible with both monolithic and stave-based designs

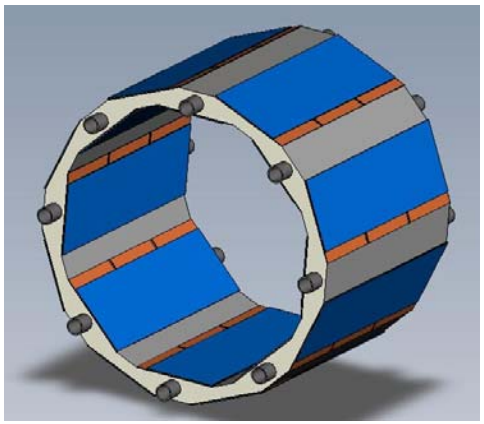
- Foam thermal properties depend on manufacture Usually varies from 6 to 30 W/mK

- K=10 W/mK a 0.6W/cm^2
- ΔT silicon–coollant ~10°C

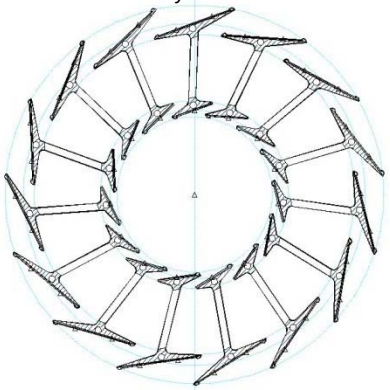


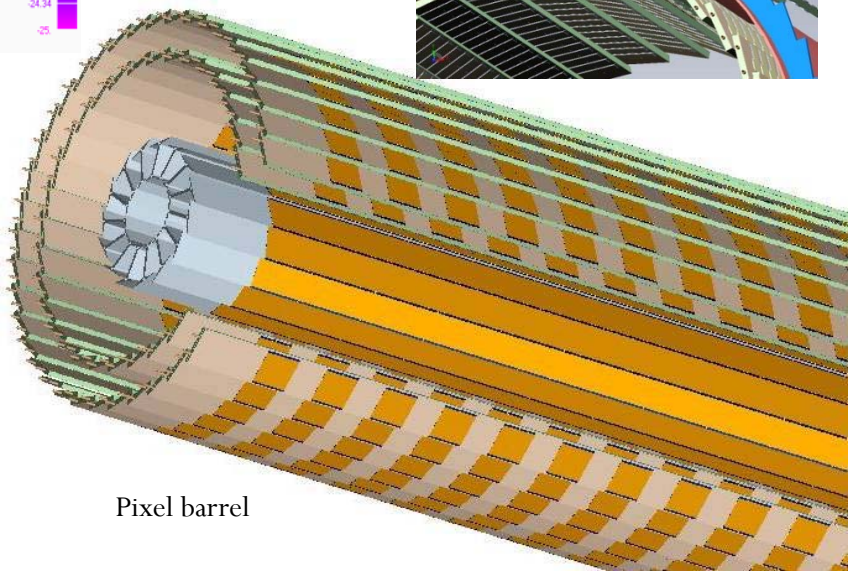
Single sided stave





2 insertable inner layers

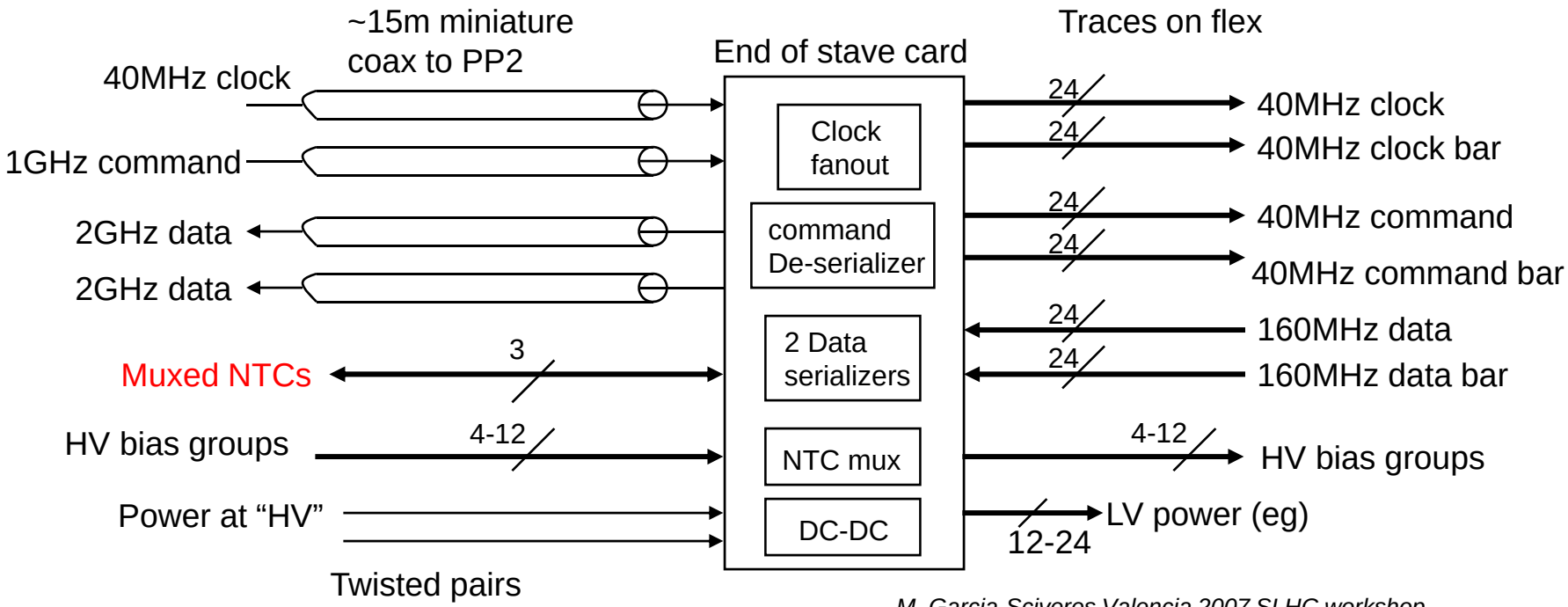




Pixel barrel

G.Gilchriese, N.Hartman , M.Garcia-Sciveres, E.Anderssen (LBNL Berkeley), CERN May 2008

Possible solution for End of stave card I/O



M. Garcia-Sciveres Valencia 2007 SLHC workshop

- general trend is to transfer some functionalities at the end of barrel staves or the edge of disc sectors
- it concerns of **D**etector **C**ontrol **S**ystem as well, we assume to place there DCS dedicated chip with LV voltage and current measurement, temperature monitoring capabilities etc.

Summary

- There are 3 main issues for the Pixel Detector Upgrade: ***Detector Performance, Lifetime and the Cost***
- Development of radiation hard silicon sensors for fluence close to $2 \cdot 10^{16}$ n_{eq}/cm^2 seems to be really very serious issue, …
- To be ready for installation during LHC shutdown (considered in 2016) is quite aggressive but still feasible, perfect coordination of all activities is essential assumption, right decisions in time and detailed scheduling step by step needed…
- The overall production cost will be certainly a key factor…, but for the innermost layer(s) we will chose the best what we can have in given time
- We may even consider 2 different module types - cheaper ones and probably also larger for outer layers and more delicate (higher granularity, radiation harder) for pixel inner layers
- New FE-I4 will be very likely suitable chip for B-Layer replacement (Y2012/13?) and we can also imagine the use at outer Pixel layers at SLHC, however for innermost layer(s) at least the pixel size has to be further reduced…
- Upgrade of innermost B-layer seems to be in intermediate step to SLHC detector upgrade. Considering installation in 2012/13, very little time for substantial R&D is left! Many key decisions have to be done within next months!
- Large fraction of the Atlas Pixel community is busy with commissioning and operation of the Pixel detector at CERN, manpower could be an issue…
- Large number of R&D's in different areas is ongoing, there are many interesting ideas but always proper prototyping needed to understand details and make a conclusion….