SLHC Upgrade Plans for the ATLAS Pixel Detector

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Abstract

The ATLAS Pixel Detector is an 80 million channels silicon tracking system designed to detect charged tracks and secondary vertices with high precision. An upgrade of the ATLAS Pixel detector is presently being considered. The Large Hadron Collider (LHC) will be upgraded to provide a ten fold increased luminosity leading to increased radiation doses and significantly higher occupancy in the region of the ATLAS Inner Detector and especially in the Pixel Detector.

The extreme radiation levels at planed Super Large Hadron Collider (SLHC) lead to a number of specific design challenges for read-out integrated circuits, silicon sensors and optical signal transmission. Options considered for a new detector are discussed, as well as some important R&D activities, such as investigations towards novel detector geometries and novel processes.

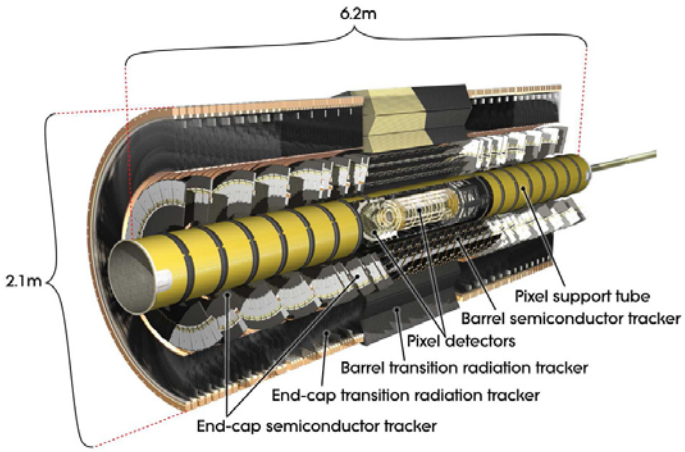

Figure 1: ATLAS Inner Detector

I. INTRODUCTION

The ATLAS detector is one of the largest and one of the most complex detectors at LHC. It is general purpose detector for the study of p-p interaction. In the heart of ATLAS, inside the solenoid magnet is the Inner detector. The Inner detector consists of Transition Radiation Tracker, Silicon Central Tracker and in the innermost region the Pixel Detector.

The Pixel detector provides critical tracking information for pattern recognition near the interaction point and very significantly contributes to overall capability of the Inner detector to find and reconstruct secondary vertices. In addition it provides very good spatial resolution for reconstruction of primary vertices coming from p-p collision point. The design of the Pixel detector is done in a way to get at least three space points on a charged track coming from the interaction point of ATLAS. There are three barrel layers approximately at radii of 5, 9 and 12cm with respect to the interaction point and six disks, three at each side of the detector. The actual layout of the Inner detector is illustrated in Fig.1.

The pixel detector is built with 1744 modules identical for both barrel and disk parts. The module consists of silicon sensor containing 2880 planar diodes of 50x400µm connected to sixteen Front - End (FE) chips. The electrical connection of the sensor and FE chips is done via bump-bonding interconnection technology using solder or indium bumps of about 12µm in diameter. The total number of channels is about 80 million and the total active silicon area is about 1,7m^2 [1].

II. THE LHC MACHINE UPGRADE

The LHC at CERN is recently ready to start operation and first data coming from proton-proton collision are expected soon. The exact upgrade scenario of LHC to SLHC is not yet defined in details but most likely it will occur in a number of phases.

An relatively modest increase above nominal luminosity 10^{34} cm^{-2}s^{-1} is expected in the first 4-5 years of LHC running and should be achieved through higher beam currents. This first upgrade phase would also involve major hardware upgrade, in particular the installation of new inner triplet focussing magnets allowing larger aperture. The changes just mentioned should allow a ramp-up close to 3 times nominal luminosity. The integrated luminosity that time should reach about 700fb^{-1} and about 70 events are expected per collision.

The second phase of upgrading to SLHC will require rather larger time counting in order of months. Several ideas are recently investigated to reach the target value 10^{35} cm^{-2}s^{-1} in 2017. The hardware changes will certainly include major improvement of injector and likely other new machine elements will have to be installed. More details can be found in [2].

The running at such high luminosity as 10^{35}cm^{-2}s^{-1} will bring up pile-up of about 400 p-p interaction per collision and the annual integrated luminosity will be around 300fb-1. In total, the integrated luminosity delivered in course of LHC and SLHC running should reach a value about 3000fb^{-1}.

The scenario recently considered and here described is shown in Fig 2.

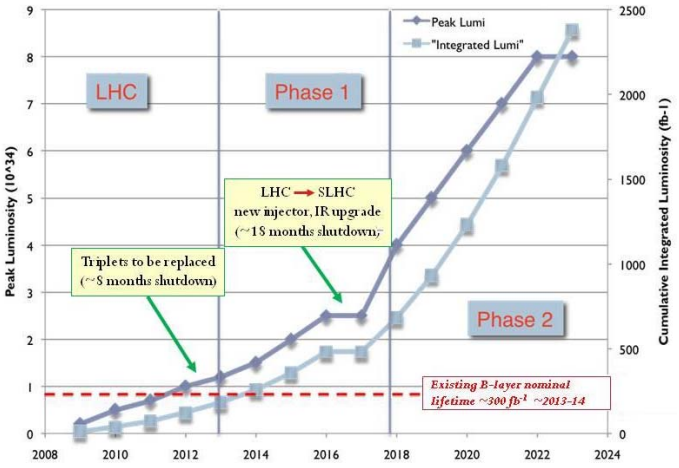

Figure 2: Expected Luminosity Upgrade Scenario [2]

III. SLHC GOALS AND PHYSICS MOTIVATION

In general, the SLHC luminosity upgrade to $10^{35}cm^{-2}s^{-1}$ allows extension of the LHC discovery mass/scale range by 25–30% and improves the sensitivity for precision measurements, for example, the couplings between the electro-weak bosons or of the couplings of the Higgs boson to various other particles. Operation of LHC will certainly provide a deep view of the physics at energy of TeV scale. Nevertheless, the physics program at LHC still does not guarantee whole understanding of all fundamental questions in particle physics. It is rather difficult to predict these days, at the beginning of LHC operation what would be the best next machine after LHC. Obviously it will become clearer when the first LHC data will be available. The upgrade to luminosity of $10^{35}cm^{-2}s^{-1}$ seems to be reasonable compromise between the cost and physics achievements. SLHC is natural extension of the LHC program for further decade of years requiring rather modest investment compared to the LHC overall cost in an efficient way. It maximally exploits the existing tunnel, the machine and also the experiments.

However, to fully exploit a factor 10 increase in the luminosity, the tracking performance of ATLAS during SLHC operation must be maintained at a level comparable to its performance during LHC operation.

IV. IMPACT TO TRACKER DETECTORS AND RADIATION LEVELS

It is evident that upgrading to SLHC will pose a significant challenge to experiments especially to ATLAS and CMS. The entire tracking system of both main LHC experiments has to be completely replaced and major upgrades are also being considered for the forward calorimeters, trigger system and beam-pipe. The start-up of LHC operation will help with focusing the main effort to right direction. In light of these upgrade issues a number of R&D's have already started in order to be ready to take SLHC data in the second half of next decade. For the detector upgrades, the overall design, production and installation schedule is already a very aggressive goal based on the LHC experience.

The expected high radiation levels as well as the large increase in the occupancy impose very strict requirements to inner tracking systems of ATLAS and CMS experiments. In order to cope with the increased occupancy, the LHC trackers will have to be replaced by ones with higher granularity. In reality it means about a factor of 2-3 more channels. The increased channel number imposes stringent constraints also for the power consumptions as well for the material budget. Therefore new powering schemes for trackers are considered. In addition, very radiation-hard techniques will be needed in the hottest region within 20cm apart from the beam pipe. Such environment is demanding fundamental R&D for new detector materials and concepts. At larger radii, evolutions of the present pixel and strip technologies should be still adequate.

Fig. 3 shows simulated radiation level inside the Inner detector region of ATLAS. The innermost part where the Pixel detector is installed will be exposed up to a fluence close to 10^{16} n_{eq}/cm^2 and to radiation dose of 5MGy in FE electronics corresponding to the total integrated luminosity of $3000fb^{-1}$ delivered by LHC/SLHC. The simulation of radiation levels is shown in Fig.3 [3].

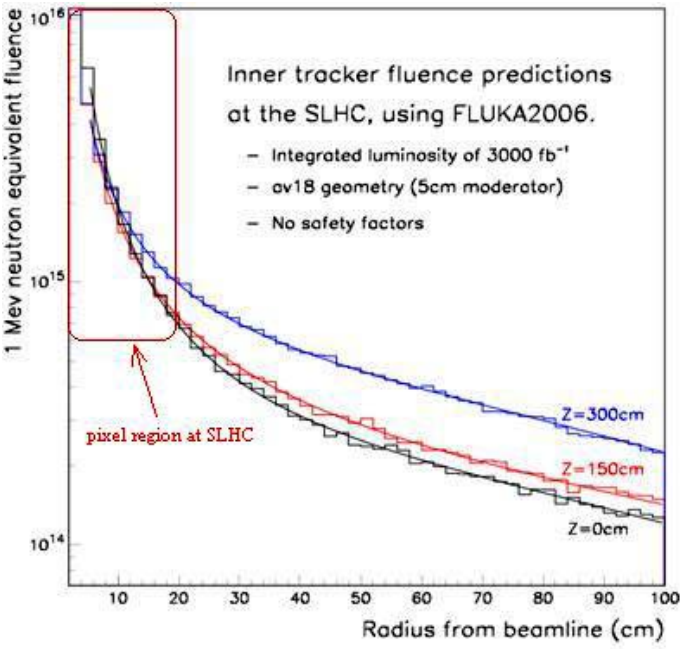

Figure 3: Prediction of 1MeV n_{eq} fluence in Inner Detector corresponding to integrated luminosity of $3000fb^{-1}$

V. PIXEL DETECTOR B-LAYER REPLACEMENT

With expected luminosity increase we assume the performance of the innermost pixel B-layer will start to

degrade due to radiation damage after 3-4 years of LHC operation. This will happen when LHC integrated luminosity will reach about 300fb^{-1} corresponding to a fluence of about 10^{15} n_{eq}/cm^2 in this innermost Pixel detector region where the B-layer is installed. As the after effects of such very harsh radiation environment influence one can expect to observe reduced efficiency and worsening of point resolution of the B-layer. Also, the present B-layer is not designed for luminosities above 2 x $10^{34}cm^{-2}s^{-1}$. Due to granularity issue, the read-out chain does not allow to read all hit pixels and the deteriorating of efficiency would be starting.

The performance of the B-layer has significant impact on Atlas physics especially on B-tagging. Therefore it is suggested to replace the recent B-layer with new one or even to insert the new B-layer built with reduced diameter whilst keeping the old one inside the detector.

The second option, the insertion of the new B-layer it will happen most likely considering access issues at ATLAS after few years of LHC operation and rather short shutdown periods allowing access to the detector cavern.

VI. Development of Sensors for SLHC

As already mentioned, the ATLAS Pixel detector will have to operate in very harsh radiation environment resulting fluence up to 10^{16} n_{eq}/cm^2. The current Pixel detector sensors are based on planar n-in-n technology (n-type bulk) and are proved to be sufficiently radiation hard up to a fluence order of magnitude lower, it means around 10^{15} n_{eq}/cm^2. Recently there are several R&D's running in parallel searching for new sensor design concepts and technologies. Obviously overall production cost of new sensors will play dominant role especially at larger radii where the detector area is not negligible.

Recently used n-in-n sensors are not radiation resistant enough to be seriously considered for the innermost Pixel detector layers at SLHC. Choosing p–bulk material seems to bring several advantages. Firstly, it requires only single side wafer processing what would lead to higher production yield and consequently to significantly reduced production cost when compared to double sided n-in-n technology. Also, the p-bulk material does not invert and the pixel connection is always at junction side. P-bulk sensors show less charge trapping when highly irradiated.

Developments of both, n-in-n and n-in-p planar sensors are aimed to rise breakdown voltage values allowing increase of maximal applicable bias voltage, probably to values close to 1000V whilst reducing the inactive area at detector edges. Obviously the cutting quality has significant influence to detector properties and therefore new "safer" methods and technologies are also searched.

The "thin sensors", ~75-150µm thick silicon planar sensors benefiting much lower voltage needed to reach full depletion state, shorter collection time, reduced reverse current and shot noise contribution. There is not significant difference when comparing amount of collected charge after fluence 10^{16} n_{eq}/cm^2 at "thin" sensors with standard ~280µm sensors. However, such sensors are yielding lower signal since the beginning of operation and are demanding low threshold operation of FE electronics (Th < 4000e-). "Thin" sensors use usually connected to thinned FE electronics vertically using very challenging Inter Chip Vias (ICV) or Through Silicon Vias (TSV) interconnection method both offering an alternative to the bump-bonding process [4].

The 3D sensors, sensors where tiny highly doped p+ and n+ electrodes are processed inside the detector bulk instead of being implanted on the wafer's surface, have progressed pretty well since time when firstly introduced. The technology developed and adopted originally at Stanford Nanofabrication Facility is being successfully transferred to the industry. Several companies (e.g. SINTEF Norway, IRST Italy, CNM Spain) already adopted key technological operations including critical steps as deep reactive ion etching or poly-silicon filling into tiny electrode holes of few microns in diameter. The 3D detectors perform quite well even after high irradiation dose (Fig.4).

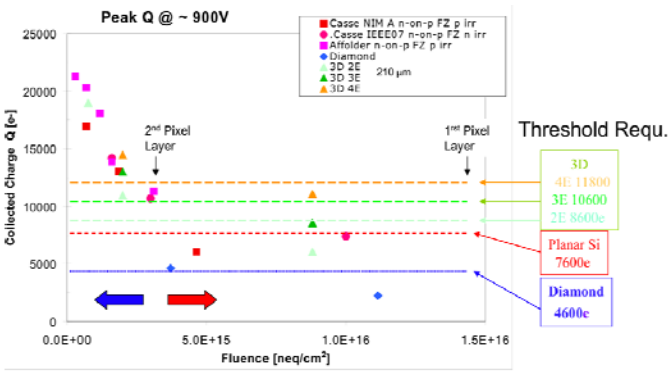

Figure 4: Collected Charge of different sensor types [6]

VII. Demands on Front-End Electronics

The increase of the luminosity by order of magnitude brings significant challenge to electronics of trackers. Firstly, the detectors need a sufficiently fine granularity and high resolution to resolve hit ambiguities when performing the pattern recognition. The pile-up of about 400events per beam crossing at SLHC is expected yielding about 30 tracks per cm^{-2} per bunch crossing. It requires to reduce the pixel size from current 50 x 400µm to 50 x 250µm or even further to 50 x 200µm. The pixel pitch of 50µm will be most likely kept to allow "safe" and relatively less costly bump-bonding processing and to provide more freedom for selection of final sensor design (inter-pixel insulation, 3D implementation, etc). The IBM 0.25µm process used for the recent FE electronics is becoming obsolete and newer IBM 0.13µm CMOS8RF process featuring with enhancements for analog design seems to be the most appropriate technology for B-layer replacement or even for SLHC FE electronics. The use of 0,13µm CMOS process should allow further scaling of design. The digital part should scale by at least 4 in going from 0.25µm to 0.13µm, due to presence of greater interconnection ability as well as device scaling. However, newer CMOS technologies can usually reduce only the size of digital circuitry, but the size and power required for the transistors in the analog

circuitry are set by the required noise and threshold matching. Newer submicron CMOS technologies would not reduce the power required for the desired noise levels, but would improve digital power efficiency.

The 0,13µm CMOS process is naturally more radiation resistant due to further reduction of thin oxide. Present pixel FE-I3 chips (0.25µm process) suffer from Vt shift at large doses affecting threshold dispersion and time over threshold (TOT) measurements. However, it does not look to be a serious issue for 0,13µm process. The 0,13µm process should allow simplification of rather complex in cell built tuning circuitry and also dropping guard rings around NMOS devices. The radiation dose seems to be mainly serious sensor issue resulting decrease of charge collection efficiency. Therefore the analog pixel electronics must cope with lower charge of irradiated sensors (8-10ke or even less), with relatively high sensor capacitance and high input current.

The goal for development of new FE electronics is to reduce inactive area (the area not covered by sensitive part of the sensor) as much as possible and also significantly enlarge the size of the FE chip. Recently used FE-I3 chips have size of 7,6 x 10,8mm (74% active area), proposed new FE-I4 pixel chip should have the size of 20,2 x 18,8mm (89% active area). Larger FE chips will reduce the assembly cost (flip chip process) and also the cost of sensors due to smaller module size considering 2x2 chips on the module or even only single chip modules for inner Pixel detector layers.

The digital readout architecture of recent FE-I3 chips is not appropriate for high SLHC luminosity and the hit inefficiency would rise steeply with high hit rate. The bottleneck is mainly data transfer through column pair bus clocked at 20MHz (shift register). All hits are transferred to the end of column buffer (64 deep) where waiting trigger, but only ~1% hits are actually triggered. The idea for new readout architecture is based on buffers placed locally close to a group of pixels and the transfer of information to the periphery would happen only when getting really triggered (Fig 5).

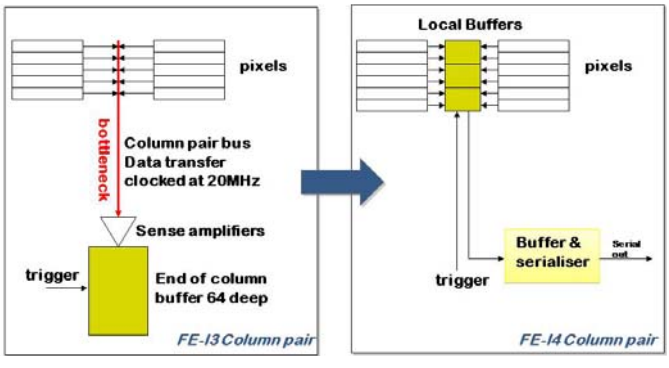

Figure 5: New FE Read-Out architecture [5]

VIII. Pixel Detector Module and Stave Concept

General trend is to have the pixel module quite simple what would lead to higher production yield reducing overall cost. Recently is proposed to have modules with 4 FE chips for outer layers and perhaps only single chip modules for inner layers. Proposed size of the outer layer module is about 36 x 42,5mm accommodating 2x2 FE chips. The module controller chip is not considered anymore and will be substituted by stave controller chip, probably with simplified functionality placed at the "end of stave card".

There are many challenging discussions and proposals concerning Pixel detector layout a local support structures. Local supports provide the mechanical support and integrated cooling for pixel modules. The aim is to reduce material budget and simplify production. The low density, thermally conductive foam with very thin carbon fibre facings appear to be very convenient material for either single layer stave support or monolithic structures [7]. The highlights of the foam material are low mass, low distortion from cool-down, easy machining, good mechanical and thermal conductivity properties and low radiation length. Such features give very promising presumption to consider this material as good candidate for future support structures of Pixel layers.

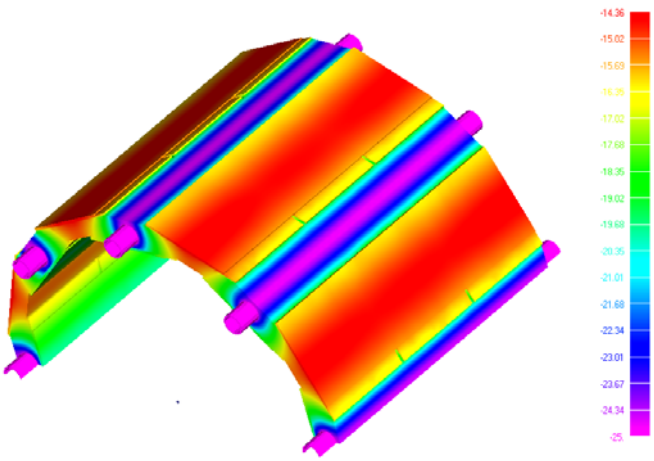

Figure 6: Monolithic foam structure thermal properties (0,6W/cm^2)[7]

IX. Powering Issues

The number of electronic channels will be dramatically increased for SLHC trackers. The total silicon area of upgraded Pixel detector will be approximately tripled. A constraint is that existing cable plant in the tracker most likely will not be replaced. The design of new tracker electronics must consider the use of existing cabling to power also additionally channels.

Presently used power scheme with separated power lines on level of the module can not be considered anymore. Such approach providing independent powering for each module is luxury way how to operate modules however, considering the cable material budget it is unacceptable furthermore. Also, the goal is to minimize the current flowing through the supply lines and to reduce cable power losses. Therefore options as DC-DC convertors with 2-3 times the target voltage placed close to the module or serial powering scheme with shunt or

linear regulators allowing supplying several FE electronic in series through one single power line are recently investigated.

X. Summary

There are three main issues to be taken into account when upgrading LHC tracking detectors: detector performance, detector lifetime and the overall cost. The lifetime of resent silicon sensors for SLHC seems to be really serious issue and there is not available appropriate sensor working at high fluence as 10^{16} n_{eq}/cm^2 without significant degradation of initial parameters. However, there are recently many R&D's focused on new technologies like 3D sensors, thin sensors or CVD diamond sensors. The planar sensors, as proved and relatively not expensive technology seem to be appropriate solution only for outer layers of the Pixel detector. The design of FE electronics partly depends on available technologies at given time. Obviously, the pixel size has to be further reduced the column readout architecture changed and the bandwidth of output links increased allowing higher data output rate. The timescale, either for B-layer replacement or full Pixel detector upgrade at SLHC is relatively short, so understanding of details, very good coordination and right decisions on time is substantial for successful development and installation at the ATLAS experiment.

XI. Acknowledgements

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