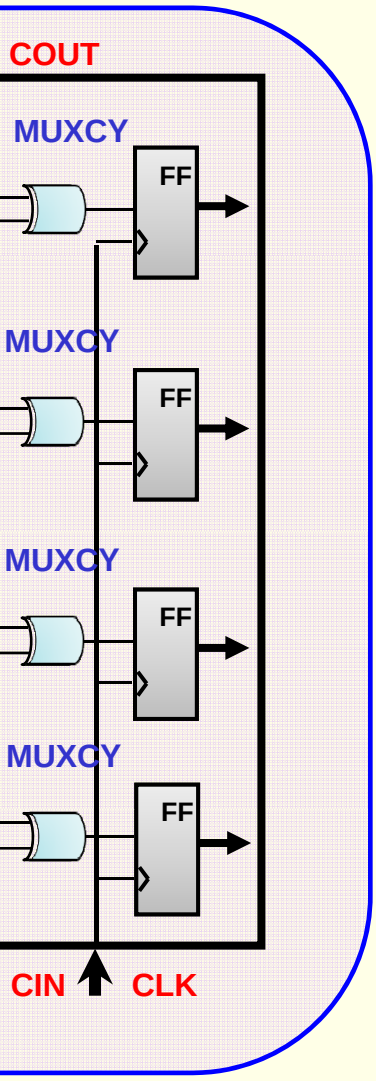

Our designs

In the FPGA available today, there ar purpose applications. A few well-kno products chains, etc. These chain str identical logic elements. They are ide In our works, the fine TDC for the me performed in two different methods:

1. The first architecture, shown in Fi newest available Xilinx Virtex 5 FPG the pertaining flip-flop on the rising e

2. The second architecture, shown i and it makes a differential delay line digital conversion process, the STO latches from the first cell up to the c consecutively set.

To implement the designs in FPGA development software, a logic cel depending on the optimization algor LEs may also be unpredictable to t placed and routed in this fashion, the To avoid this, the designer is forced layouts are presented respectively i diagrams of the Virtex 5 is shown.

test the two own in Fig.4. requency we

based on an FPGA based t to access a nput a delay es data bus,

Buffer to latch

Buffer to h