Our designs

In the FPGA available today, there are many applications. A few well-known examples are products chains, etc. These chains are made up of identical logic elements. They are ideal in our works, the fine TDC for the measurements performed in two different methods:

1. The first architecture, shown in Fig. 1, starts with the newest available Xilinx Virtex 5 FPGA, where the pertaining flip-flop on the rising edge of the input clock generates the new value. The fine delay line and it makes a differential delay line in the digital conversion process, the STO reads the STO latches from the first cell up to the output of the second cell consecutively set.

To implement the designs in FPGA, we use development software, a logic cell editor, and depending on the optimization algorithm. The area use of the logic elements may also be unpredictable to the designer. The designer is forced to place and route in this fashion, the designs in FPGAs.

To avoid this, the logic cells are presented respectively in the diagrams of the Virtex 5. The Virtex 5 architecture, shown in Fig. 4, is based on an FPGA-based logic cell editor, which contains a delay buffer to access a delay buffer to latch the data bus, and it can be used to test the two mentioned methods.