



Our designs

In the FPGA available today, there are purpose applications. A few well-known products chains, etc. These chain structures are identical logic elements. They are identical. In our works, the fine TDC for the measurement is performed in two different methods:

1. The first architecture, shown in Fig. 4.1, is the newest available Xilinx Virtex 5 FPGA. It is based on the pertaining flip-flop on the rising edge of the clock signal.
2. The second architecture, shown in Fig. 4.2, is based on a differential delay line. In the digital conversion process, the STO is implemented by latches from the first cell up to the output cell consecutively set.

To implement the designs in FPGA development software, a logic cell is placed depending on the optimization algorithm. Since the LEs may also be unpredictable to the placement and routed in this fashion, the layout is not optimal. To avoid this, the designer is forced to use a specific layout. The layouts are presented respectively in Fig. 4.1 and Fig. 4.2. The diagrams of the Virtex 5 is shown.

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