High-Resolution Time-to-Digital Converter in Field Programmable Gate Array

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Two high-resolution time-interval measuring system implemented in a SRAM-based FPGA device are presented. The two methods ought to be used for time interpolation within the system clock cycle. We designed and built a PCB hosting a Virtex-5 Xilinx FPGA and high stability oscillators to test the two different architectures. In the first method, dedicated carry lines are used to perform fine time measurement, while in the second one a differential tapped delay line is used. In this paper we compare the two architectures and show their performance in terms of stability and resolution.

Summary

High-resolution Time-to-Digital Converters are often required in many applications in high-energy and nuclear physics. Furthermore, they are widely used in many scientific equipments such as Time-Of-Flight (TOF) spectrometers and distance measurements.

Different configurations of tapped delay lines are widely used to measure sub-nanosecond time intervals both in ASIC and FPGA devices. However, the design process of an ASIC device can be expensive, especially if produced in small quantities, while FPGAs lower the development cost and offer more design flexibility. In 1997, Kalisz et al. [1] proposed an FPGA-based approach: their design used a variation of conventional delay line and offered a time resolution of 200 ps. In 2000 [2], rapid progress in electronics technology allowed them to achieve a time resolution of 100 ps. It should be noted that the above used FPGA devices were one-time programmable so that each iteration involved the utilization of a new device. By using SRAM-based FPGAs, the user benefits from the in-system-programming (ISP) and reconfiguration features. Resolution values between 50 ps and 500 ps have been achieved with this technology [3]. Two different digital delay line circuits have been designed and tested by the authors thus far [4]. We designed and built a PCB hosting a Virtex-5 FPGA from Xilinx [5] to test the two different TDC architectures. Two high stability oscillators from Valpey-Fisher have been installed in order to compare their performance side by side. Test points for high-bandwidth active probes are used to perform the Virtex-5 clock signal characterization. They are placed just near the FPGA, making the shortest distance for the device output signals. SMA connectors are used to send the START and STOP signals to the board. They may adopt differential lines or single ended signaling schemes.

Both approaches of the two architectures use the classic Nutt method [6] based on the two stage interpolation. The time interval T to be measured is decomposed into three intervals:
- the integer number N of the reference clock periods Tc is measured by a binary counter;
- two short intervals Δt1 and Δt2 at the initial and final part of the measured interval, each having a duration within one clock period.

The fine time measurement of the short time intervals have been performed in two different methods. The delay elements exploit either general purpose resources, like logic element, or special purpose resources, like dedicated carry logic. The first architecture uses carry chain delays, while in the second one a differential tapped delay line is used. The main design problem was the implementation of the delay line by using the logic cells offered by the FPGA technology. In order to assure the uniformity of the propagation delays, the cells have been placed and routed by hand.

In this paper, we describe the implementation and characterization of the two different fine TDC. The behaviour of the two architectures is compared and we show their performance in terms of stability and resolution.

References:

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