Contribution ID: **108** Type: **Poster**

FPGA Implementation of Optimal Filtering Algorithm for TileCal ROD System

Thursday 18 September 2008 16:15 (20 minutes)

Traditionally, Optimal Filtering Algorithm has been implemented using general purpose programmable DSP chips. Alternatively, new FPGAs provide a highly adaptable and flexible system to develop this algorithm.
TileCal ROD is a multi-channel system, where similar data arrives at very high sampling rates and is subject to simultaneous tasks. It include different FPGAs with high I/O and with parallel structures that provide a benefit at a data analysis.
The Optical Multiplexer Board is one of the elements presents in TileCal ROD System. It has Cyclone devices that present an ideal platform for implementing Optimal Filtering Algorithm. Actually this algorithm is performing in the DSPs included at ROD Motherboard.
This work presents an alternative to implement Optimal Filtering Algorithm.

Summary

Digital Signal Processor (DSP) is actually the main component in the TileCal Read-Out Driver (ROD) System. The DSPs are responsible for data reconstruction in real time at the ATLAS first level trigger rate (100 KHz). The DSP has to compute energy, phase and Quality Factor (QF) for all the channels in less than 10 μs at the ATLAS maximum rate and send the reconstructed data to the second trigger level.
The Optimal Filtering (OF) Algorithm reconstructs the amplitude and phase of a digitized signal by a linear combination of its digitized samples, pedestal subtracted. DSPs executes OF Algorithms in real time.
To reduce data loss due to radiation effects, the TileCal collaboration decided to include data redundancy in the output links of the FrontEnd. This was accomplished using two optical fibres which transmit the same data. For this purpose a new module, called Optical Multiplexer Board (OMB) was conceived. This board would be able to provide, in case of error in one link, the correct data to the ROD input by analyzing the Cyclic Redundancy Codes (CRC) of the data packets on both fibers coming from the FEB.
OMB has Cyclone devices that provide an ideal platform for implementing low-cost digital signal processing (DSP) systems on an FPGA. Cyclone devices present a flexible hardware solution in which we can implement an Optimal Filtering Algorithm.
This work presents an alternative to implement Optimal Filtering Algorithm.

Primary author: Dr TORRES, Jose (Universidad de Valencia)

Co-authors: JALAL, Abdallah (IFIC); VICTORIA, Castillo (IFIC); CRISTOBAL, Cuenca (IFIC); ANTONIO, Ferrer (IFIC); ESTEBAN, Fullana (IFIC); VICENTE, Gonzalez (Universidad de Valencia); EMILIO, Higon (IFIC); JOAQUIN, Poveda (IFIC); ARANCHA, Ruiz-Martinez (IFIC); BELEN, Salvachua (IFIC); ENRIQUE, Sanchis (Universidad de Valencia); CARLOS, Solans (IFIC); ALBERTO, Valero (IFIC); JUAN, Valls (IFIC)

Presenter: Dr TORRES, Jose (Universidad de Valencia)

Session Classification: POSTERS SESSION