Status Report on the LOC ASIC

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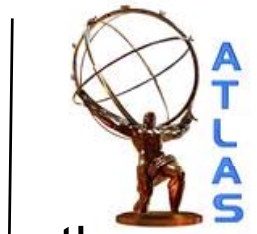
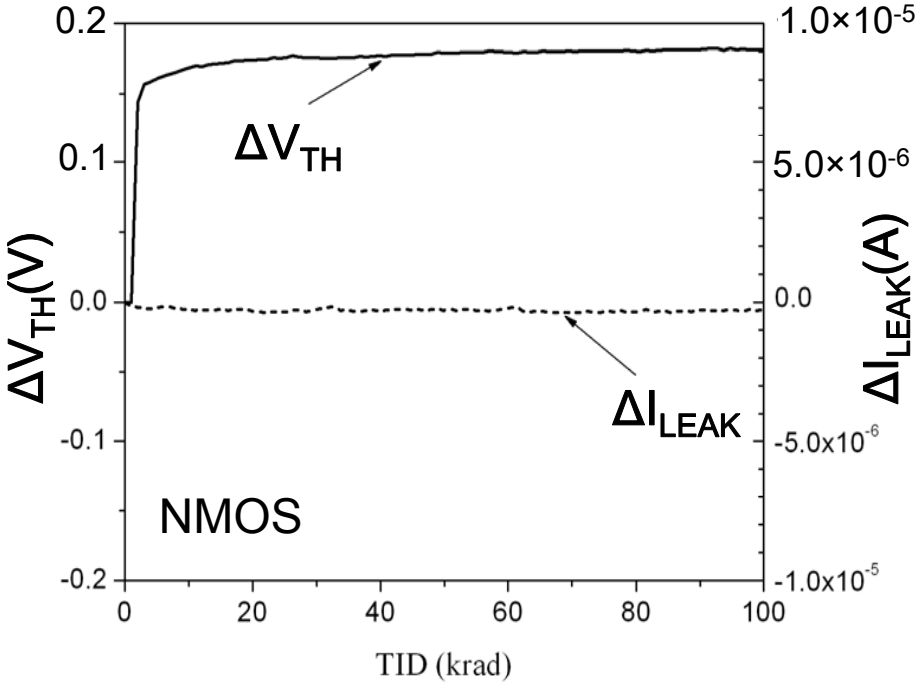
The LOC ASIC proposal

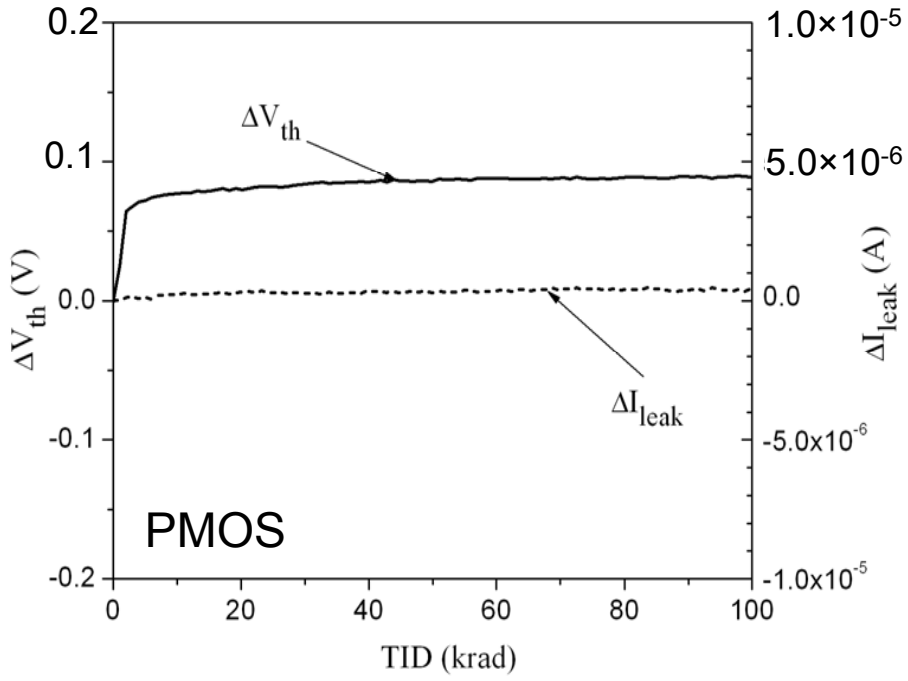


- The LOC (link-on-chip) was proposed as a serializer ASIC for the ATLAS LAr readout upgrade, under the US-ATLAS upgrade program.
- The initial idea was to integrate “everything” into one chip, including the optical interface. Fiber would be coupled directly to the chip to spare the high speed copper traces on the PCB.
- The project started with the SOS technology evaluation.
- A first prototype, LOC1 was designed with collaborative effort between the EE and physics departments at SMU. This prototype provided valuable information on key components, especially the PLL and the serializer structure, for the LOC2 design.
- The second prototype, LOC2 is the one to be reported in detail here.
- The whole project benefits tremendously from the CERN GOL ASIC design. We would like to express our gratefulness to many people in the CERN microelectronics group, especially to Paulo Moreira for his very kind help in the LOC project. Without his help, we would not be here today to present the design results on LOC.

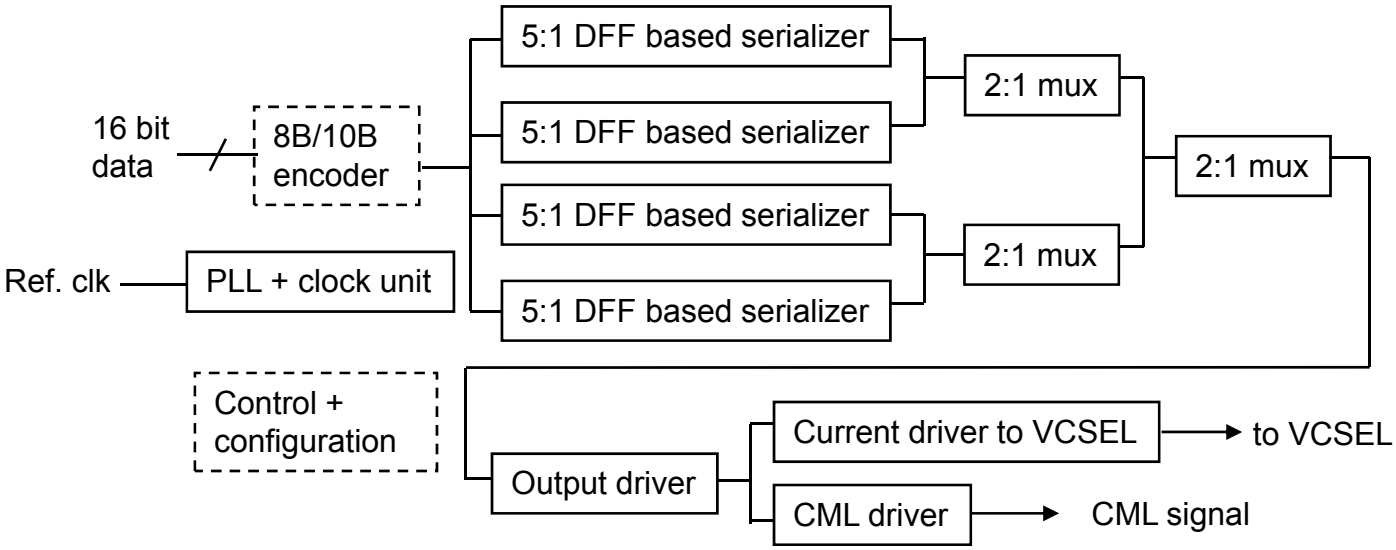
The SOS technology

- A 0.25 micron Silicon on Sapphire commercial CMOS technology has been chosen for the LOC ASIC development.
- A dedicated test chip with transistors, ring oscillators and shift registers has been designed and fabricated for irradiation tests.
- Some results from the irradiation tests have been published at RADECS 2007.
- The TID test results on transistors are summarized here. The substrate is grounded.
  - Almost no leakage current change;
  - A small threshold voltage change happens at the very beginning of the irradiation and then remains unchanged with the increase of total dose.
- The technology evaluation continues with more detailed studies, supported by the ADR (US DOE) program.

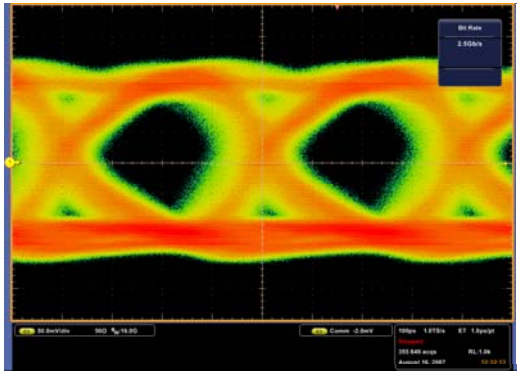




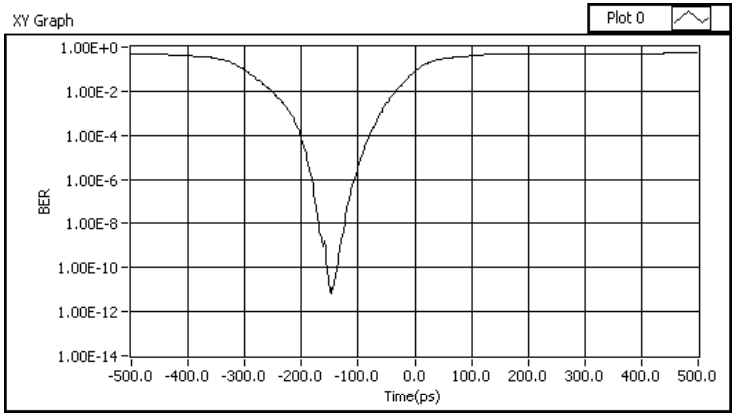
The LOC1 test results



Solid line box: implemented; dashed line box: implemented in FPGA.



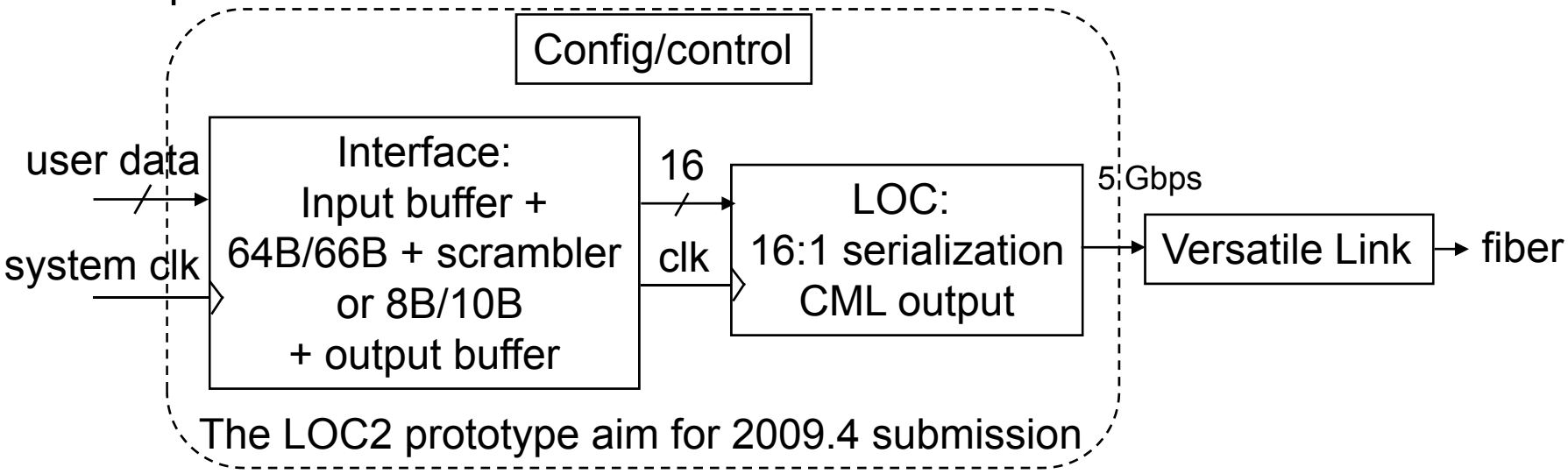
Eye diagram of an 2^7-1 pseudo random input data. The data rate is 2.5 Gbps. Large DJ is observed, understood and will be corrected in LOC2



The bit error rate bathtub curve at 2.5 Gbps, the best BER reached is ~10^{-11}.

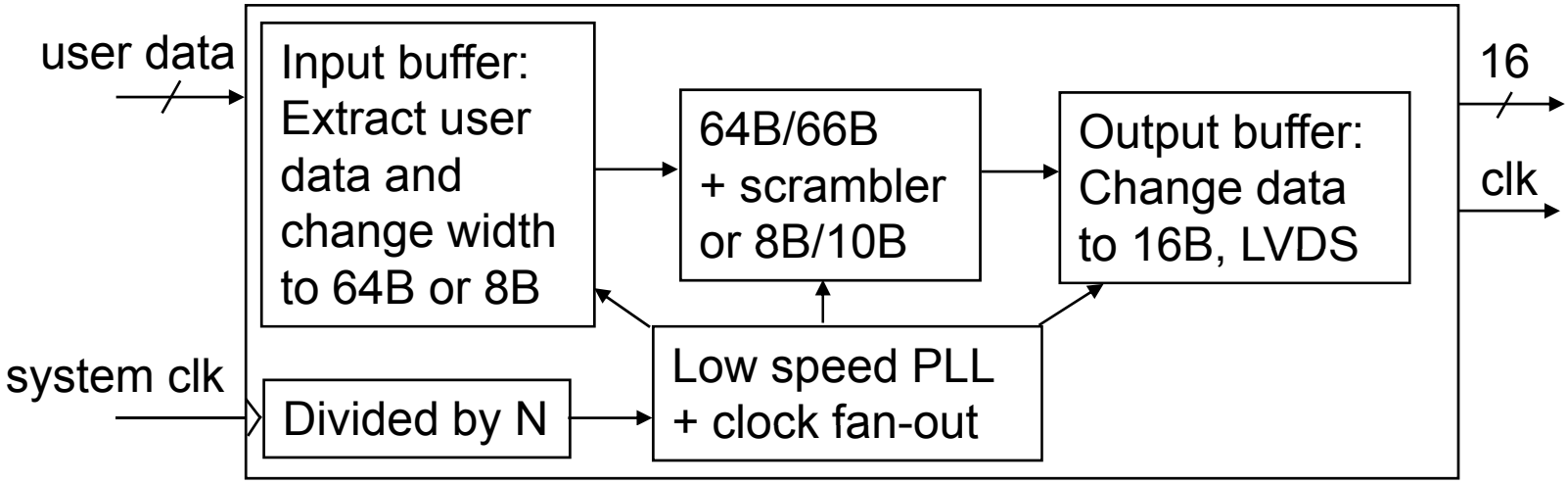
LOC2 Block diagram and design considerations

- After many discussions with people in the ATLAS Inner Detector and the LAr, we now propose the LOC2 ASIC as a 16:1 serializer with the serial output in the 5 Gbps range.
- Since the LOC design speed has been pushed higher and higher, towards the technology limit, a 16:1 serializer simplifies the implementation of high speed circuits.
- We move the framing unit into the interface for better integration with both the ATLAS Inner Detector and the LAr readout systems.
- We take advantage of the CERN Versatile Link project and move the optical interface into the VL, so LOC will only provide a CML electrical output.

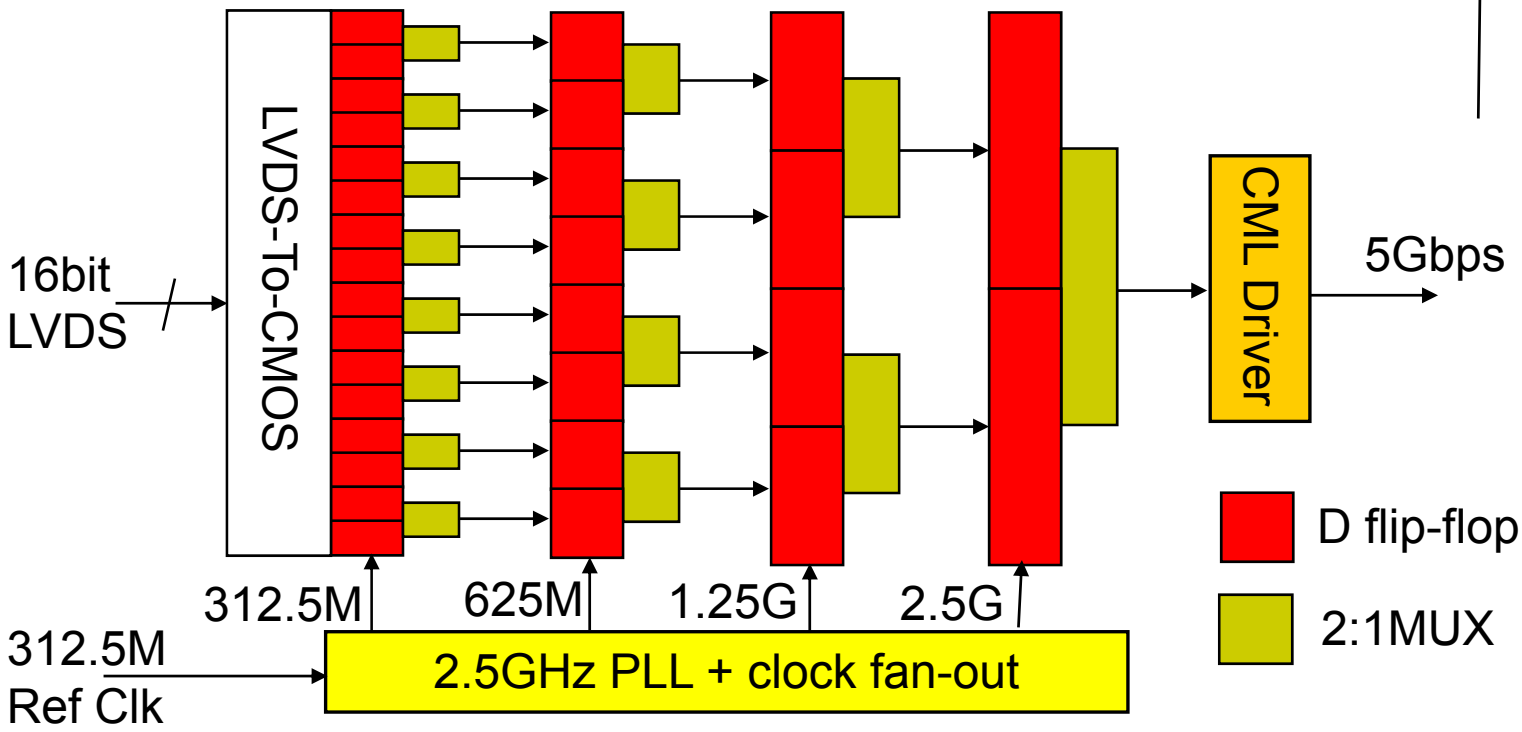


Interface to different users

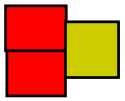
- For ATLAS Inner Detector, the input to the optical link may contain DC balance coding that may need to be removed to save on bandwidth overhead.
- For LAr, link bandwidth is the premium.
- We propose the interface chip/function block to be:



The 16:1 serializer and challenging spots:



The logic structure is much simpler than a 20:1 serializer.

The fundamental structure is 2:1 multiplexing unit 

The Critical components:

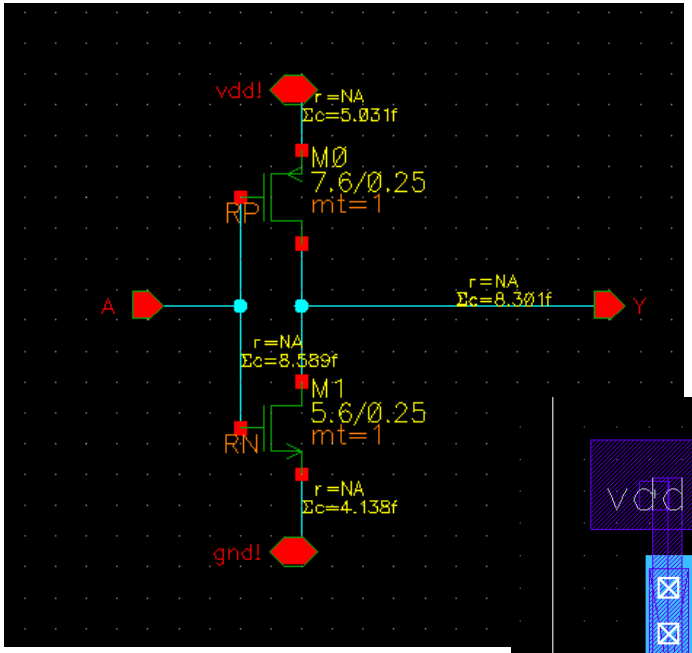
1. 2.5 GHz PLL → Low jitter, duty cycle 50%
2. Static D-flip-flop. The building block of the clock divider, and the shift register → speed.
3. CML driver → Pre-emphasize will be considered.

LOC2 design status

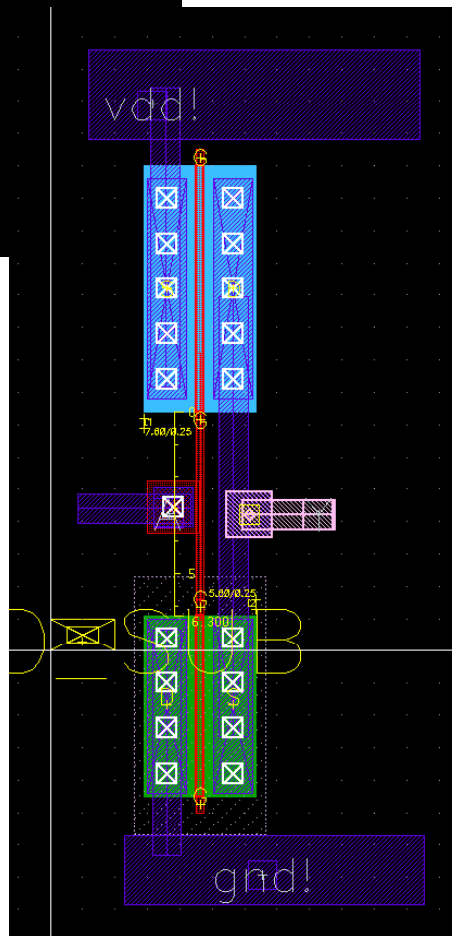
- Speed comparison of 0.25 μm SOS and BulkCMOS (TSMC) with inverter, and adjust the PMOS/NMOS transistors ratio for the same 0→1 and 1→0 transition time. ➔ done.
- Choose a static D-flip-flop design that meets the 5 Gbps speed requirement. ➔ done.
- Choose the self-biasing PLL structure to minimize noise. ➔ in progress.
- Interface chip/block: 8B/10B logic checked. Need to understand how to implement 64B/66B+scrambler. ➔ need manpower help.

The inverter

- PMOS/NMOS ratio adjusted to have the same 1→0 and 0→1 delays.
  The ratio is: n*(1.9/1.4)
  where n = 1,2,3,4…
- Basic layout, multi-finer layout checked to optimize speed. The delay is about 32~35 ps (drive itself), corresponding to a frequency of about 30 GHz. Agree with Peregrine's tech notes, and comparable with speeds achieved in 0.13 to 0.15 micron bulk CMOS technology.
- A comparison is made with 0.25 micron bulk CMOS (TSMC) on the same inverter design. Simulation shows a 60 ps delay with the same layout and driving condition.



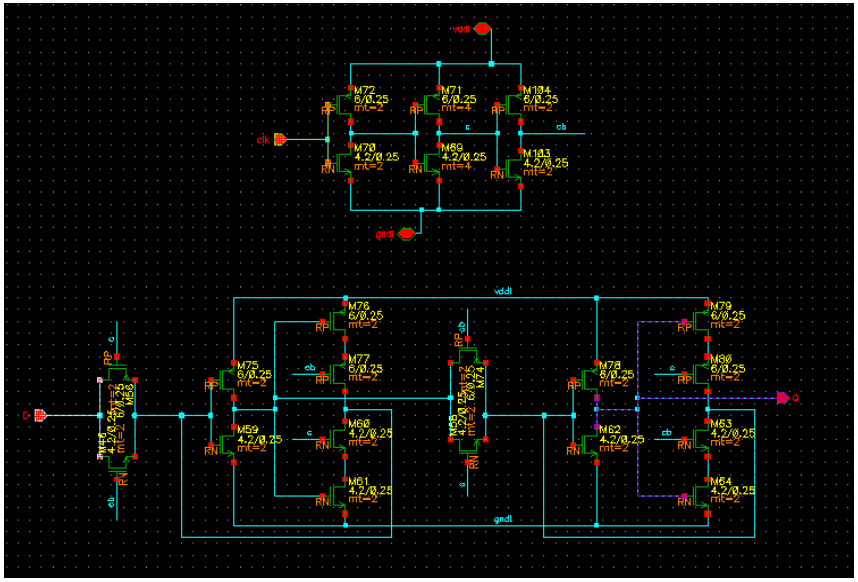
schematics



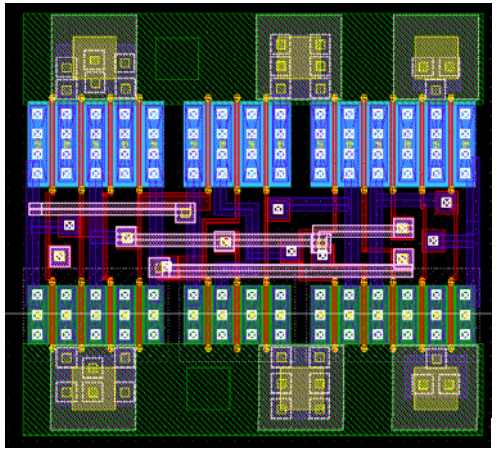
layout

The D-flip-flop (DFF)

- We started out with the C^{2}MOS type of DFF used in GOL, but moved to the TGDFF: ~20% faster, and at least the same SEE immunity (Ramanarayanan, Upenn).
- Different transistor size, single finger and multi-finger layouts are checked. The total delay is 292 ps (slowest or the S-S corner). This indicates a 5 Gbps serializer possible, because the time needed for a basic unit (DFF+mux) is 400 ps.

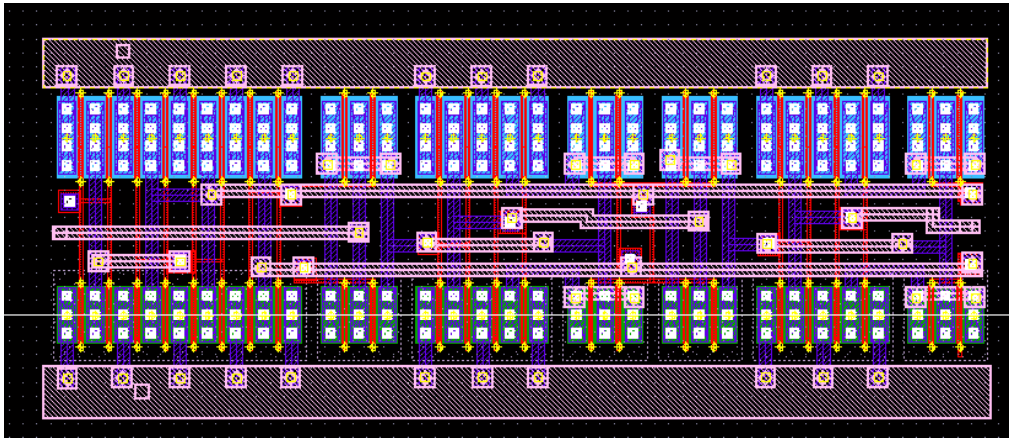


schematics

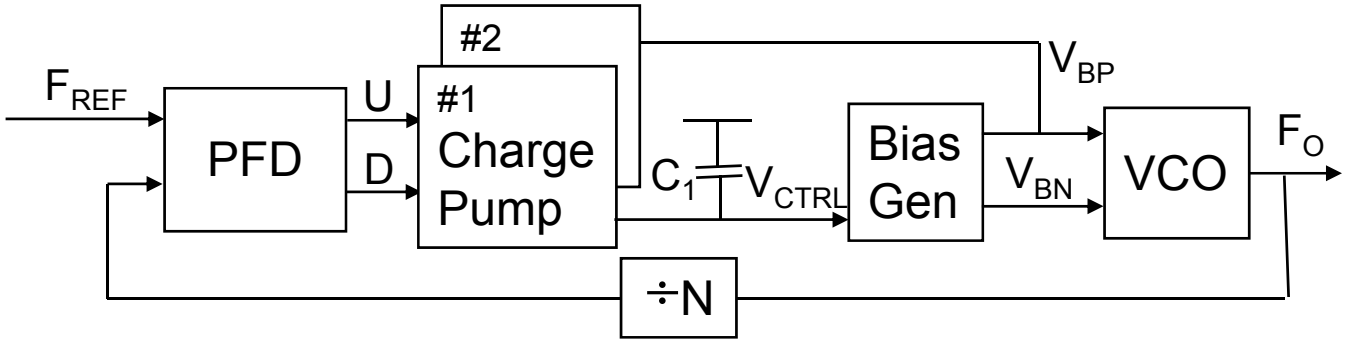


Mostly single-finger layout

multi-finger layout



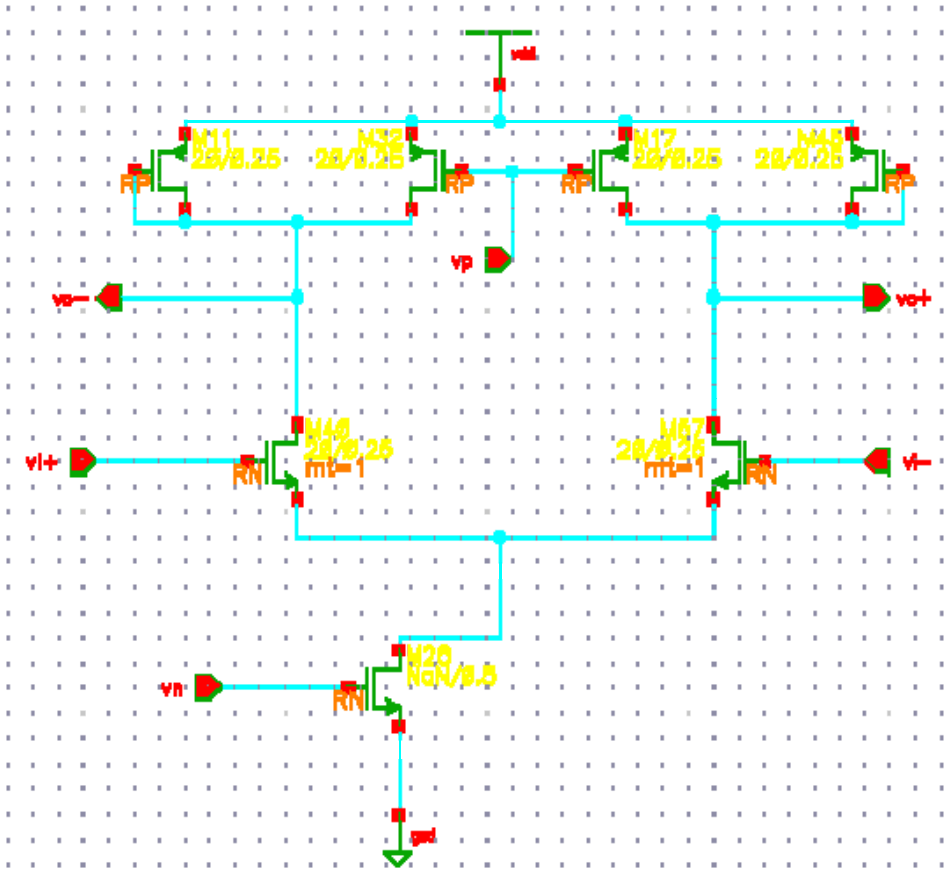
Self-biasing PLL structure

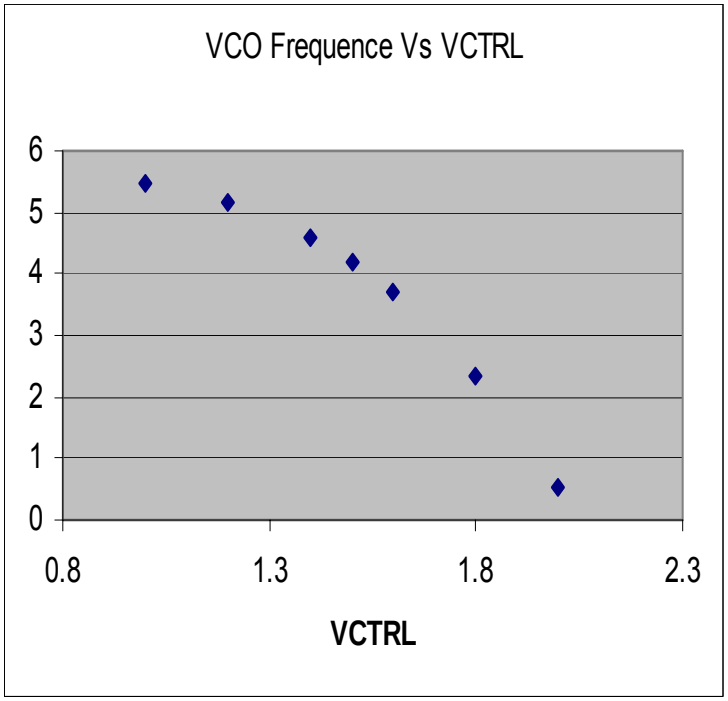


1. Bias generator has strong power noise rejection, result in low jitter.
2. Dump factor and bandwidth to operation frequency ratio are fixed, leading to broad frequency range.

- We have the design for the PFD and the Charge Pump.
- We finished the bias generator and VCO tuning and just started the layout of them.
- Phase noise simulation will follow afterwards.
- The goal is to finish the PLL design before mid Nov. 2008, so that we can concentrate on the CML driver, and then the whole chip layout.

Differential Ring oscillator VCO





We choose this 4-stage VCO, a similar structure as in the GOL. **Schematic level simulation** indicates that a maximum frequency of 5.5GHz can be reached (the typical-typical corner) . We need 2.5 GHz from post layout for 5 Gbps data transmission.

Summary

- The LOC ASIC proposal evolves with time. We incorporate into our LOC design the development from the Versatile Link project (see reports in the optoelectronics working group) and decide to move the optical interface from the LOC to the V.Link. The LOC now is proposed to be a 16:1 serializer. Different interface ASICs or function blocks will be developed according to the application of the LOC.
- Technology evaluation on the 0.25 micron SOS technology produced encouraging positive results and enables us to go ahead with the LOC design using this technology. More studies will be performed on this technology with support from the ADR program.
- The design work for the present prototype, LOC2, is in progress. Simulation on critical components indicate that 5 Gbps serial data rate is hopeful.
- We aim for the April 09 submission, and the tests in lab July 09. We will provide demo-link and system design document for groups that are interested in using this chip in the fall of 2009.