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Status Report on the LOC ASIC

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The LOC ASIC is a serializer for data transmission. This ASIC development is supported by US-ATLAS upgrade program, and is based on a 0.25 μm Silicon on Sapphire technology. Characterization tests on the technology and the first prototype LOC1 have been carried out both in lab and in irradiation tests. Measurement results on jitter and Bit Error Rate of the ASIC as well as the TID and SEE effects will be reported. Design considerations, specifications and simulation results on the second prototype LOC2 will be discussed

Summary

A test-chip has been designed and fabricated to evaluate a 0.25 μm Silicon-on-Sapphire technology for ASIC developments for detector front-end electronics. TID tests using gamma irradiation from a Co-60 source have been carried out on NMOS and PMOS transistors with different layouts on the test-chip. With a floating substrate, different leakage current sources are identified. Threshold voltage shifts are also observed. With an electrically biased substrate, one can "dial"up or down leakage currents in NMOS or PMOS with the potential applied to the substrate. When the substrate is grounded, the leakage currents in NMOS and PMOS are both very small, and the threshold voltage shifts are also reduced compared with the floating substrate case. A crude model has been proposed to explain the observations and a more precise simulation or modeling is needed. More tests are also needed. These tests and modeling work will be carried out in the time from 2008 to 2010.

The first prototype of the LOC ASIC, LOC1 has been measured in lab and in a 200 MeV proton beam at IUCF. The in-lab studies include jitter analysis, bit error rate scan (the bathtub curve) and the eye diagram measurement. In the jitter study, different jitter components are analyzed and their sources identified. The BER measurement of LOC1 is carried out with a 12G BERT and the best BER is found to be 5E-11 in the bathtub scan running at 2.5 Gbps. The eye diagram of the serial bit stream is measured, and from which the signal amplitude, rise and fall times are obtained. Many lessons in the design of LOC1 have been learned and that will help in the LOC2 design. Using TLK2500 as the de-serializer and running at 2.5 Gbps, SEE on LOC1 is measured with a 200 MeV proton beam and the preliminary result indicates that the proton induced SEE has a cross section less than 1E-10 cm2/proton. Data analysis is still on-going. More tests are planned for the summer or fall of 2008. The SEE measurement results will be reported.

A LOC2 design specification is being reviewed in the ATLAS LAr and Inner Detector upgrade communities. This specification will be presented together with the LOC2 design. In the LOC2 design, we try to incorporate the Versatile Link as the LOC's optical interface. Design simulation has been carried out and preliminary results indicate that we may be able to decrease the jitter and increase the serial data speed in LOC2. This design and simulation work is on-going and the latest results will be reported. A schedule on LOC2 will also be discussed.

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