Evaluation of Two SiGe HBT Technologies for the ATLAS sLHC Upgrade

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Overview

- Framework
  - S-LHC radiation levels
  - SiGe proposal
- SiGe Prototype designs
  - Silicon Tracker (SGST)
  - LAr
  - Test chip
- Radiation Studies
  - Neutrons
  - Gammas
- Conclusions
- On-going work

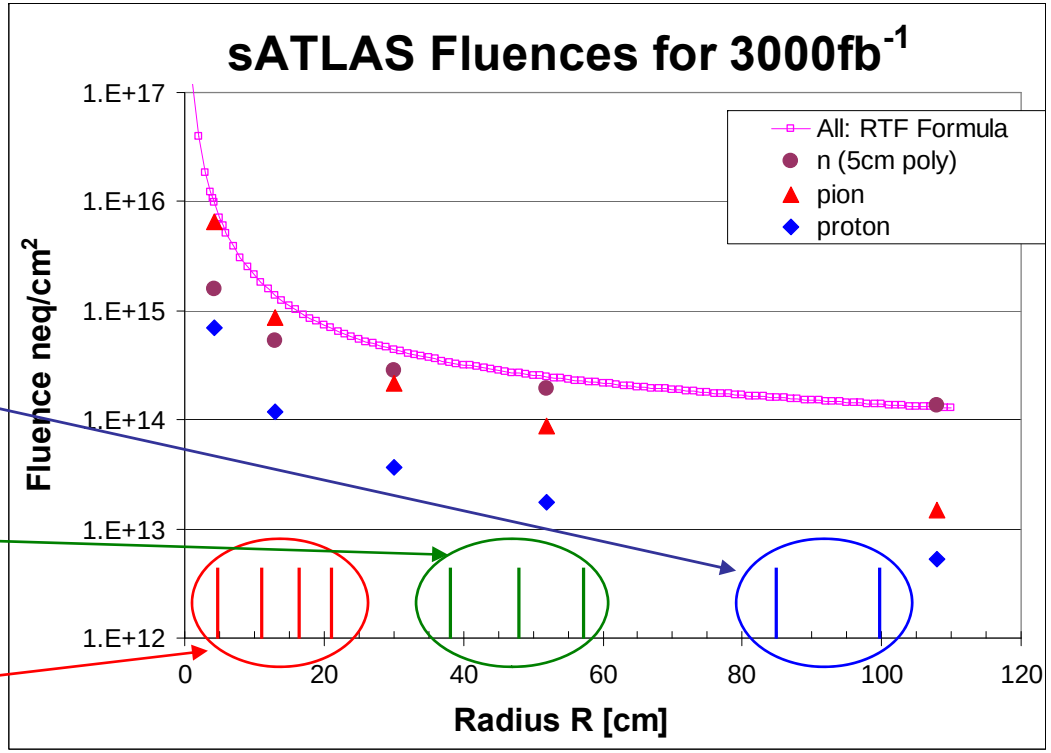
Fluence in Proposed sATLAS Tracker

Radial Distribution of Sensors determined by Occupancy < 2%, still emerging

Long Strips

Short Strips

Pixels



ATLAS Radiation Taskforce http://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/RADIATION/RadiationTF_document.html

5 - 10 x LHC Fluence

Mix of n, p, π depending on radius R

Strips damage largely due to neutrons

Pixels Damage due to neutrons+pions

Design fluences for sensors (includes 2x safety factor) **:**

Innermost Pixel Layer (r=5cm):	$1.4*10^{16}$ neq/cm^2	712 MRad
Outer Pixel Layers (r=11cm):	$3.6*10^{15}$ neq/cm^2	207 MRad
Short strips (r=38cm):	$6.8*10^{14}$ neq/cm^2	30 MRad
Long strips (r=85cm):	$3.2*10^{14}$ neq/cm^2	8.4 MRad

Radiation Targets for Now

- There are no firm specifications yet for radiation levels, but based upon these simulation studies and the working “strawman layout” and consistent with the radiation levels to which the silicon sensor group is testing, we are presently targeting these values (which include one safety factor of 2).

– Short Strips	6.8×10^{14} neq/cm^2	30 Mrad
– Long Strips	3.2×10^{14} neq/cm^2	8.4 Mrad
– LAr	9.6×10^{12} neq/cm^2	30 krad

Why SiGe

- The silicon microstrip detector (Si Strip Tracker: 5pF to 16pF) and the liquid argon calorimeter (LAr: 400pF to 1.5nF) for the ATLAS upgrade present rather large capacitive loads to the readout electronics.
- To maintain shaping times in the tens of nanoseconds, CMOS front-ends must increase bias currents to establish large enough transconductance.
- The extremely low base resistances of SiGe HBTs can accomplish this with relatively low bias currents thus affording possible power reduction.
- The low base resistance also minimizes the intrinsic base resistance noise allowing a good S/N ratio

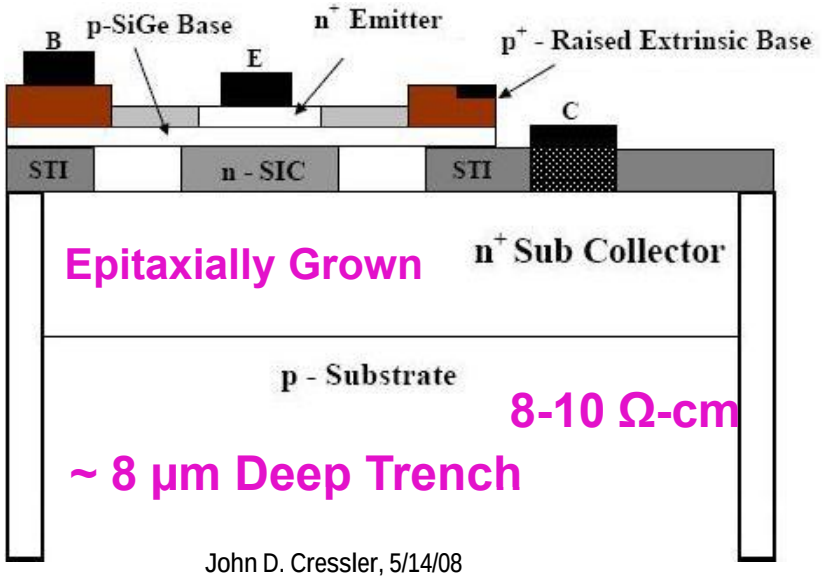
- IBM provides two SiGe technologies along with their 130 nm CMOS as fully BiCMOS technologies.
  - The 8HP process and the less expensive 8WL process.

2 IBM SiGe techs.

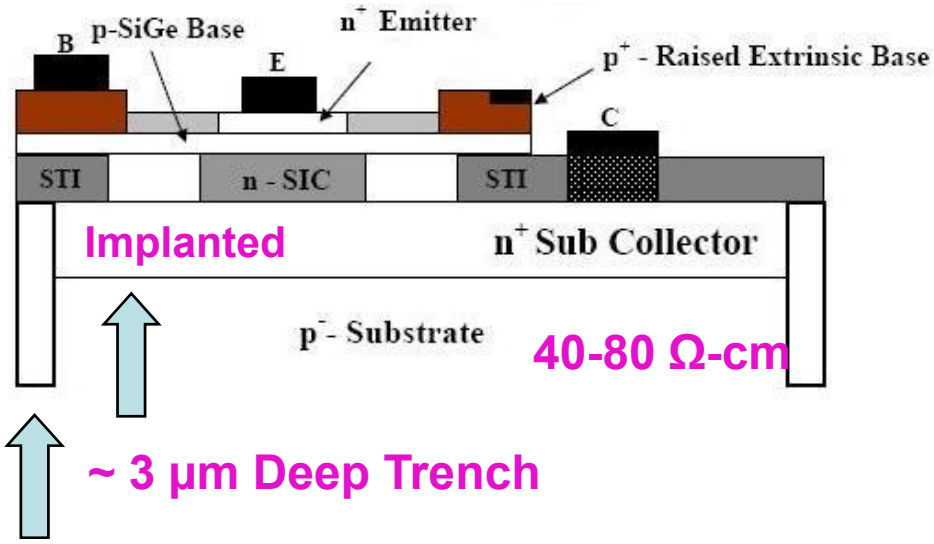
Georgia Institute of Technology

- **Cost-Performance Platform Incorporating 130 nm SiGe HBTs**
  - implanted subcollector **(much shallower subcollector-substrate jx)**
  - "shallow" deep trench isolation **~ 3 μm (vs. 8 μm for 8HP)**
  - lightly doped substrate **~ 40-80 Ω-cm (vs. 8-10 Ω-cm for 8HP)**
  - 100 / 200 GHz peak f_T / f_{max} **(vs. 200 / 285 GHz for 8HP)**

8HP SiGe HBT



8WL SiGe HBT

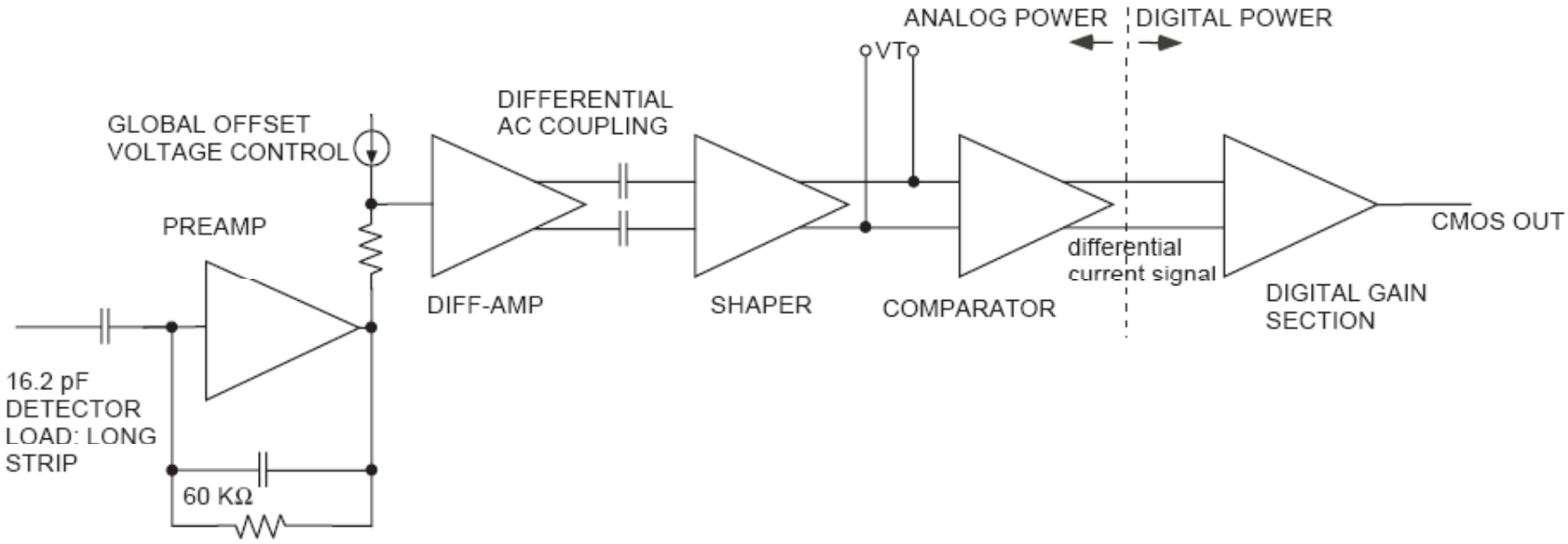


SGST Overview

SiGe Silicon Tracker readout test chip

- Circuit development goal: **minimize power** and meet SCT noise and 25 ns crossing specs.
- IBM **8WL process** is used, 0.13 μm 8RF CMOS with SiGe 140 Ghz npn added. To be submitted to MOSIS on **October 20**, 2008.
- Two detector loads simulated, including strays, of 5.5 pF for VT= 0.5 fC and 16 pF for VT = 1 fC. This corresponds to **2.5 cm and 10 cm strip lengths**.
- Threshold and bias adjustment for device matching skew is included in design, using **different strategy** than ABCD or ABCNext, **for lowered power rail to 1.2 V**.
- **Resistive front transistor feedback** used to reduce shot noise from feedback current source. For long strips, this is good strategy for bias.
- **Shaping time adjustable** over +/- 15 % range.
- Overall, SiGe allows **large current reduction** in each analog stage as compared to 0.13 μm CMOS.
- Actual CMOS design is needed to quantify the power difference.
  - SGST **0.2 mW/channel for long strips load sets a comparison point** with CMOS.

BLOCK DIAGRAM AND POWER FOR SiGe SCT FRONT-END



SGST biases total: 168 uA @ 16.2 pF (1350 e-), 108 uA @ 5.5 pF(900 e-)

POWER @1.2 Volt RAIL: 0.202 mW/channel @ 16.2 pF, VT=1fC
0.130 mW/channel @ 5.5 pF, VT=0.5 fC

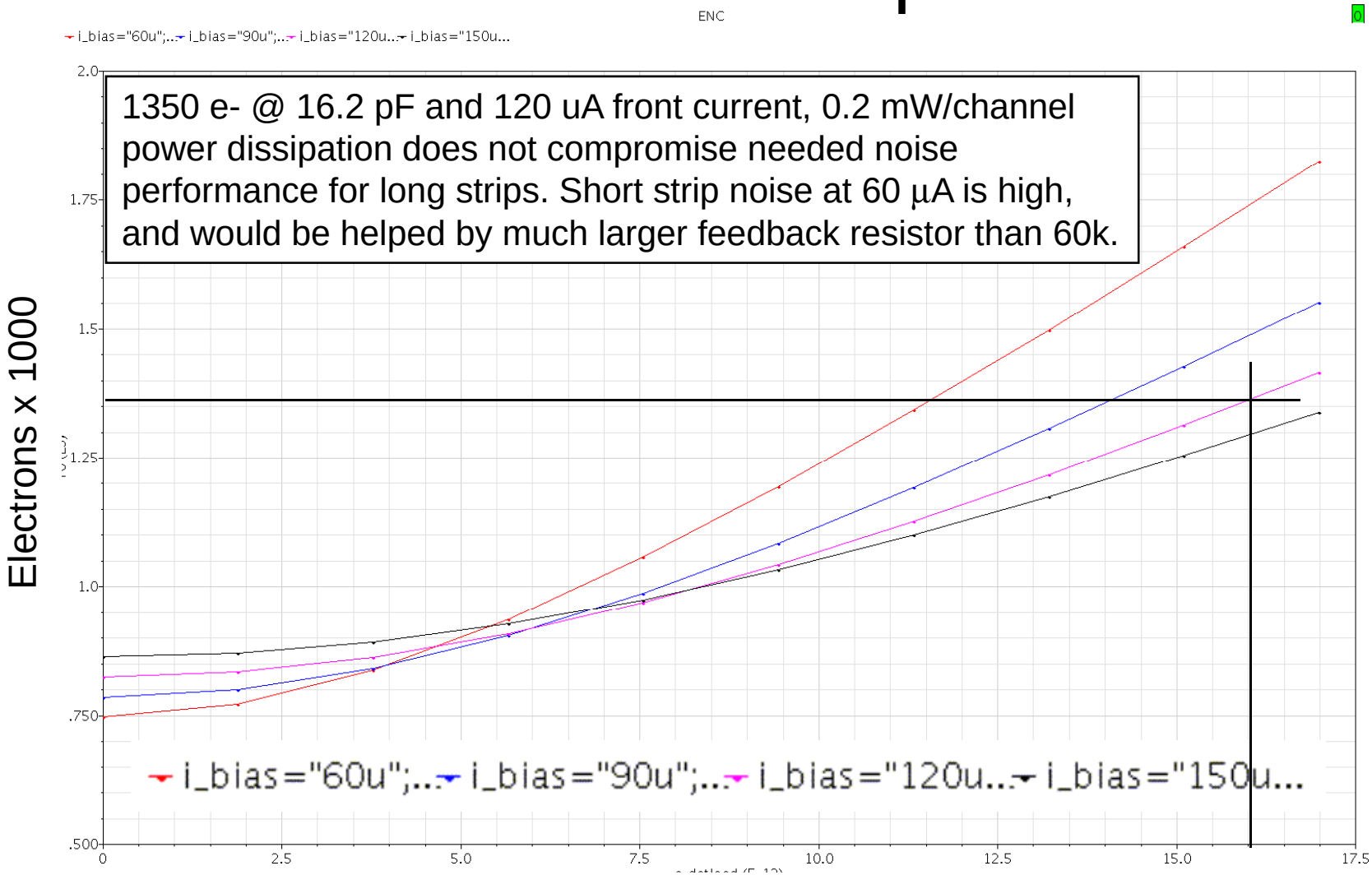
0.2 mW/channel compares with ~1 mW for current SCT front-end.
This is an essential power dissipation improvement!

SiGe technology allows very low power analog design.

Edwin Spencer, SCIPP

Edwin Spencer, SCIPP

SGST Simulated ENC performance



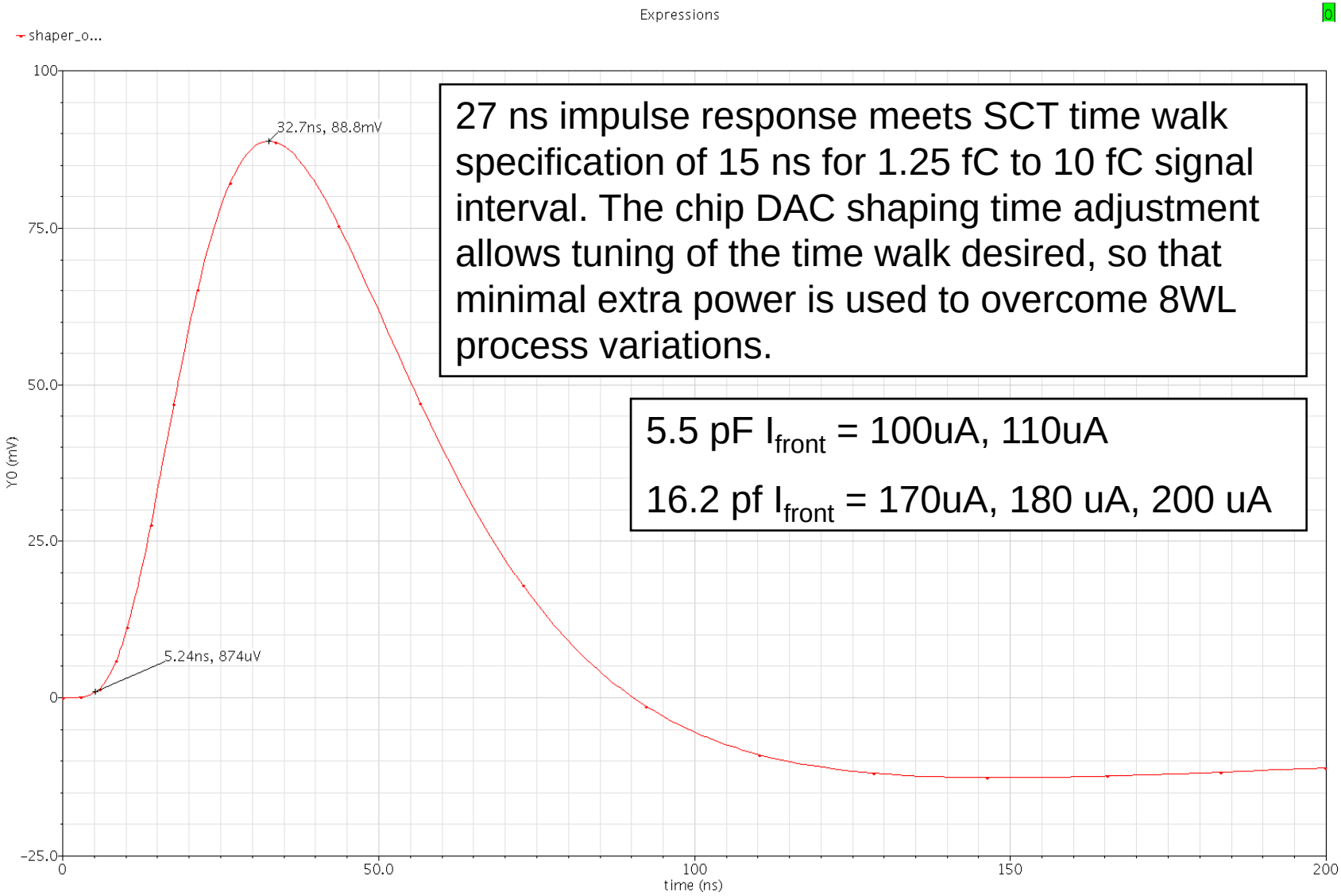
Electrons x 1000

Total Detector Capacitance (pF)

600 nA detector leakage is included.

Edwin Spencer, SCIPP

Impulse Response at Comparator



27 ns impulse response meets SCT time walk specification of 15 ns for 1.25 fC to 10 fC signal interval. The chip DAC shaping time adjustment allows tuning of the time walk desired, so that minimal extra power is used to overcome 8WL process variations.

5.5 pF I_{front} = 100uA, 110uA

16.2 pf I_{front} = 170uA, 180 uA, 200 uA

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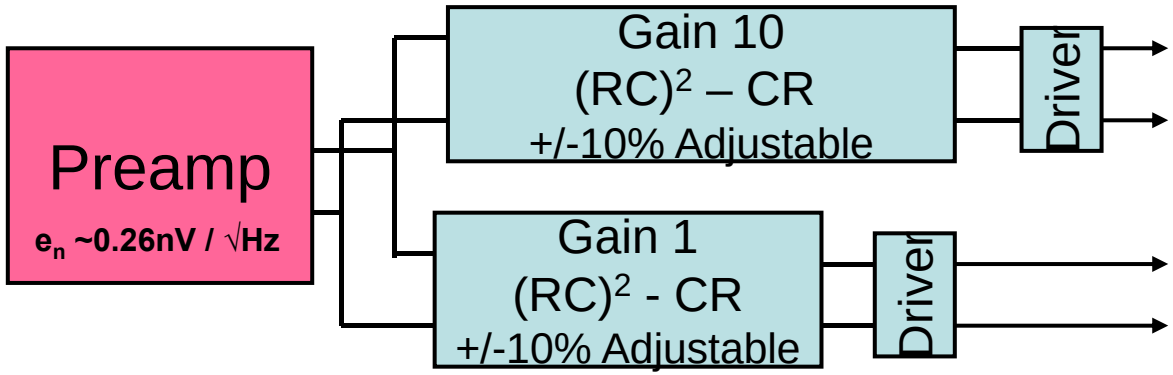
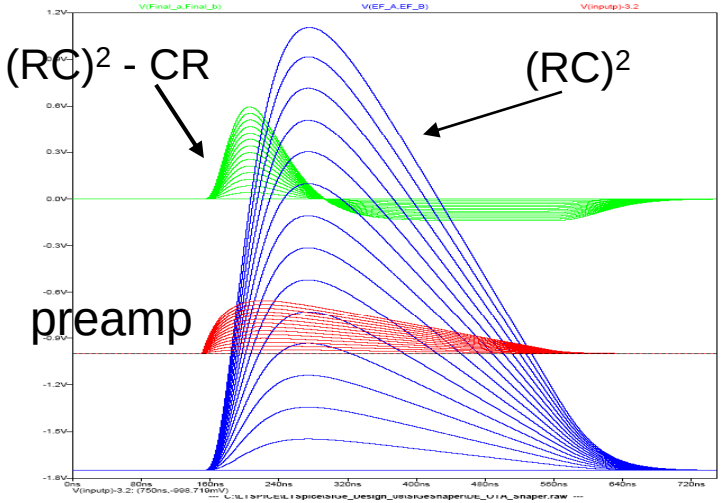
Prototype LAr Preamp and Shaper co-submission with SCT in 8WL

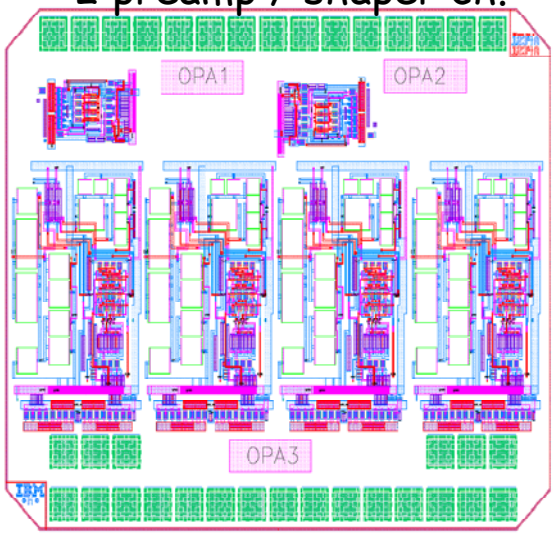


0-5mA Input LAr Input
0.1% Linearity
14 bit Dynamic Range
~200mW / ch

0 – 700uA Into Preamp Gain 10

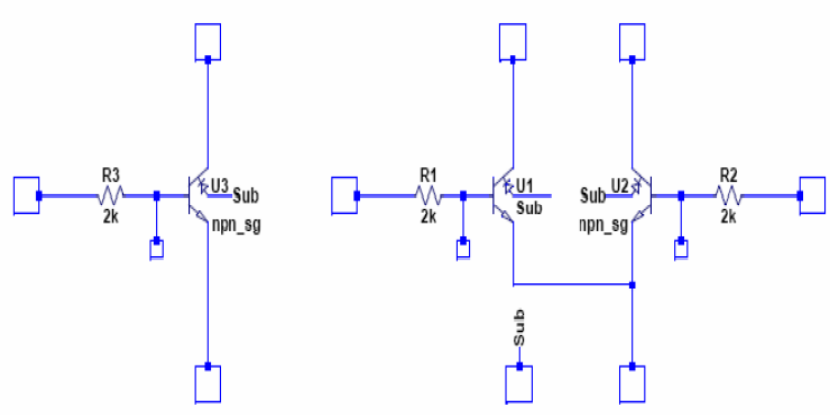


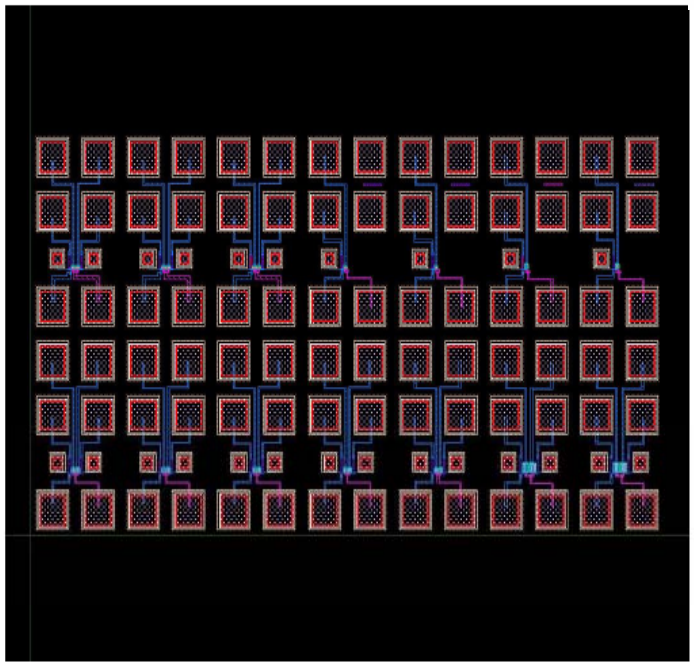
LAr Chiplet 1.8mm^2
2 preamp / shaper ch.



8WL Test Structures co-submission with SCT and LAr Chiplets

8WL Bipolar Test Structures
Standard Kit Devices
All 0.12 emitter width

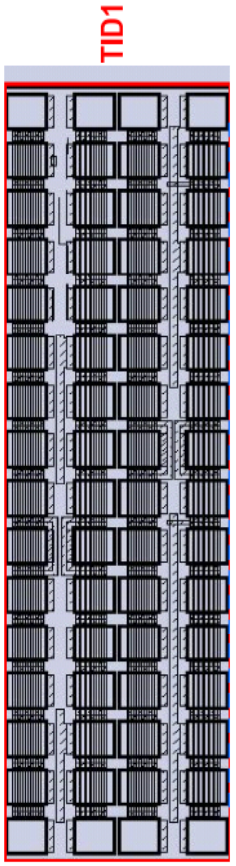




Item	(HP transistors) Quantity	
1um diffpair		3
8um diffpair		5
20um/2stripe diffpair		2
1um npn		2
8um npn		2
Opndres		1
Opppcres	1	
Oprppres	1	
Oprrpres		1

CERN Micro Electronics Group CMOS8RF Test Structure Ported to 8WL for Direct CMOS comparison

MPW CERN CMOS Test Structures 0.6mm X 2mm



8WL CMOS

Device	Size	Pad count
2.2nm gate oxide devices		
NMOS W array, L=0.12	W=0.16, 0.32, 0.48, 0.64, 0.8, 2	8 (s, g, 6xd)
NMOS L array, W=10	L=1, 10	3 (g, 2xd)
NMOS edgeless (ELT)	W=min, L=0.12	1 (d)
NMOS ZVt	W=3, L=0.42	1 (d)
NMOS ZVt edgeless (ELT)	W=min, L=0.42	1 (d)
NMOS triple well array, L=0.12	W=0.16, 1	2 (2xd)
PMOS W array, L=0.12	W=0.16, 0.48, 0.8, 2	6 (s, g, 4xd)
PMOS L array, W=10	L=1, 10	3 (g, 2xd)
		25
5.2nm gate oxide devices		
NMOS W array, L=0.24	W=0.36, 0.50, 0.8, 2	6 (s, g, 4xd)
NMOS L array, W=10	L=1, 10	2 (2xd)
NMOS edgeless (ELT)	W=min, L=0.26	1 (d)
NMOS ZVt	W=2.94, L=0.56	1 (d)
NMOS ZVt edgeless (ELT)	W=min, L=0.56	1 (d)
NMOS triple well array, L=0.24	W=0.36, 1	2 (2xd)
NMOS with metal filling on top	W=0.36, L=0.24	1 (d)
PMOS W array, L=0.24	W=0.36, 0.50, 0.8, 2	6 (s, g, 4xd)
PMOS L array, W=10	L=1, 10	2 (2xd)
		22
Resistors		
OP N+ diffusion resistor	L=0.28, 1.50 (R=11.66 and 2.40 kΩ respectively)	3
		3
FOXFETs		
Nwell/Nwell foxfet array, W=200	L=0.92, 1.48	3
N+diff/N+diff foxfet, W=200	L=0.18	2
N+diff/Nwell foxfet array, W=200	L=0.3, 0.6	2
		7
Diodes		
Forward biased diodes array p+ in Nwell, Area = 1680 μm^2	Large perimeter (2.434mm), small perimeter (164µm),	3

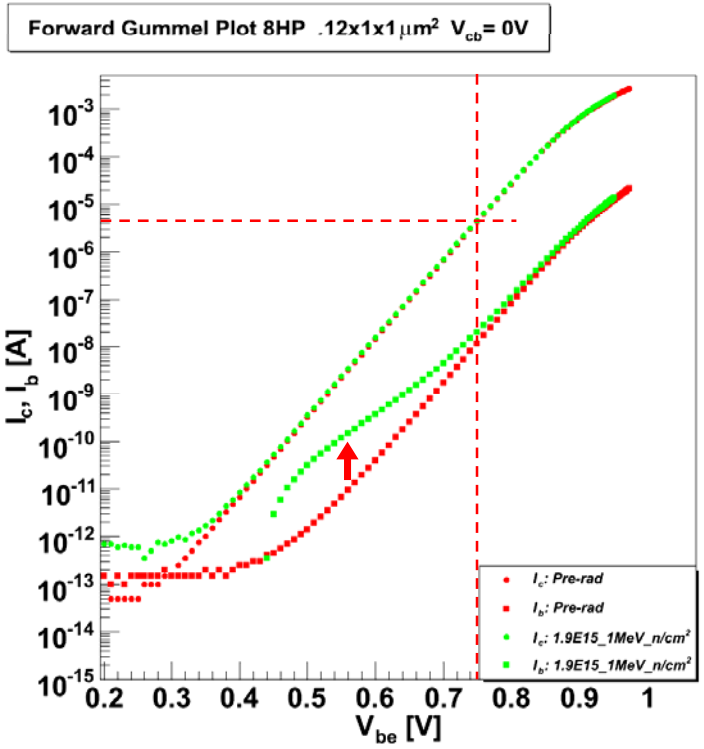
Radiation Studies

- 2 IBM BiCMOS SiGe technologies being evaluated using “spare” test chips from IBM
  - 8HP
  - 8WL
- Gamma irradiations
  - Brookhaven National Laboratory
  - Doses: 10, 25, 50 Mrads(Si)
  - Biased – shorted – floating
- Neutron irradiations
  - TRIGA Nuclear Reactor, Jozef Stefan Institute, Ljubljana, Slovenia
  - Fast Neutron Irradiation (FNI) Facility, University of Massachusetts Lowell Research Reactor
  - Fluences: 2×10^{14}, 6×10^{14}, 1×10^{15}, 2×10^{15} eq. 1 MeV neutrons/cm^2

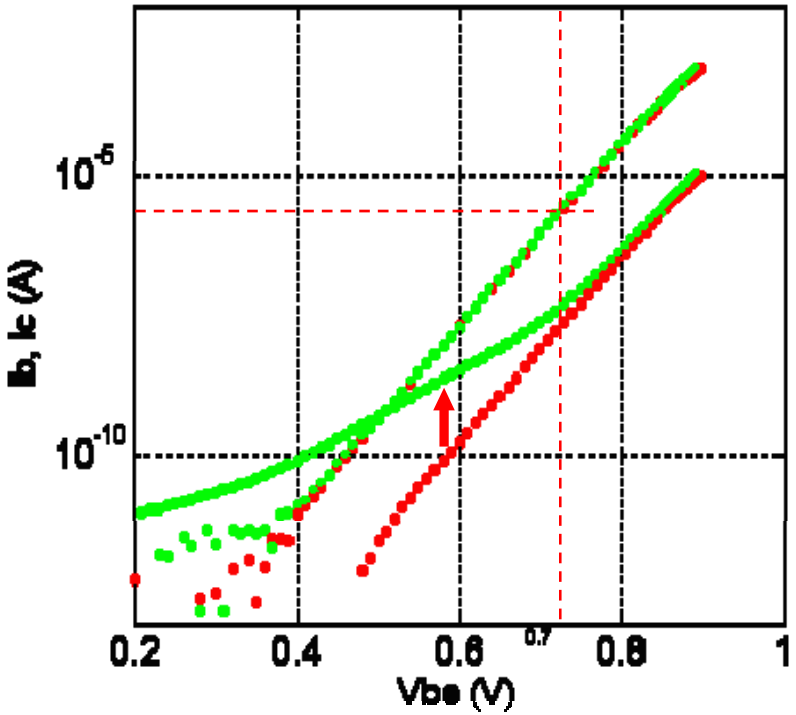
Radiation Damage – Neutrons

- Forward Gummel Plots of SiGe Bipolar transistors:
  - ➢ Base current increase ⇒ Current gain (β) decreases at relevant current densities

8HP



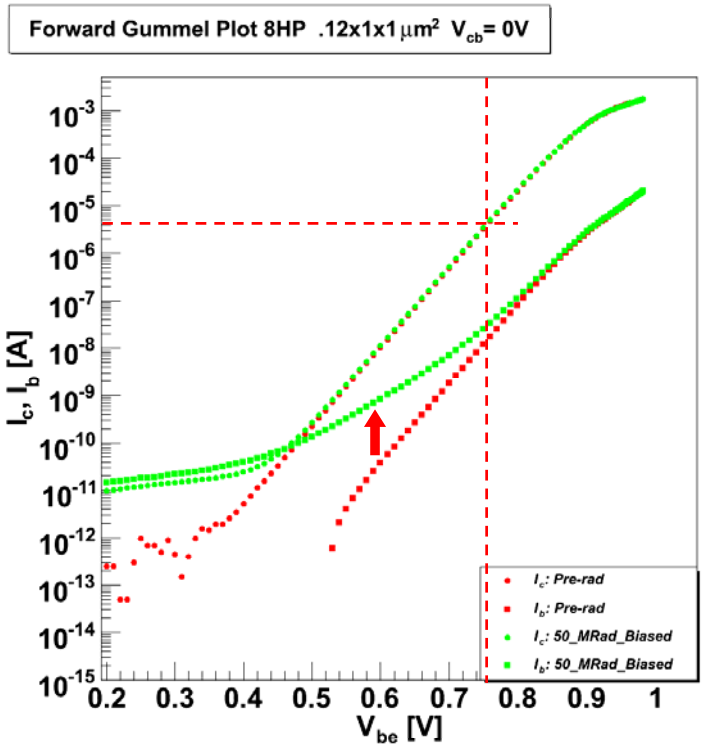
8WL



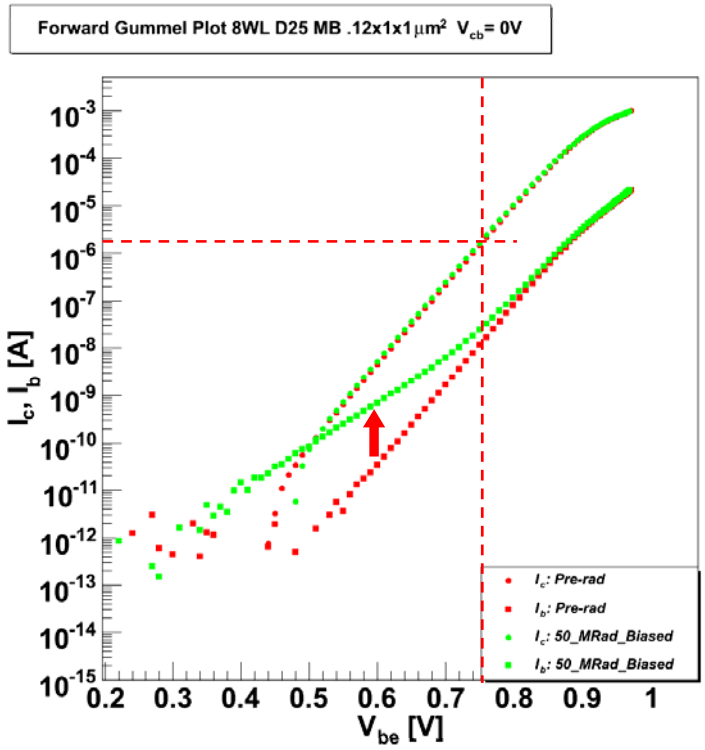
Radiation Damage - Gammas

- Forward Gummel Plots of SiGe Bipolar transistors:
  - ➢ Base current increase ⇒ Current gain (β) decreases at relevant current densities

8HP



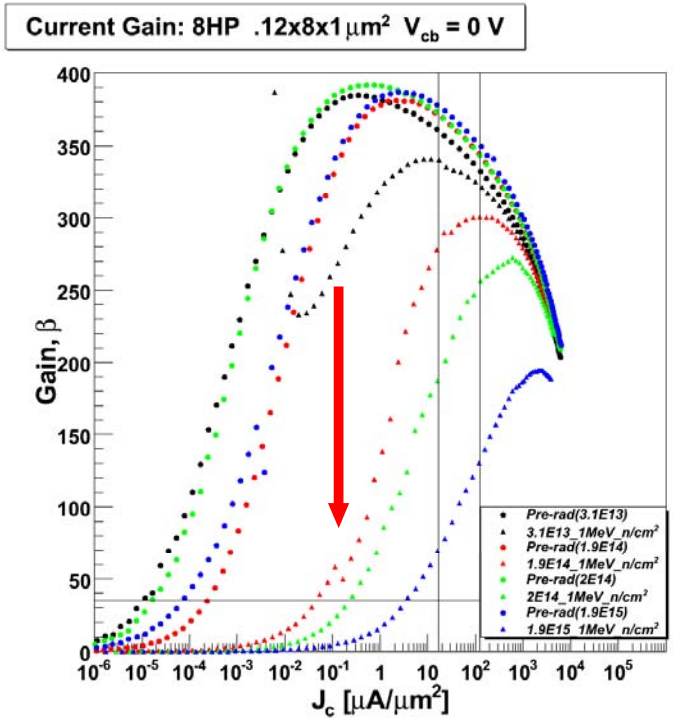
8WL



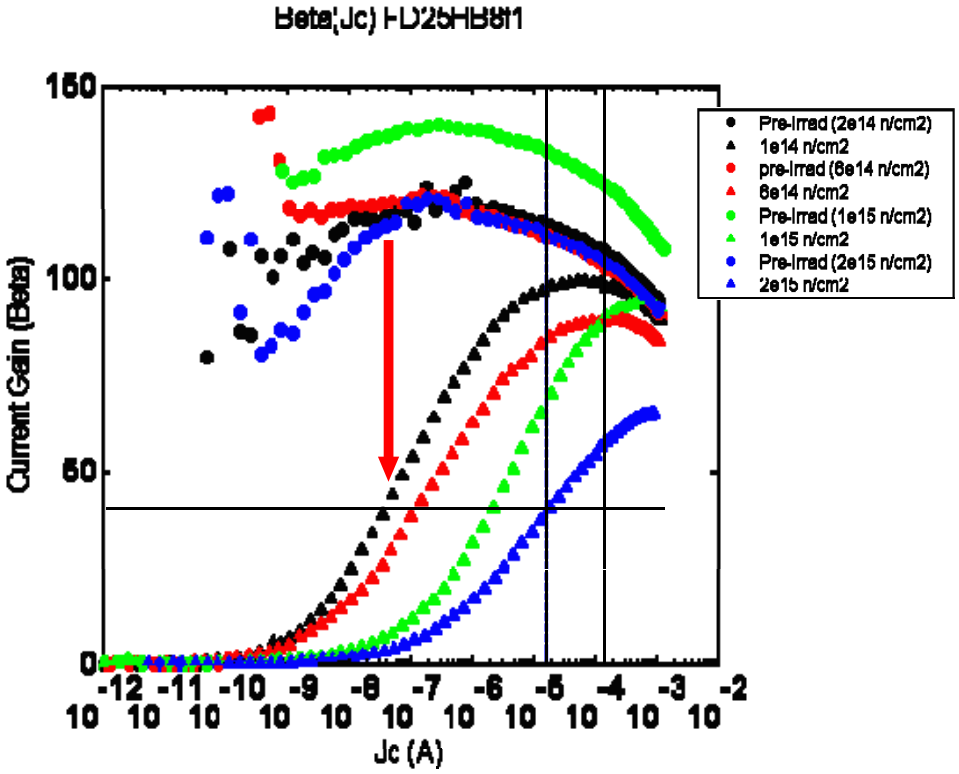
Current gain (β) vs. J_C – Neutrons

- Beta vs. injection level (collector current density)
  - ➢ High transistor damage although very dependent on injection level

8HP



8WL



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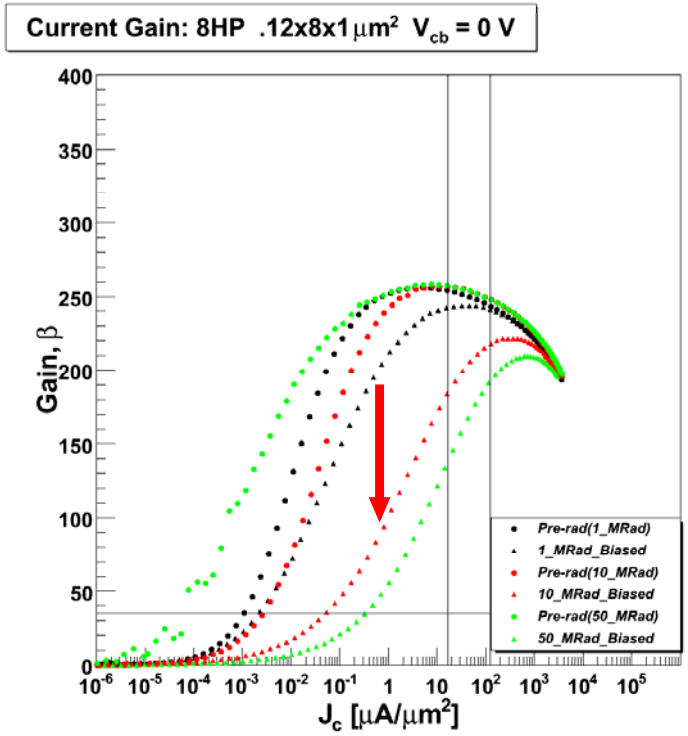
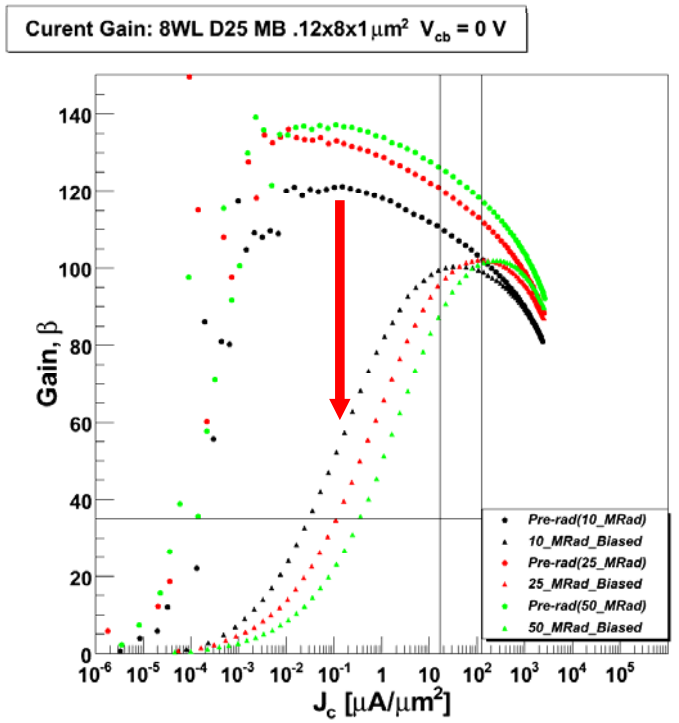
8HP



8WL



Reciprocal gain – Neutrons

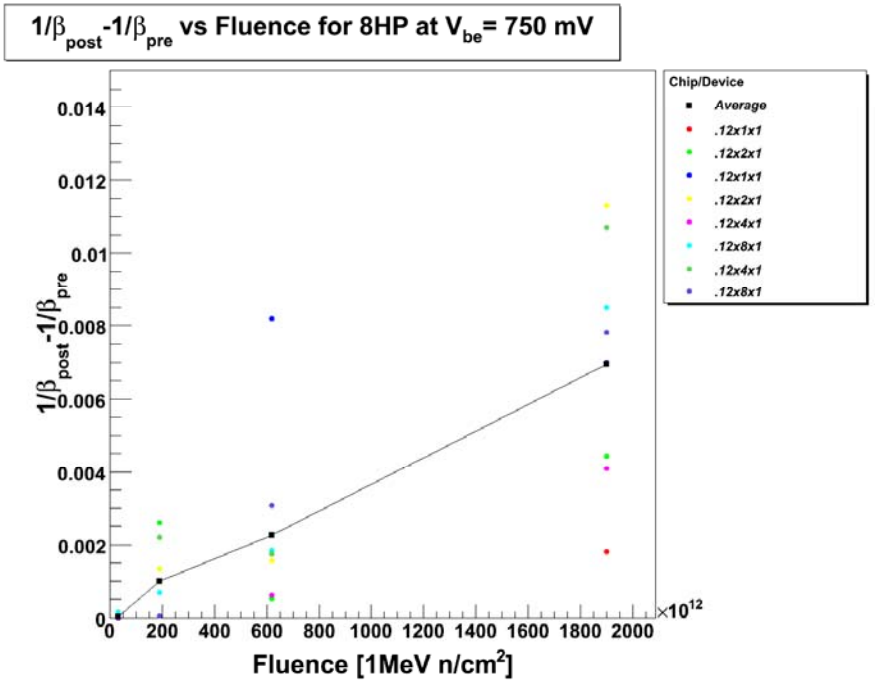
- $\Delta(1/\beta) = 1/\beta_F - 1/\beta_0$ (@V_{BE} = 0.75 V)
- Linear with fluence as expected
- High dispersion among transistor types

G. C. Messenger et al:

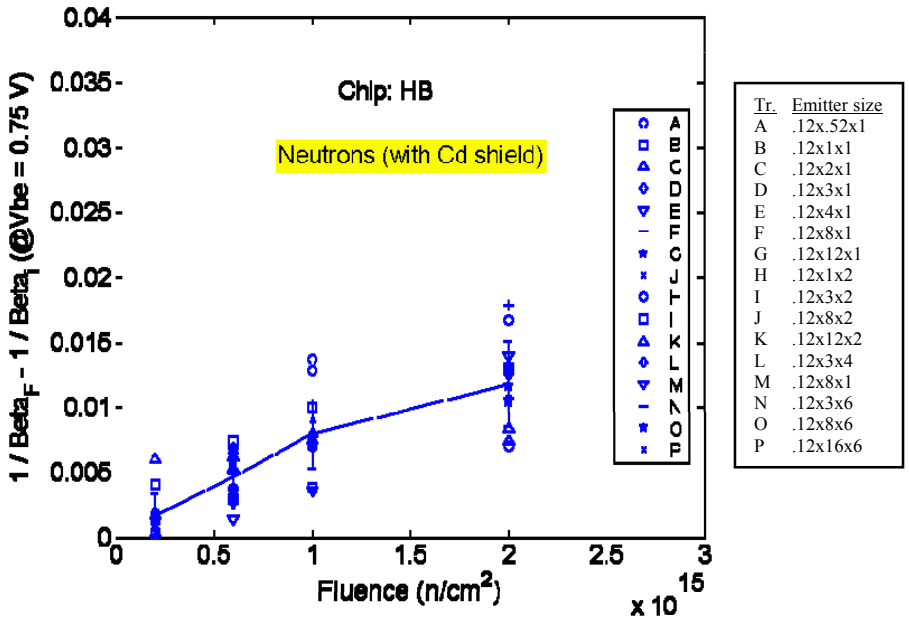
$$\frac{1}{h_{fe}} = \frac{1}{h_{fe0}} + K(E)\Phi$$

where the term $1/h_{fe0}$ is the initial reciprocal gain, $K(E)$ is the particle- and energy-dependent displacement damage factor, and Φ is the incident particle fluence.

8HP



8WL

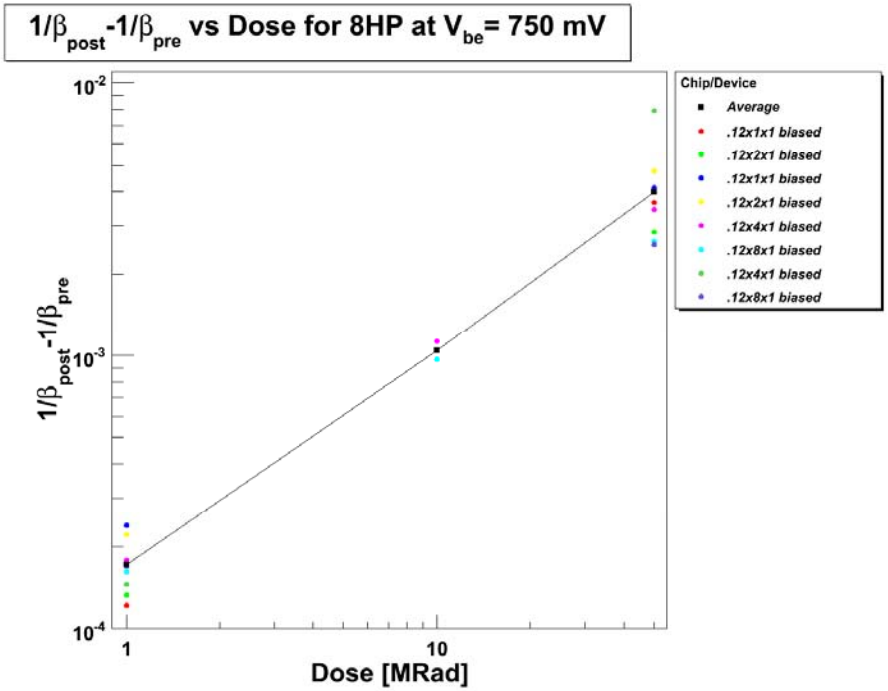


Tr.	Emitter size
A	.12x.52x1
B	.12x1x1
C	.12x2x1
D	.12x3x1
E	.12x4x1
F	.12x8x1
G	.12x12x1
H	.12x1x2
I	.12x3x2
J	.12x8x2
K	.12x12x2
L	.12x3x4
M	.12x8x1
N	.12x3x6
O	.12x8x6
P	.12x16x6

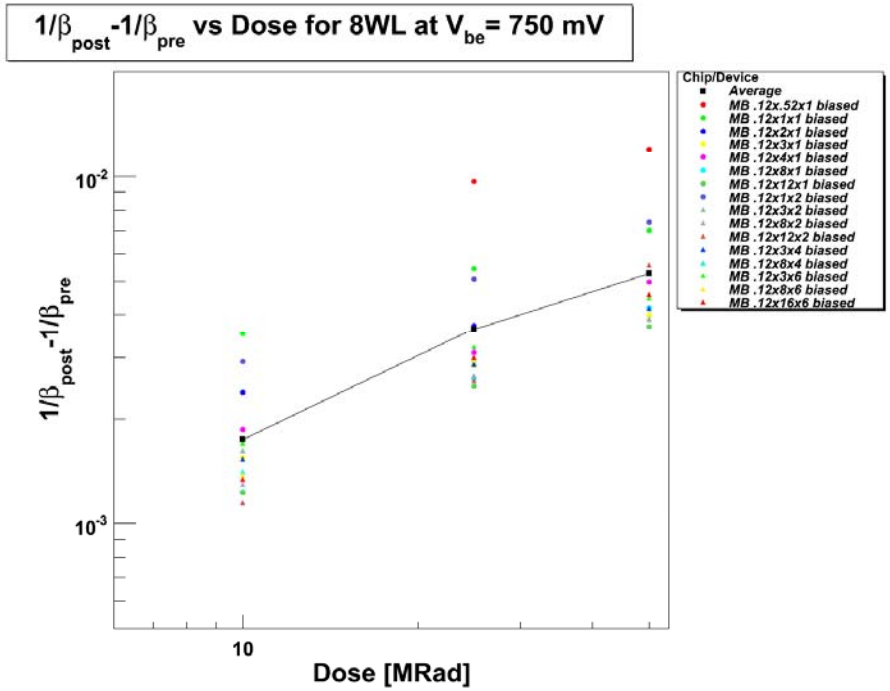
Reciprocal gain – Gammas

- Linear in the log-log axis $\Delta(1/\beta) \propto (dose)^a$
- High dispersion in 8WL results

8HP



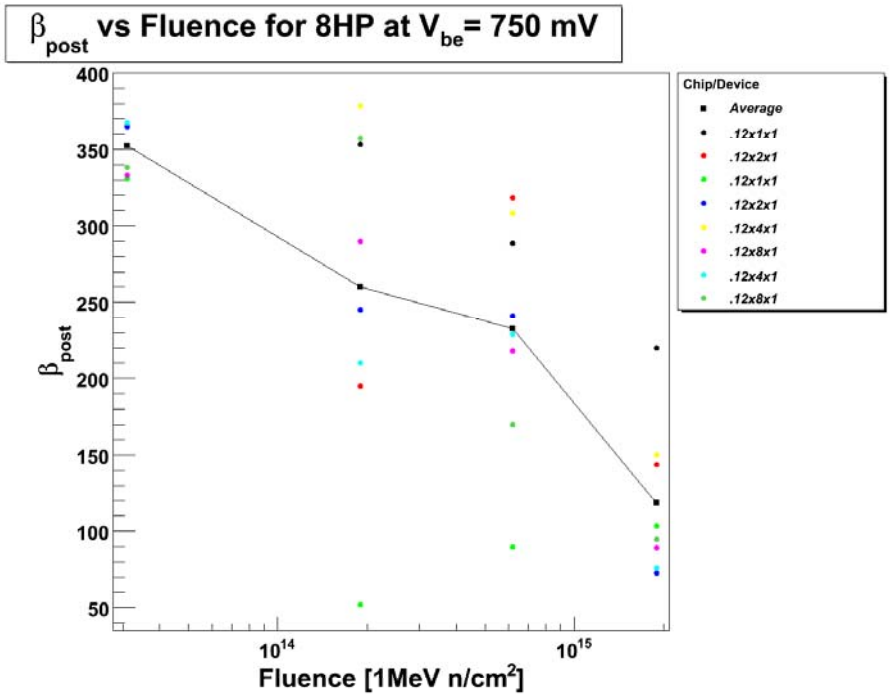
8WL



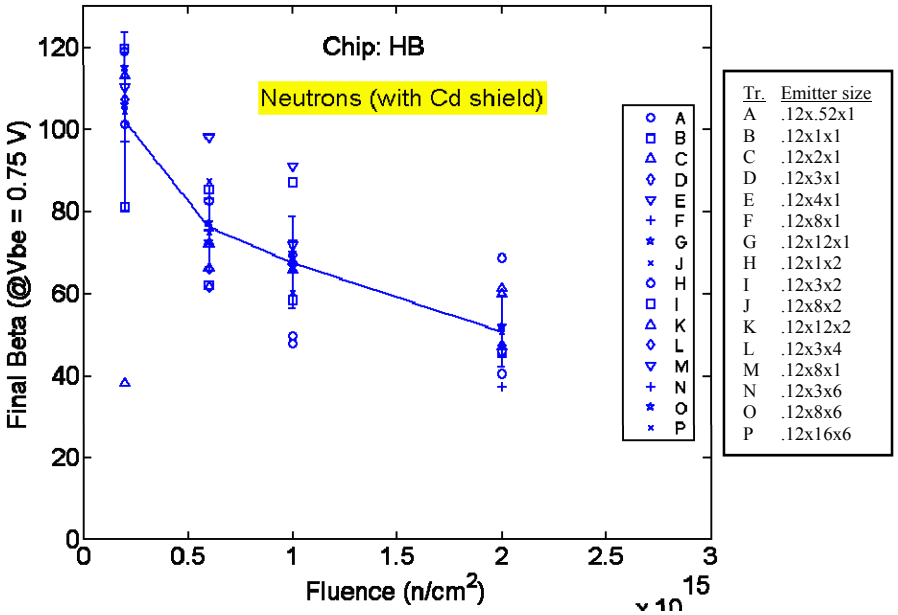
Final Transistor gain – Neutrons

- $\beta_F >> 50$ (@$V_{BE} = 0.75$ V) after 6 x 10^{14} eq. 1 MeV n/cm^2
- Higher final gains in 8HP transistors (also pre-irrad)
- Some dispersion specially in 8HP transistors

8HP



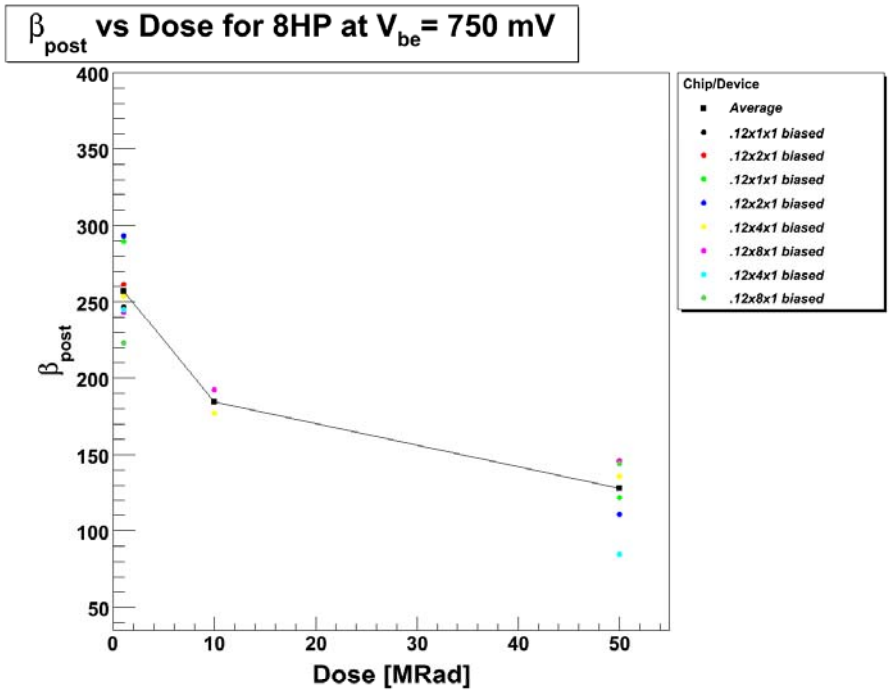
8WL



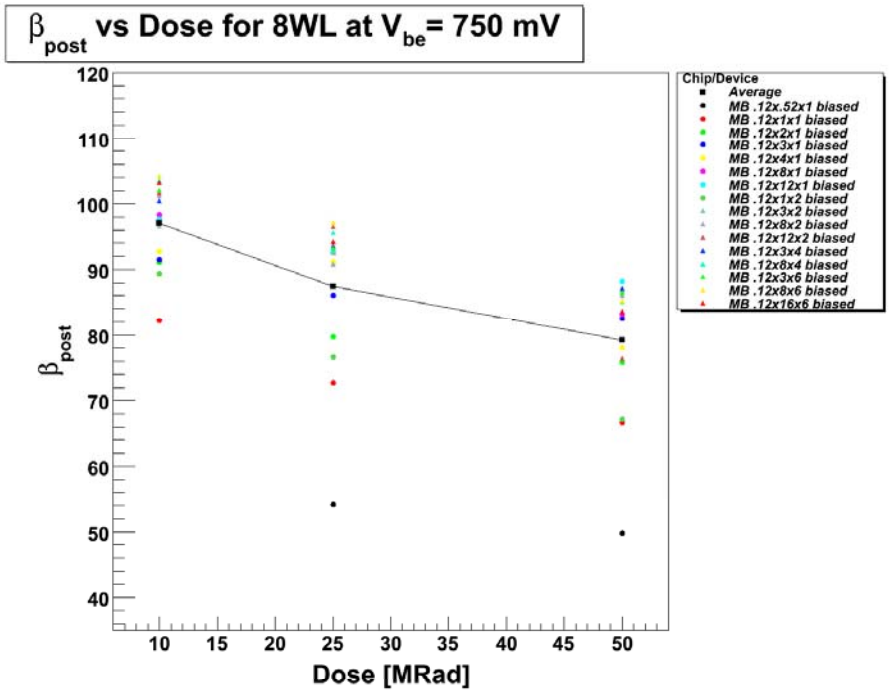
Final Transistor gain – Gammas

- β_F >> 50 (@V_{BE} = 0.75 V) after 50 Mrads
- Also higher final gains in 8HP transistors
- Some dispersion in 8WL transistors

8HP

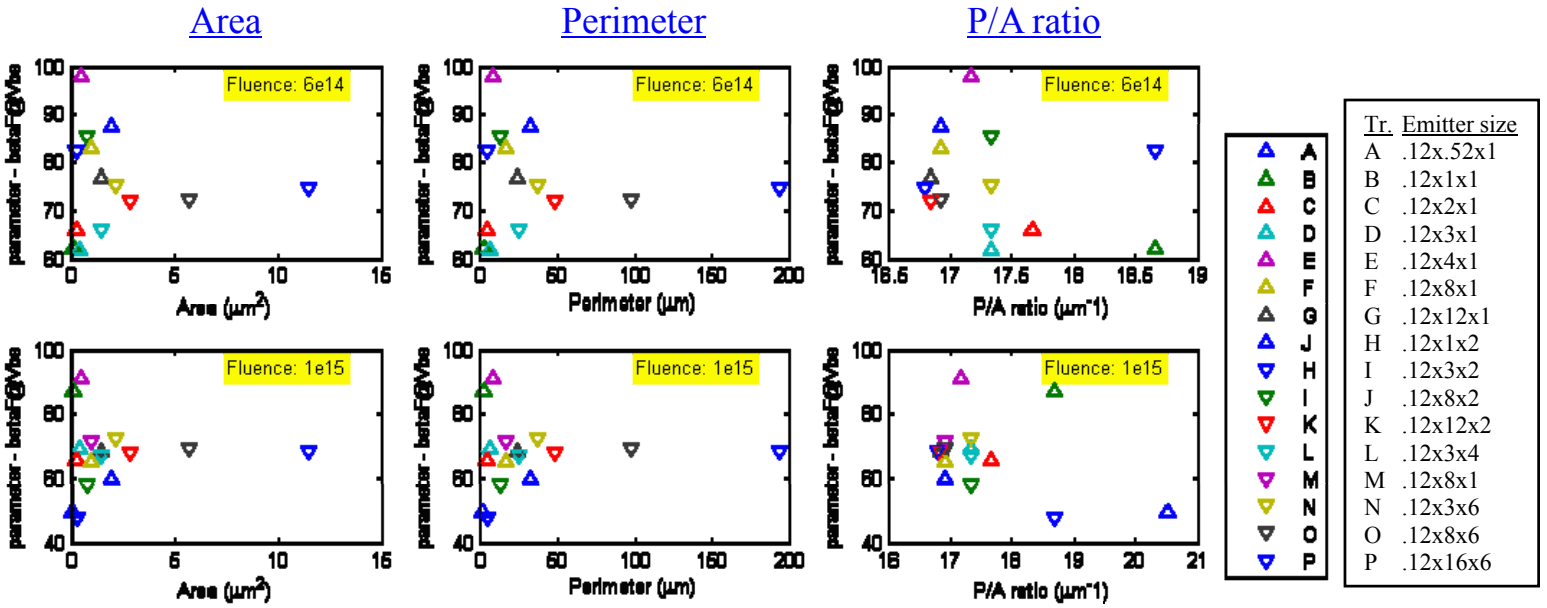


8WL



Dispersion

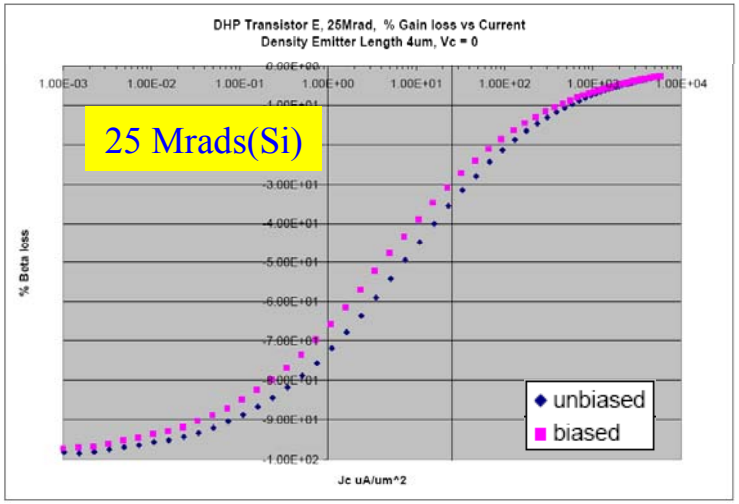
- High dispersion in radiation results among transistors, especially in 8WL.
- It is not related with emitter geometry:

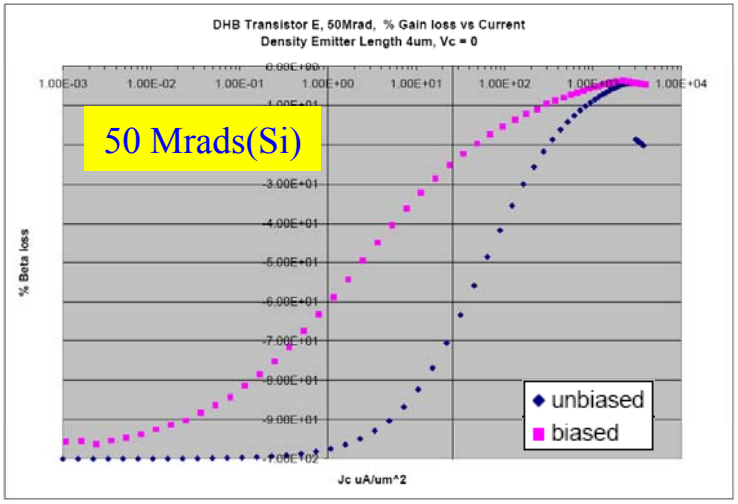


- We believe it is due to problems or variability in the test structure.
- We do not know the real cause, but we want to try with our own test chip made with design-kit transistors in case it is related to that.

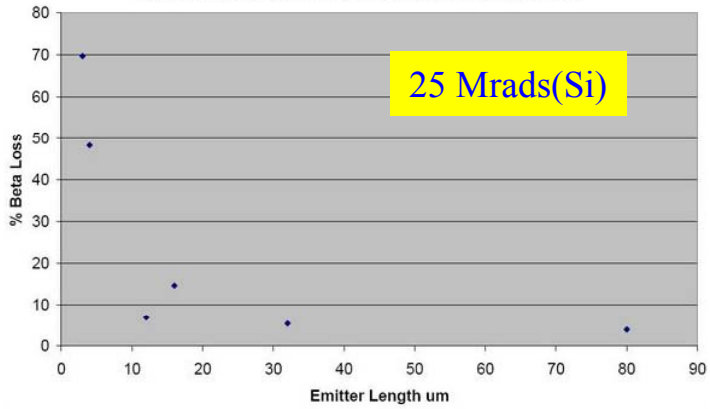
Bias effects studies

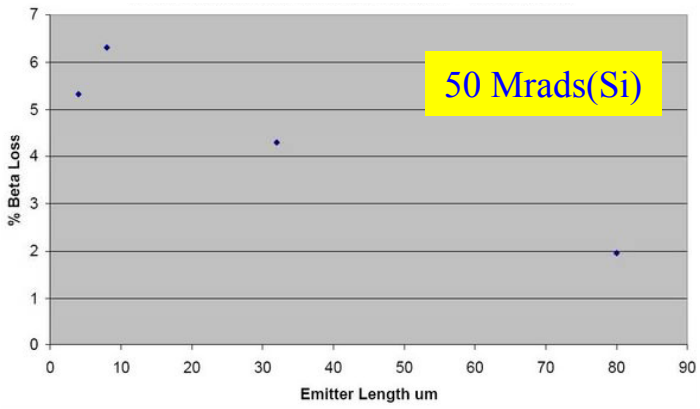
- Effects very dependent on total dose





- Seems to be a strong correlation between emitter length and beta damage for the unbiased transistors





Conclusions

- The electrical characteristics of both SiGe technologies make them good candidates for the front-end readout stage for sensors that present large capacitive loads and where short shaping times are required, such as the upgraded ATLAS silicon strip detector (especially long strip version) and the liquid argon calorimeter.

- The devices experience performance degradation from ionization and displacement damage.
    - The level of degradation is manageable for the expected radiation levels of the upgraded ATLAS LAr calorimeter and the silicon strip tracker.
    - The dispersion of final gains after irradiation may be a concern which warrants further investigation.
    - The initial quality of the test structures may be clouding the higher fluence results.

On-going work

- Fabrication of Si tracker and LAr readout circuits, plus a custom designed test structure array.
- Pre and post irradiation testing of all three fabrications.
- Low Dose Rate Effects (LDRE) study.