

Evaluation of Two SiGe HBT Technologies for the ATLAS sLHC Upgrade

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Abstract

As previously reported, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technologies promise several advantages over CMOS for the front-end readout electronics for the ATLAS upgrade. Since our last paper, we have evaluated the relative merits of the latest generations of IBM SiGe HBT BiCMOS technologies, the 8WL and 8HP platforms. These 130nm SiGe technologies show promise to operate at lower power than CMOS technologies and would provide a viable alternative for the Silicon Strip Detector and Liquid Argon Calorimeter upgrades, provided that the radiation tolerance studies at multiple gamma and neutron irradiation levels, included in this investigation, show them to be sufficiently radiation tolerant.

I. INTRODUCTION

SiGe technologies are known for their high transconductance at low current. BiCMOS Silicon-germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technologies are of interest for high luminosity applications in high energy physics because they have the benefit of requiring less power than standard CMOS technologies while still having low noise and fast shaping times even after exposure to high radiation levels [1]. The silicon microstrip detector and the liquid argon calorimeter for the ATLAS upgrade present rather large capacitive loads to the readout electronics (Si Strip Tracker: 5 pF to 16 pF; LAr: 400 pF to 1.5 nF). In order to maintain shaping times in the tens of nanoseconds, CMOS front-ends must increase bias currents to establish large enough transconductance. However, the extremely low base resistances of SiGe HBTs can accomplish this with relatively low bias currents thus affording possible power reduction. Their low base resistance also minimizes the intrinsic base resistance noise allowing a good signal-to-noise ratio.

Prototype readout circuits using the IBM's 8WL SiGe HBT technology are currently planned for submission. The prototype circuits are designed to explore their possible use in the upgrade of the Silicon Strip Detector and Liquid Argon

Calorimeter of the ATLAS detector as part of the Large Hadron Collider upgrade (sLHC) [2][3]. In these applications, power consumption is a critical parameter, which must be minimized. These preliminary circuit designs have been used to guide the assessment of relevant device parameters. The design of a low noise amp (LNA) with SiGe 8WL technology is presented.

In order to determine if SiGe technologies can survive the radiation environment of the upgraded ATLAS detector, an investigation was made to assess the radiation hardness of the two latest generation IBM SiGe platforms, 8WL and the 8HP. This is a follow up to a previous paper from this 2005 conference where only very early results were presented [4]. Previous IBM SiGe generations have already been reported to be quite radiation tolerant up to a high dose, showing post-radiation current gains well above workable limits [5][6][7]. Compared to 8HP, 8WL is a lower cost option, with 100 GHz peak f_T versus 200 GHz for 8HP, and has reduced depth deep trench isolation, a thinner, implanted sub-collector, and a higher resistivity substrate. Both are available with a 130 nm CMOS technology to provide high-speed BiCMOS ASIC solutions.

This radiation study envelopes the predicted target radiation levels that will be reached at 60 and 20 cm radii in the upgraded ATLAS detector. There are no firm specifications yet for radiation levels, but based upon the simulation studies [8] and the working "strawman layout" [9], and consistent with the radiation levels to which the silicon sensor group is testing, we are presently targeting the following values (which include one safety factor of 2). For the silicon strip detector the current studies predict 30 Mrad(Si) of total ionizing dose (TID) and $6.8 \times 10^{15} \text{ cm}^{-2}$ 1 MeV equivalent neutron fluence in the "short-strips" region, and 8.4 Mrad(Si) - $3.2 \times 10^{14} \text{ cm}^{-2}$ in the "long-strips" region, while the radiation levels for the liquid argon calorimeter (LAr) are expected to be in the order of 300 Krad(Si) total ionizing dose (TID) and a total 1 MeV equivalent neutron fluence of $9.6 \times 10^{12} \text{ cm}^{-2}$.

II. PROTOTYPE CIRCUITS

Three Integrated Circuits (ICs) are being designed to be submitted for fabrication in the 8WL, IBM's SiGe 0.13 μm BiCMOS technology: a SiGe Silicon Tracker readout test chip (SGST), a prototype LAr preamplifier and shaper, and a test structures chip.

The differences between the 8WL and the 8HP technologies are mainly that the 8WL is a cost-performance platform (100 / 200 GHz peak f_T / f_{max} vs. 200 / 285 GHz for 8HP); with much shallower implanted sub-collector versus a thicker epitaxially grown sub-collector in the 8HP technology; a lightly doped substrate ($\sim 40\text{-}80\ \Omega\cdot\text{cm}$ vs. $8\text{-}10\ \Omega\cdot\text{cm}$ for 8HP); and a “shallow” deep trench isolation ($\sim 3\ \mu\text{m}$ vs. $8\ \mu\text{m}$ for 8HP) [10]. A schematic cross-section of the two technologies can be seen in Figure 1.

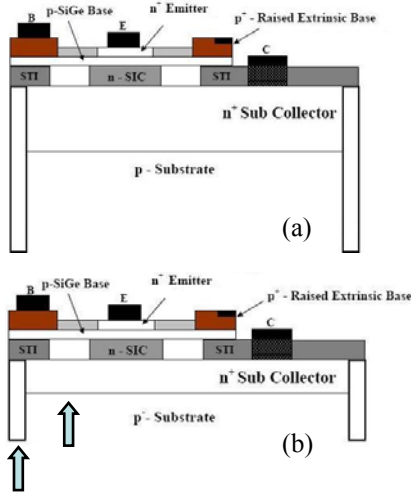


Figure 1 Schematic cross section of the 8HP (a) and the 8WL (b) technologies where the shallower sub-collector and trench isolations can be appreciated [10].

A. Silicon strips tracker prototype

The general circuit schematic of the SGST can be seen in Figure 2. For the SGST the main circuit development goal is to minimize power and meet the SCT noise and 25 ns crossing specs. Threshold and bias adjustment for device matching skew is included in the design, using a different strategy than ABCD or ABCNext ICs, for lowered power rail to 1.2 V. Resistive front transistor feedback is used to reduce shot noise from a feedback current source. The size of this resistor is now optimized for long strips and may need a different optimization for a short strip load. The design allows the shaping time to be adjustable over a $\pm 15\%$ range. Overall, SiGe allows significant current reduction in each analog stage as compared to $0.13\ \mu\text{m}$ CMOS.

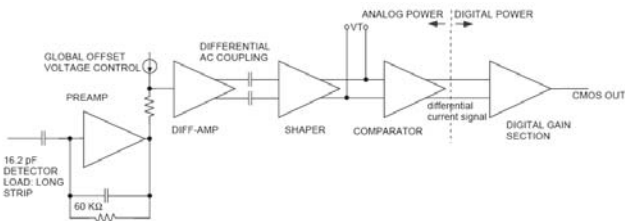


Figure 2 : Circuit schematic of the SGST prototype IC

Two detector loads have been simulated, including strays, one of $5.5\ \text{pF}$ for $V_T = 0.5\ \text{fC}$ and the other of $16\ \text{pF}$ for $V_T = 1\ \text{fC}$. This corresponds to $2.5\ \text{cm}$ and $10\ \text{cm}$ detector strip lengths. Although a final pure CMOS design is needed to quantify the power difference, as a result of the simulations the SGST prototype IC will consume $0.2\ \text{mW}$ per channel for long-strips type load. This sets a comparison point with the CMOS prototypes being developed. Figure 3 shows the simulations results for the equivalent noise charge (ENC) at different circuit biases and for the interesting range of detector loads. The simulations include $600\ \text{nA}$ of detector leakage. In Figure 4 can be seen that the $27\ \text{ns}$ simulated impulse response at comparator for a $5.5\ \text{pF}$ load meets SCT time walk specification of $15\ \text{ns}$ for $1.25\ \text{fC}$ to $10\ \text{fC}$ signal interval. Nevertheless, the chip DAC shaping time adjustment allows tuning of the time walk desired, so that minimal extra power is used to overcome 8WL process variations.

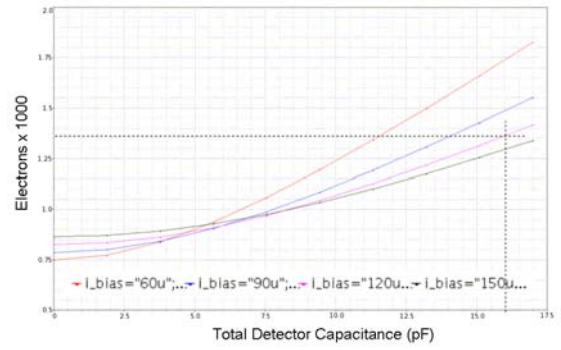


Figure 3 ENC of the long strip readout. ENC=1350 e- @ $16.2\ \text{pF}$ and $120\ \mu\text{A}$ front current, $0.2\ \text{mW/channel}$ power dissipation does not compromise needed noise performance for long strips. Short strip noise at $60\ \mu\text{A}$ is high, and would be helped by much larger feedback resistor than $60\ \text{k}\Omega$.

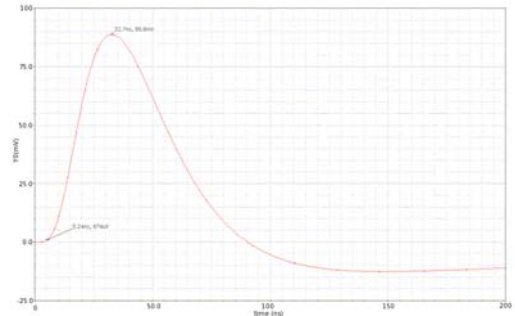


Figure 4 Simulated impulse response at comparator in the SGST circuit for a $5.5\ \text{pF}$ load

B. Liquid Argon Calorimeter Prototype

A block diagram of the LAr front-end readout architecture can be seen in Figure 5 (top) together with a view of the chiplet design (bottom).

The preamplifier is based on the “super common base” architecture as is the one presently installed in the LAr front-end boards (FEB) [11]. Thanks to the SiGe low spreading base resistance it employs an input transistor of manageable size (emitter length $4 \times 20\ \mu\text{m}$, 2 emitter stripe geometry) biased at $8\ \text{mA}$ collector current. The preamplifier achieves an overall equivalent series noise of $0.26\ \text{nV}/\sqrt{\text{Hz}}$, while dissipating $42\ \text{mW}$. In the present prototype the fully

differential shaping stage is divided into two gain ranges, each dissipating about 100 mW. A fully differential gain $\times 10$ low noise stage amplifies the preamplifier signal for the high gain branch to limit second stage noise.

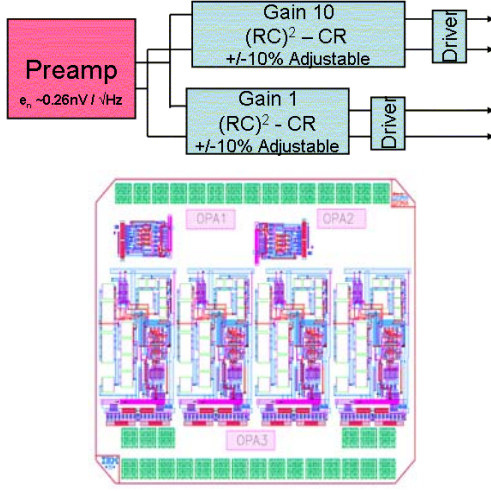


Figure 5 : LAr chiplet 1.8 mm². 2 preamp & shaper channels

As in the present generation the shaper employs a $\text{CR}(\text{RC})^2$ transfer function. Including second stage noise, the front-end readout has an input-referred noise to signal, ratio $\text{ENI}=72$ nA rms, about 28% lower than the current generation.

Figure 6 shows simulation results, for a 0.5 mA to 5 mA range of LAr input current. The linearity is better than 0.2% over the full dynamic range.

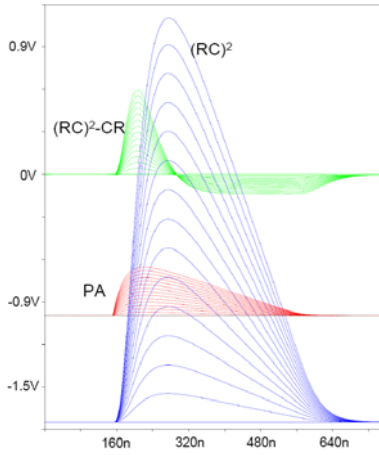


Figure 6 : LAr circuit prototype response for Pre-Amp (PA), and Shaper after integration, $(\text{RC})^2$, and at output $(\text{RC})^2$.

C. Radiation test chip

A third chip will be fabricated containing test structures of the 8WL technology. Standard design-kit devices are introduced, including individual SiGe bipolar transistors, configured in differential pairs, and resistors. The test chip also incorporates a pure CMOS test structure designed by the CERN Micro Electronics Group for the IBM 0.13 μm CMOS 8RF technology that has been ported to the 8WL technology for direct comparison of the CMOS modules of both technologies. A description of the composition of the bipolar section of the test structure can be seen in Table 1.

Table 1 : Composition of the radiation test chip

Device	Dimensions	Quantity (pairs)
SiGe bipolar transistor differential pair	$1 \times 0.12 \mu\text{m}^2$	4
'High Performance' type	$8 \times 0.12 \mu\text{m}^2$	4
SiGe bipolar transistor differential pair	$20 \times 0.12 \mu\text{m}^2 \times 2$ stripes	4
'High Breakdown' type	$1 \times 0.12 \mu\text{m}^2$	2
	$8 \times 0.12 \mu\text{m}^2$	2
	$20 \times 0.12 \mu\text{m}^2 \times 2$ stripes	2
RP type resistor	$2 \text{ k}\Omega$	3

III. RADIATION STUDIES

Two IBM 0.13 μm BiCMOS SiGe technologies, the 8HP and the 8WL, are being evaluated for radiation hardness using “spare” test chips from IBM, until we have the newly designed test chip at our disposal. Gamma irradiations have been performed at the Brookhaven National Laboratory (BNL), USA. Three different total doses have been reached: 10, 25, 50 Mrads(Si). Neutron irradiations have been also performed in the TRIGA Nuclear Reactor, of the Jozef Stefan Institute in Ljubljana, Slovenia and also in the Fast Neutron Irradiation (FNI) Facility in the University of Massachusetts Lowell Research Reactor, USA. The 1 MeV neutron equivalent fluences reached are: 2×10^{14} , 6×10^{14} , 1×10^{15} , and $2 \times 10^{15} \text{ cm}^{-2}$. Gamma irradiations have been performed both with the devices shorted and biased in the forward active region, while for the neutron irradiations the devices had all their terminals shorted together. Cadmium shielding has been used in the neutron irradiations at the nuclear reactor in order to avoid excess damage from thermal neutrons [12].

The effects of both neutron and gamma irradiations on the characteristics of the SiGe bipolar transistors are an increase of the base current (I_B), which produces a reduction in the common emitter current gain ($\beta = I_C / I_B$). This base current increase has a strong dependency on the injection level in the transistor, as a result the performance degradation of the transistors is much more severe at lower collector currents than at higher currents, as can be observed in the example plot in Figure 7.

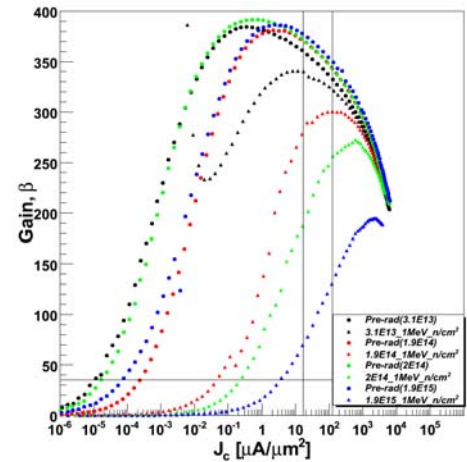


Figure 7 : Pre- and post-irradiation current gain of several 8HP transistors irradiated with neutrons at various fluences.

In order to quantify the radiation hardness of these devices for their application in the ATLAS Upgrade electronics, several figures-of-merit have been chosen: The change in

reciprocal gain, $\Delta(1/\beta) = 1/\beta_F - 1/\beta_0$, is a widely used parameter in the literature of radiation effects on bipolar transistors, but we have also chosen the final post-irradiation gain (β_F) in order for the designers to have a more direct insight on the performance degradation of the transistors within the circuits. These figures-of-merit have been extracted for all the transistors irradiated with neutrons and gammas at a base-emitter voltage of 0.75 V, which corresponds to an injection level close to the actual injection level that these transistors are expected to work in the real circuits.

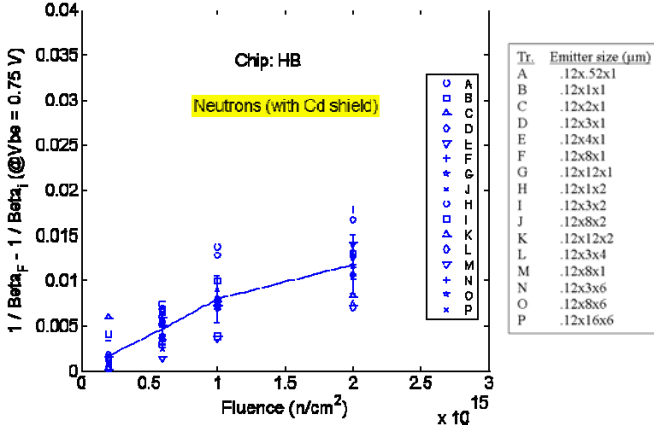


Figure 8 : Reciprocal gain of 8WL “high breakdown” transistors irradiated with neutrons, extracted at $V_{BE} = 0.75$ V.

Figure 8 shows the change in reciprocal gain for the 8WL transistors irradiated with neutrons. As is expected from the literature [13], there is a linear dependency of this parameter with the 1 MeV neutron equivalent fluence, although it seems that the damage starts to saturate at the higher fluence of $2 \times 10^{15} \text{ cm}^{-2}$. The same plot but this time for the gamma irradiated 8HP transistors (Figure 9) shows a linear dependency in the log-log plot, resulting in a dependency of the type $\Delta(1/\beta) = (\text{dose})^a$ where a is a constant, which we have also observed in the past for advanced bipolar transistors [14].

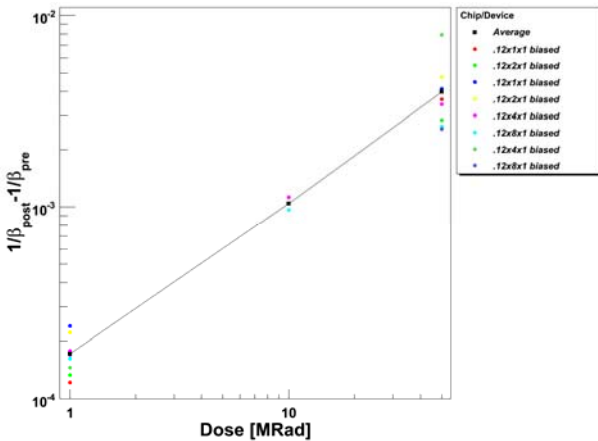


Figure 9 : Reciprocal gain of 8HP transistors irradiated with gammas, extracted at $V_{BE} = 0.75$ V.

For a more direct knowledge of the suitability of these transistors for the ATLAS upgrade electronics, we can see the plots of their final current gain after irradiation. Figure 10 and Figure 11 show this parameter for neutron and gamma

irradiations respectively. It can be seen that all transistors remain well over a minimum acceptable value for the current gain of 50 after irradiation up to our highest target fluence and dose. Some of the transistors irradiated with neutrons at higher fluences do show more marginal performance. Also, some dispersion in the results for the different transistors can be seen. We believe this is due to problems or variability in the test structure. In any case, as we do not really know the actual cause and we have no information about the fabrication conditions of these parts, we want to repeat these measurements with our own test chip made with design-kit transistors, as presented above, and fabricated within process specifications.

IV. CONCLUSION

The electrical characteristics of both IBM 8HP and 8WL SiGe technologies make them good candidates for the front-end readout stage for sensors that present large capacitive loads and where short shaping times are required, such as the upgraded ATLAS silicon strip detector (especially the long strip version) and the liquid argon calorimeter.

Three ICs have been designed to evaluate the suitability and radiation hardness of these technologies and their performance for the mentioned applications. Simulations show that the circuits will meet the requirements and allow considerable power savings to the systems.

The bipolar devices of the two SiGe BiCMOS technologies studied experience performance degradation from ionization and displacement damage. Nevertheless, the level of degradation is manageable for the expected radiation levels of the upgraded ATLAS LAr calorimeter and silicon strip tracker. The dispersion of final gains after irradiation may be a concern that warrants further investigation.

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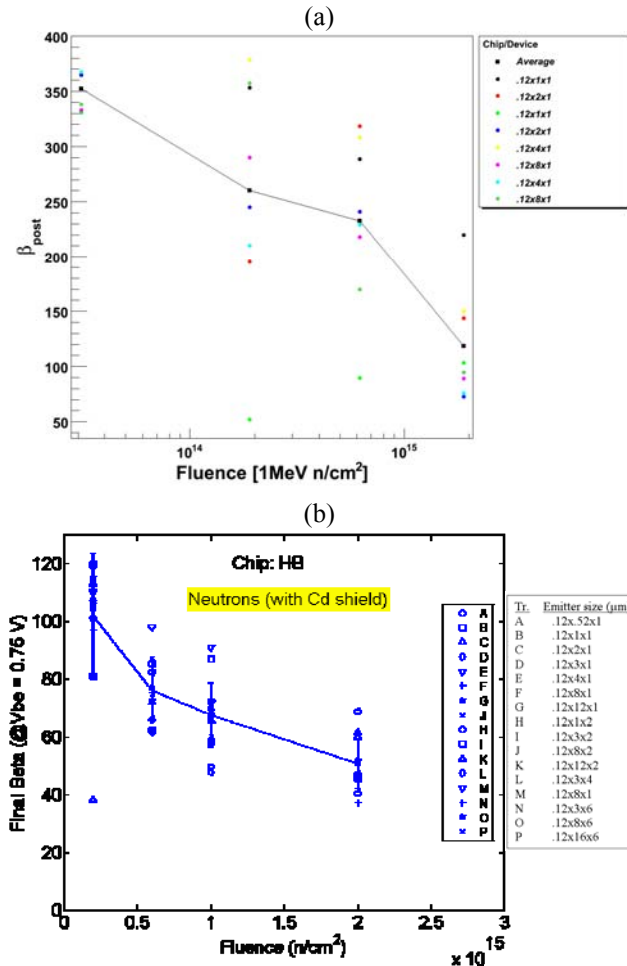


Figure 10: Post-neutron irradiation of 8HP (a) and 8WL (b) transistors at an injection level of $V_{BE} = 0.75$ V.

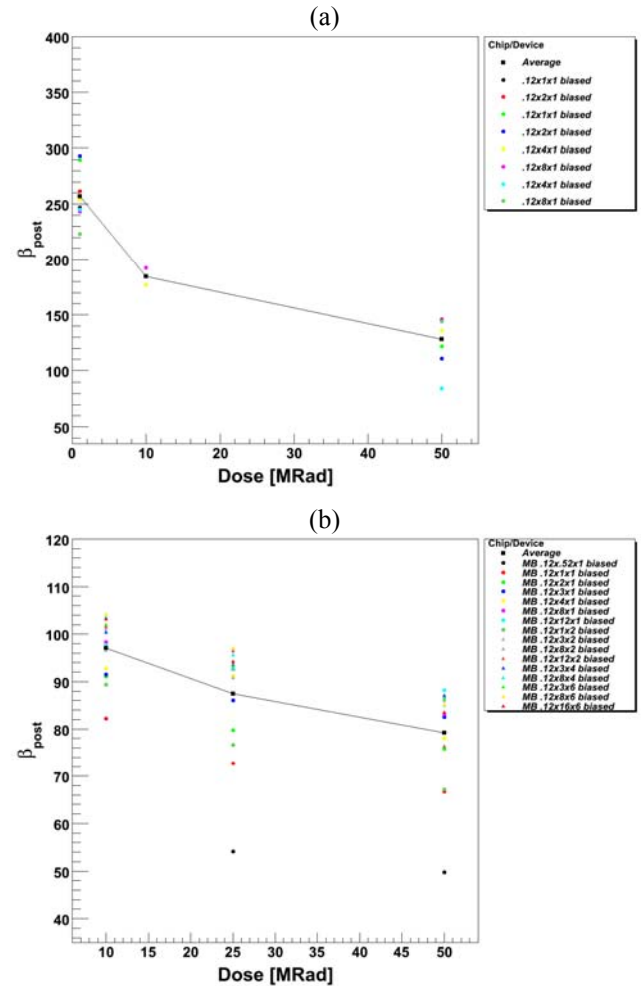


Figure 11: Post-gamma irradiation of 8HP (a) and 8WL (b) transistors at an injection level of $V_{BE} = 0.75$ V.