Design studies of a low power serial data link for a possible upgrade of the CMS pixel detector

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TWEPP 2008

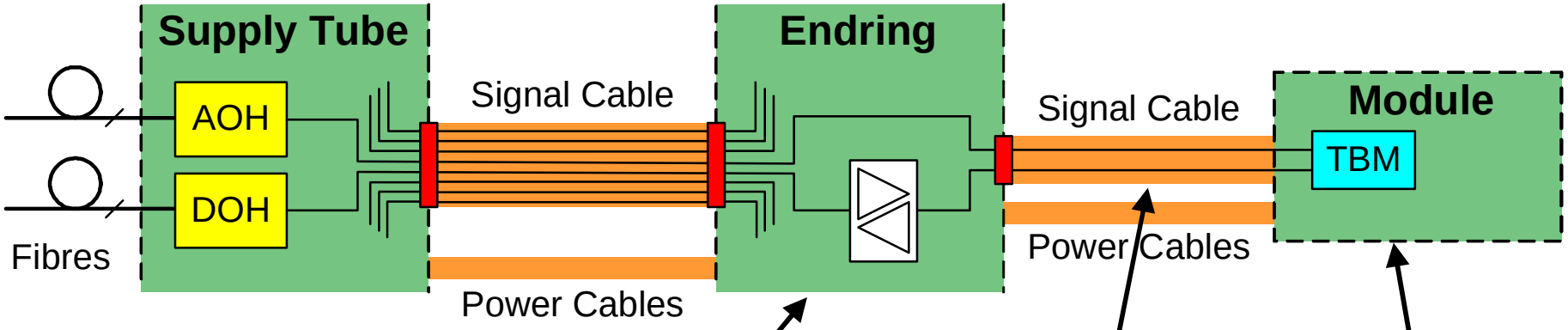
Motivation

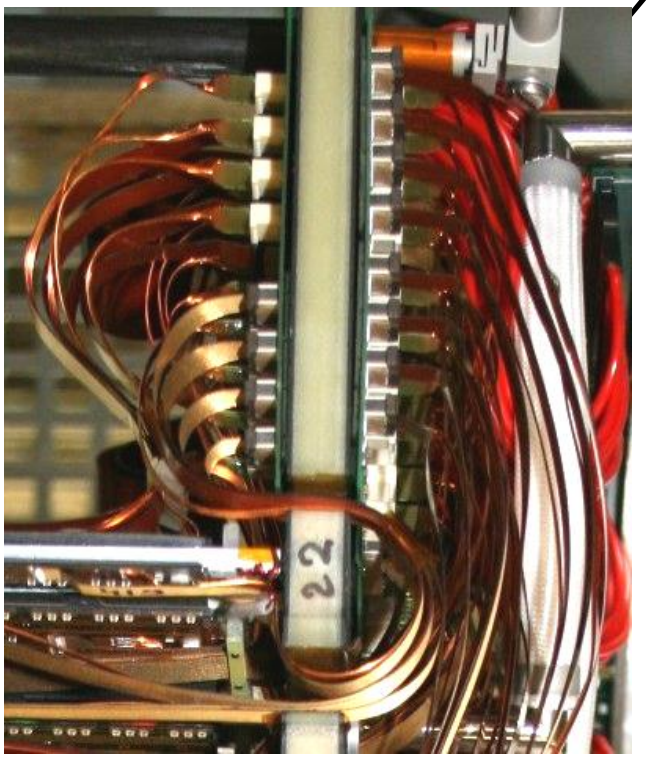
Communication link between detector (pixel module) to outside the tracker volume (BPIX supply tube) with

- minimal material budget → micro twisted pair (unshielded)
- minimal power consumption → low voltage swing → differential
- minimal wiring effort (# cables) → serial data link
- 160 or 320 Mbit/s (4x or 8x LHC clock)
- 1…2 m cable length

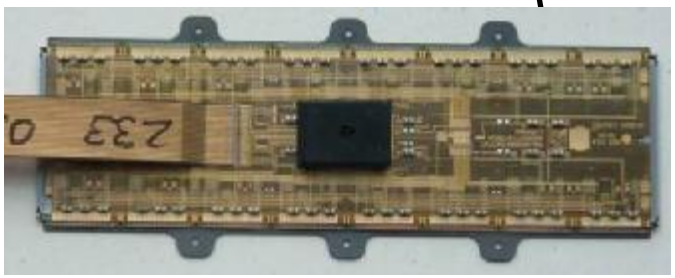
What is possible ?

Existing Data Link in CMS Pixel Detector



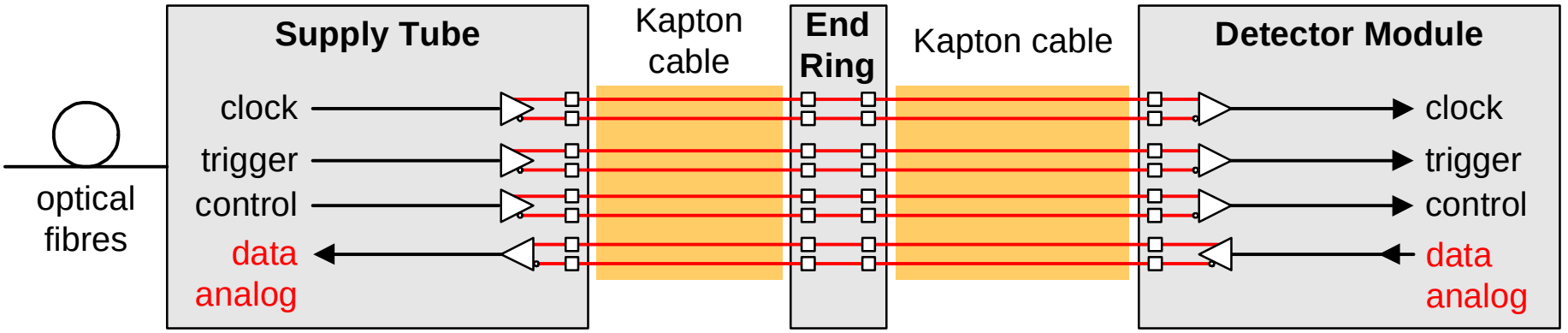


Kapton cable with 21 traces and ground plane

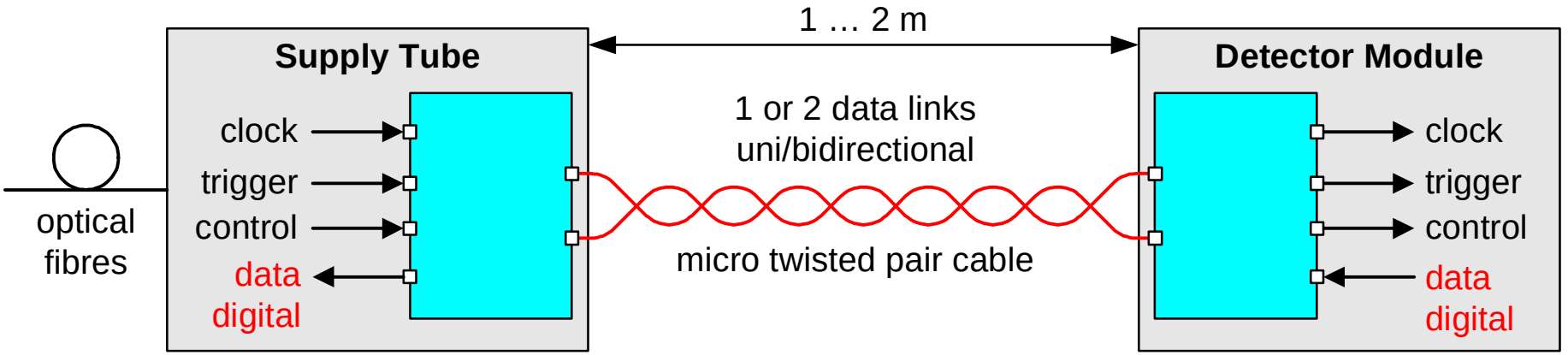


Comparison to a possible new Concept

Existing System in CMS Pixel Detector

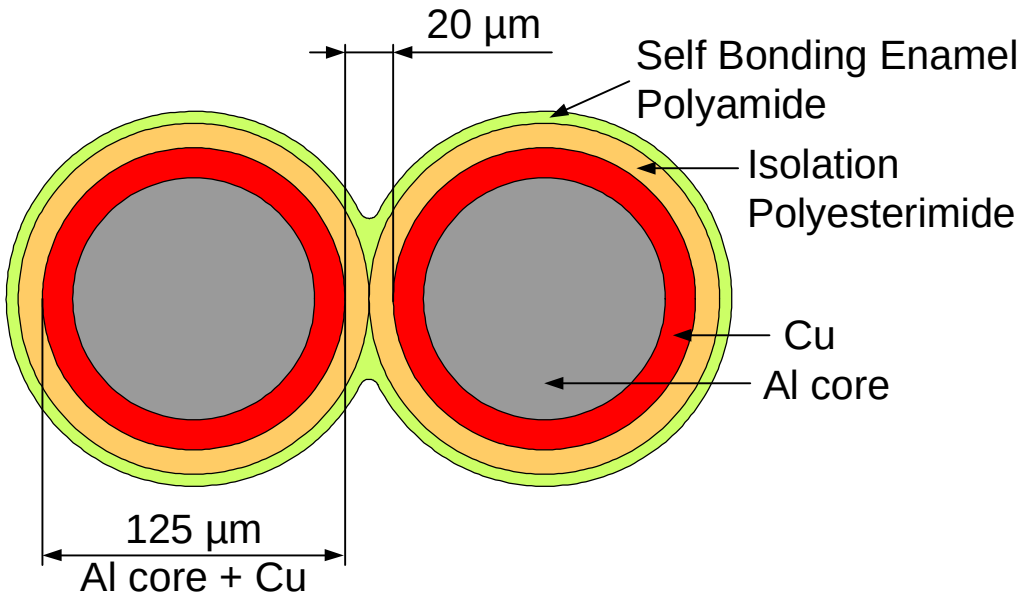


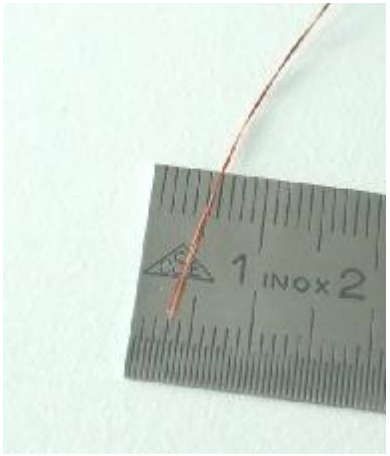
New Concept



Micro Twisted Pair Cable

cross section





First Choice:

- twisted pair self bonding wire
- 125 µm wire diameter (4um Cu)
- 10 mm per turn

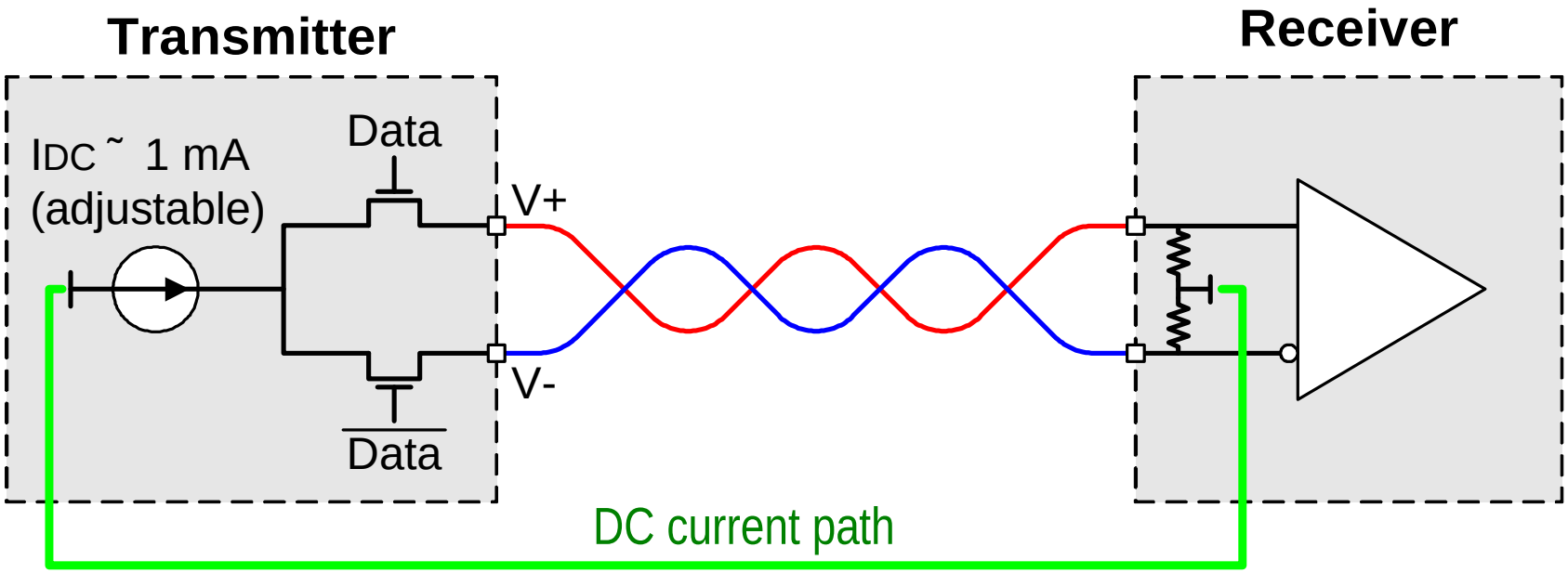
Electrical characteristics:

- Impedance: 50 Ohms (very low for differencial line)
- Impedance change: 1.3 Ohms per 1 µm distance variation
  (Calculation done with ATLC by Sandra Oliveros UPRM)
- $v = 2/3\ c_0$ (5 ns/m)
- C = 100 pF/m, L=250 nH/m

Lossy Transmission Line

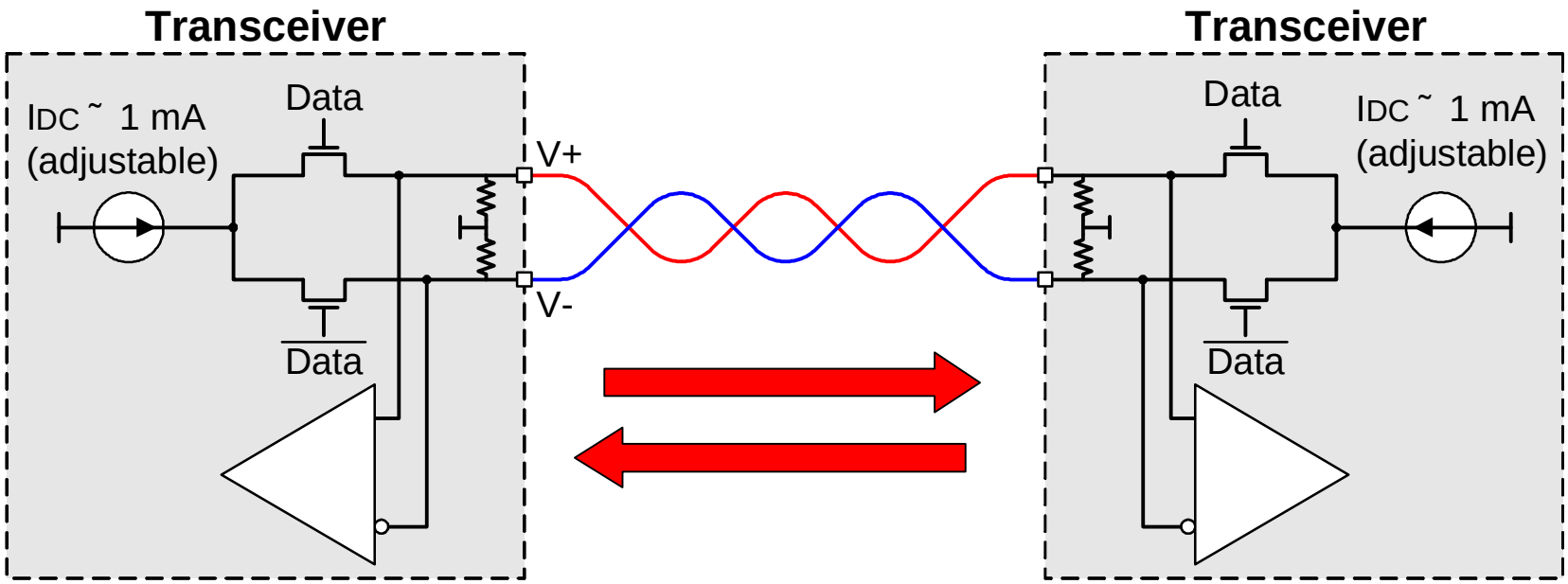
- DC Resistance R_{DC} = 2.3 Ohm / m
- Skin deepth $\delta = \sqrt{\frac{2}{\omega \cdot \mu \cdot \sigma}}$ → 8.5 µm at 100 MHz (wire diameter 125 µm)
- AC Resistance $R(\omega) = \sqrt{R_{DC}^2 + R_{AC}^2(\omega)}$, $R_{AC}(\omega) = \frac{1}{\pi\, d\, \delta\, \sigma}$
  → 8.5 Ohms at 100 MHz
- Proximity effect probably increases R_{AC} by a factor of 3
- Line Impedance $Z_l(\omega) = \sqrt{\frac{j\,\omega\, L + R(\omega)}{j\,\omega\, C}}$
- Propagation coefficient $\lambda(\omega) = \sqrt{j\,\omega\, C\,(j\,\omega\, L + R(\omega))}$
- 50% signal power loss in a 2 m cable

Data Link on electrical Level



- Differential Current Driver (LCDS) from CMS Pixel
- rise time < 400 ps
- DC loop closed over power lines
- output signal adjustable with IDC

Bidirectional Data Link

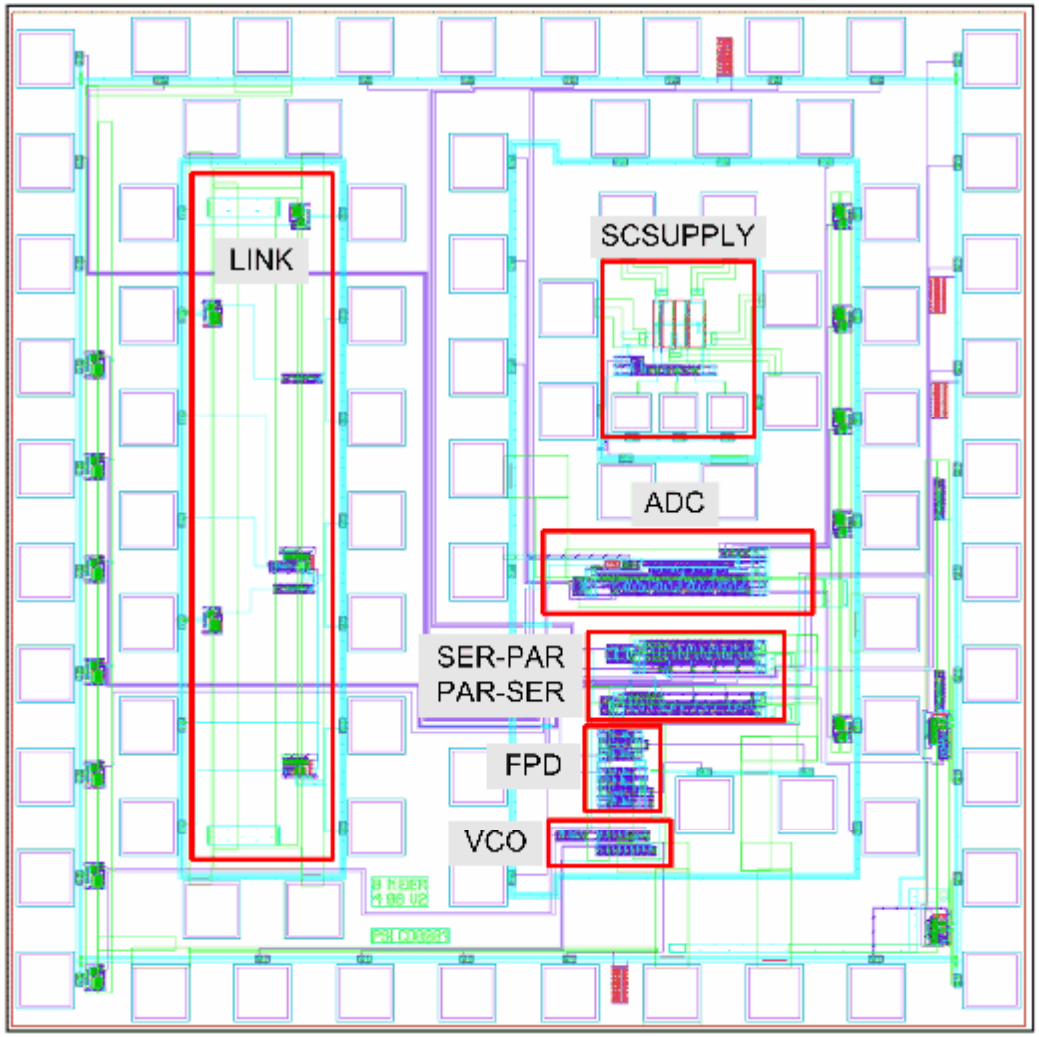


Logic Levels

	V+	V-	diff	sum
L	0	I_{DC}	$-I_{DC}$	I_{DC}
H	I_{DC}	0	$+I_{DC}$	I_{DC}
high Z	$I_{DC}/2$	$I_{DC}/2$	0	I_{DC}

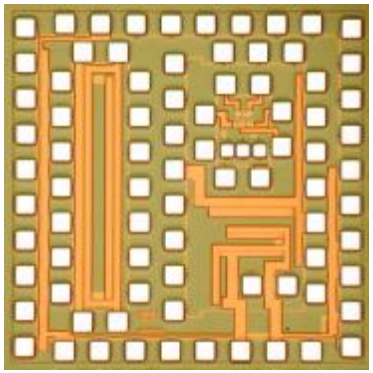
- Driver has a $I_{diff} = 0$ state
- No common mode
- fast switch of data direction

Test Chip Layout

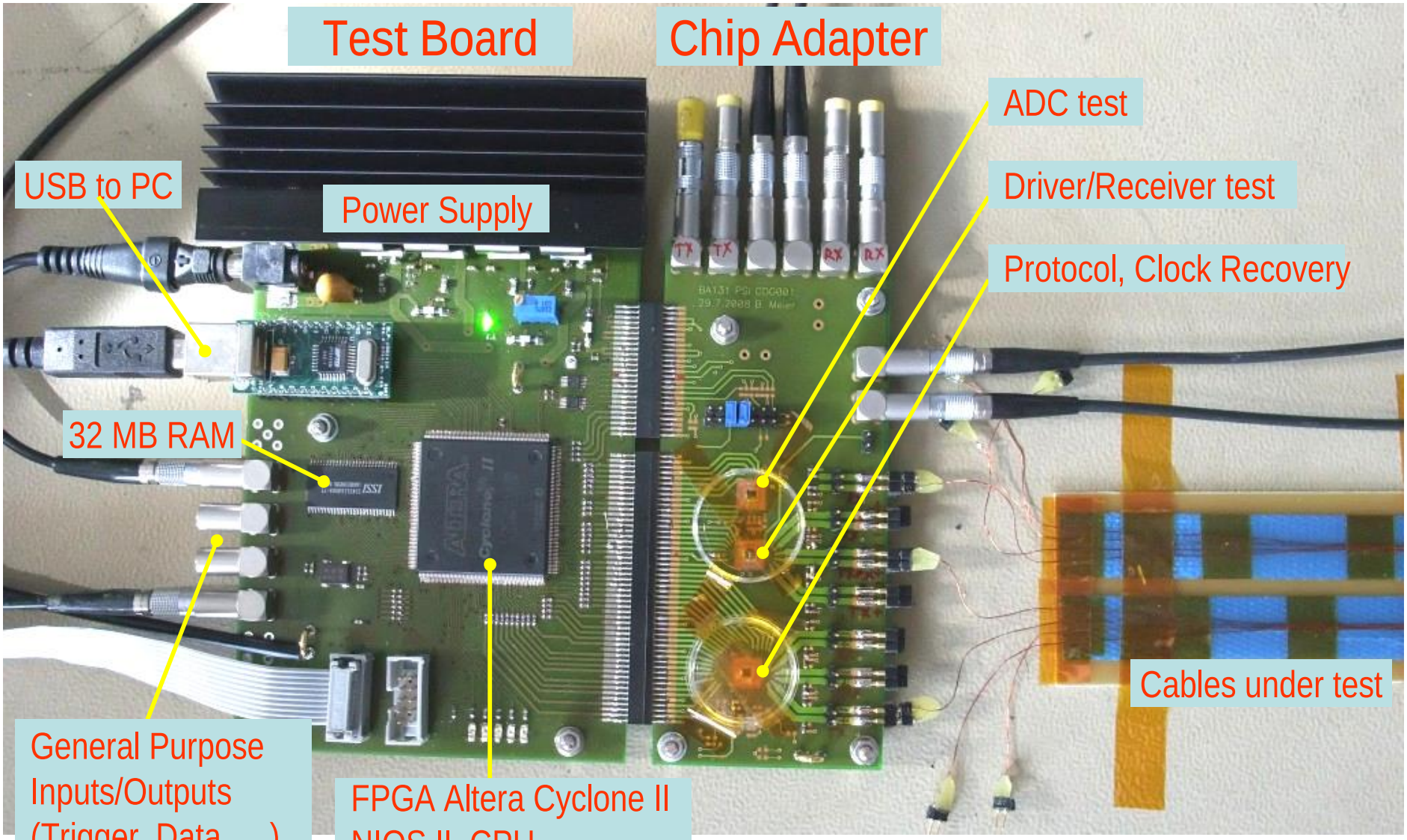


Design of a first test chip
(PSI Chip Design Core Team)

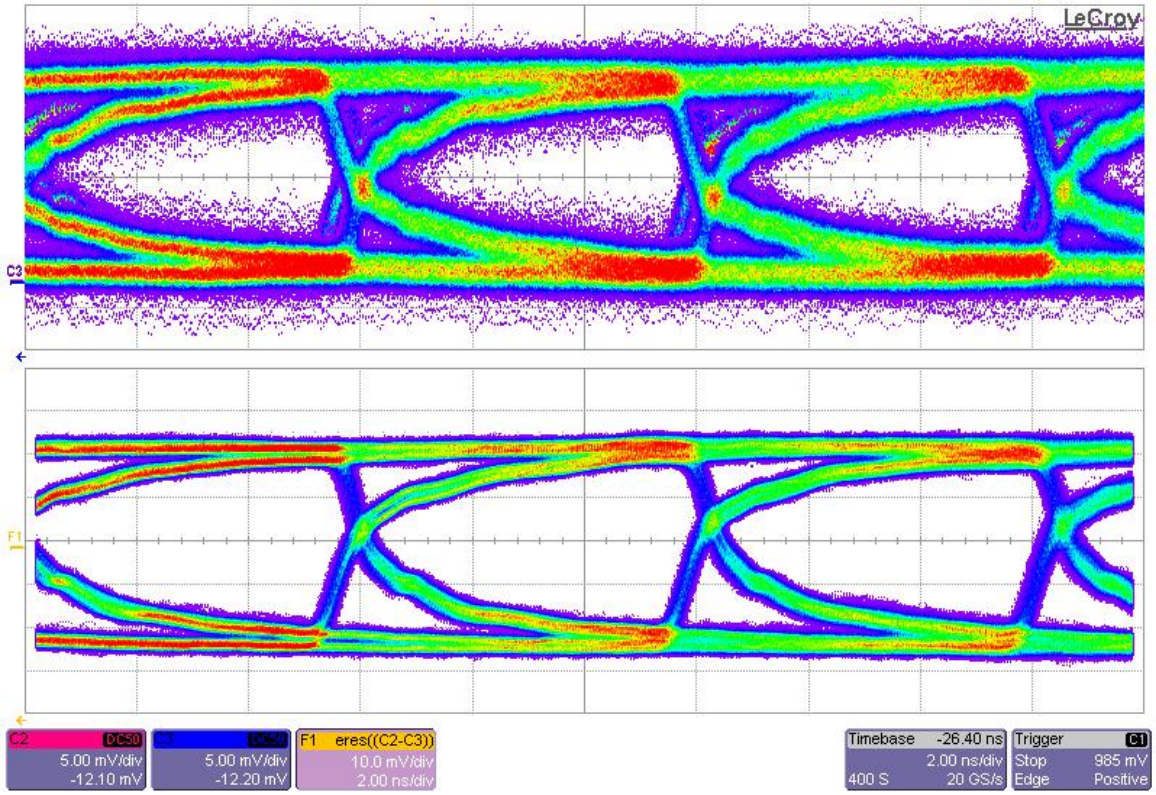
- Size: 2 x 2 mm
- Technology: 250 nm CMOS IBM
  same as CMS Pixel ROC
- radiation hardness design
- CERN MPW submitted in April 2008
- design time was 4 weeks



Chip Test System



Eye Diagram at 160 Mbit/s

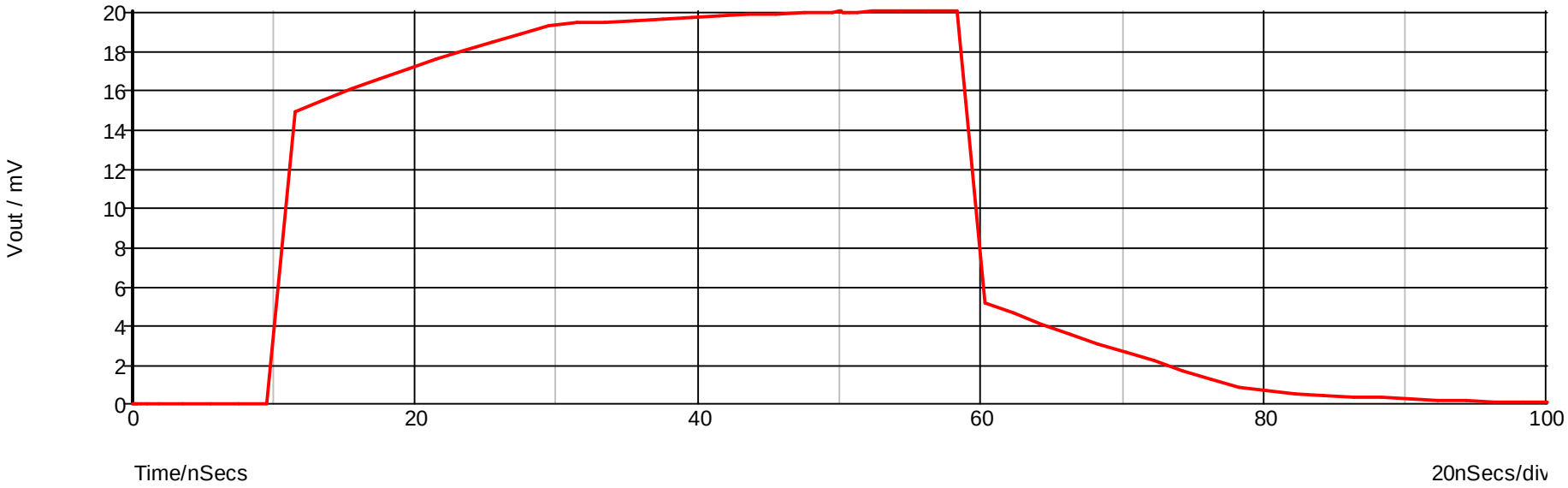


V+ and V-

V_{diff} = 45 mV

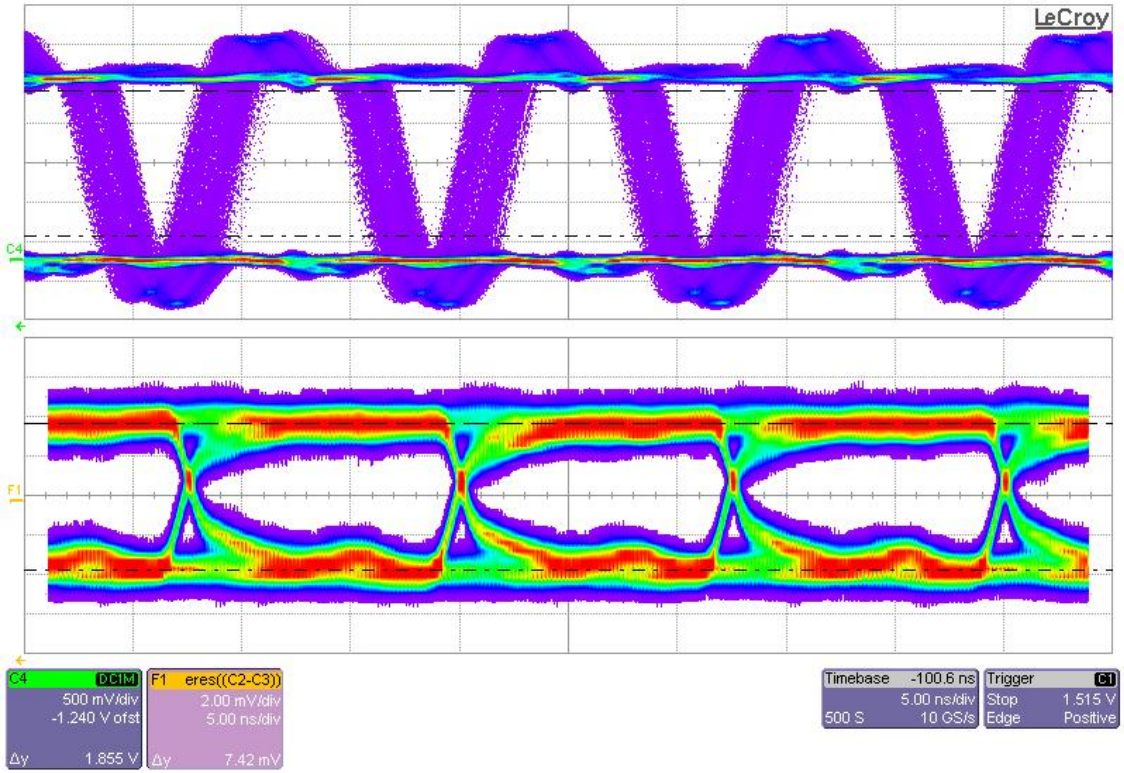
- Line length: 2 m
- Lossy line effects visible (rising and falling edges)
- Line in the RC (low frequency) and LC (high frequency) region

Simulation with Spice



Fast and slow region in rising/falling edge as a result of the lossy line

Bit Error Rate Measurements



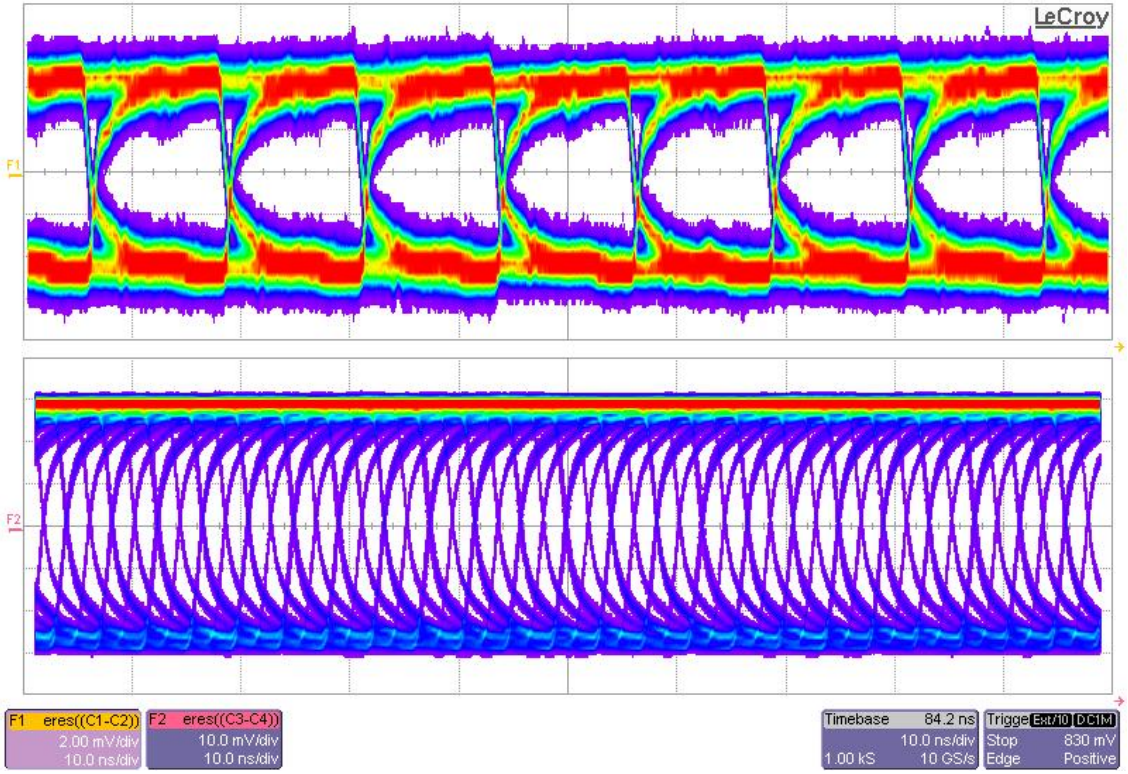
Receiver output signal

V_{diff} = 7.4 mV @ 80 Mbit/s

Scope bandwith limited to 1 GHz

- 80 Mbit/s and 160 Mbit/s
- Bit Error Rate < 10^{-11}
- Receiver design error (time asymmetry) → amplitude at receiver > 35 mV @ 160 MHz

Crosstalk



V_{diff} = 9 mV @ 80 Mbit/s

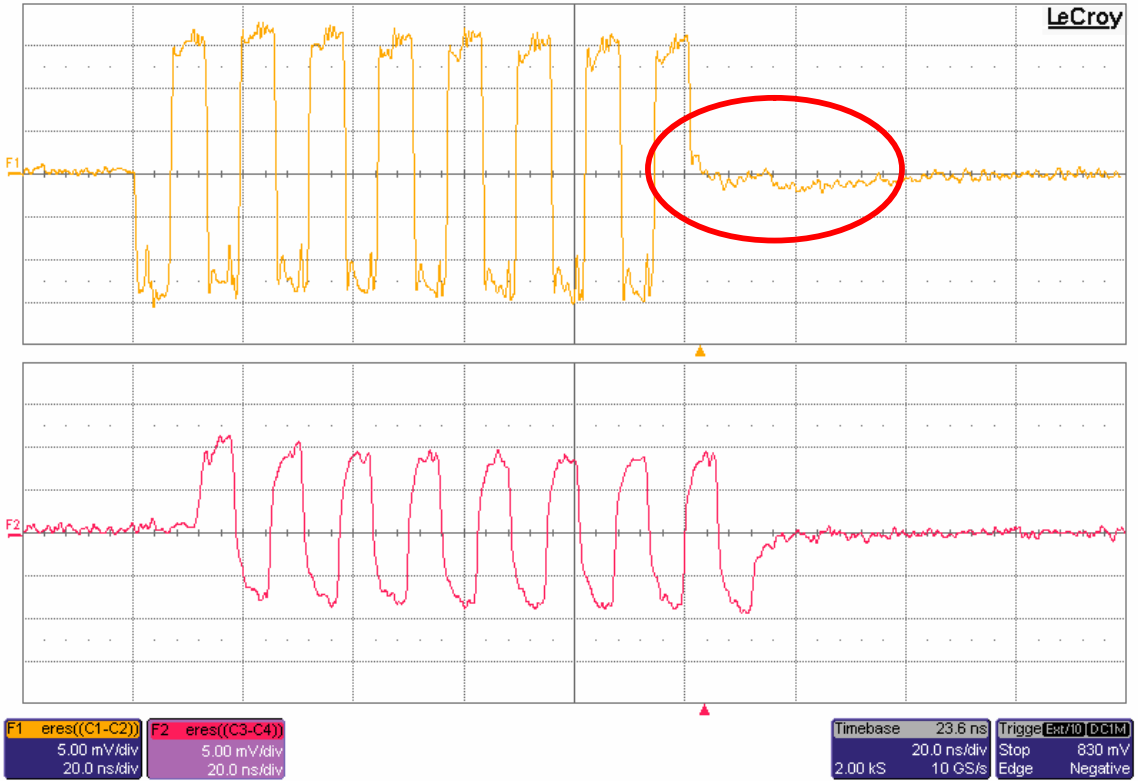
Scope bandwith limited to 1 GHz

parallel line signal (asynchronous)

V_{diff} = 56 mV

- 80 Mbit/s and 160 Mbit/s (with higher level)
- No difference in bit error rate visible with/without disturbing signal
- very robust for crosstalk (twisted cable, high capacitance cable)

Tranceiver switching Time



V_{diff} = 27 mV at transmitter

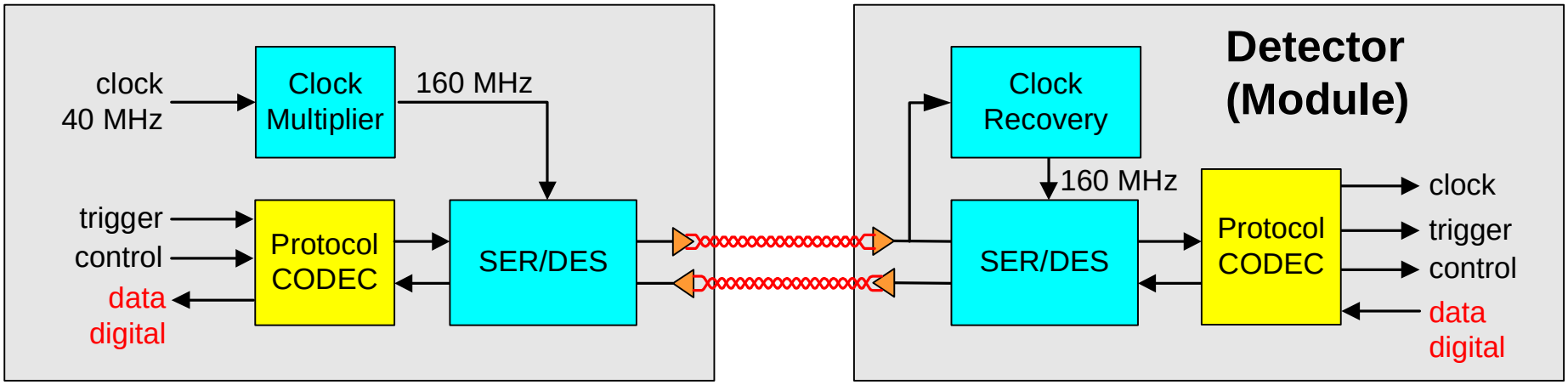
V_{diff} = 18 mV at receiver (line end)

- Data direction switching at 160 Mbit/s
- Line length: 2 m
- minimal delay for line stabilization (less than 1 signal round trip in a 2 m line)

Power Calculations

	new Data Link	CMS Pixel
Supply Voltage	2 V	2 V
Driver Current	0.4 mA (V_{diff}=20 mV_{pp})	2 mA
Receiver Current	0.2 mA	0.2 mA
Total Power per Link	1.2 mW	4.4 mW
Bitrate per Data Link	160 Mbit/s (320 Mbit/s)	100 Mbit/s (2.6*40)
Total electrical Links	2	6 (clock, data, …)
Total Power	2.4 mW (+ PLL)	26 mW
Energy per Bit and Link	7.5 pJ (160 Mbit/s)	

Data protocol



Implemented on the Chip (blue)

- Clock multiplier (PLL)
- Clock recovery (PLL)
- Serializer/Deserializer SER/DES

To implement on the FPGA (yellow)

- Bit coding
- Protocol

Conclusions, Outlook

- Less than 10 pJ per bit per link over 2 m
- 160 Mbit/s is ok
- No crosstalk problems, it is possible to bundle the unshielded cable

- Tests with 320 Mbit/s (probably over a distance < 2 m)
- Tests with other wires
- Tests with different data protocols
- Clock recovery