

# Design Studies of a Low Power Serial Data Link for a possible Upgrade of the CMS Pixel Detector

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## Abstract

The material budget inside the sensitive tracking volume is highly dependent on the dissipated power for data transmission. It is therefore important to have a very low power serial data link, which allows transmission of digital data over short distances within the tracking volume. This low power ohmic data transmission through micro-twisted transmission lines aims for a transmission speed of 160/320 MHz and allows concentration of the tracker data to multi gigabit optical data hubs. For such a future link we need low swing differential drivers and receivers with PLLs for frequency multipliers and clock recovery. We have implemented in radiation hard layout all the necessary components on a recently submitted 250nm CMOS test chip. After reporting on the experience gained with low power data transmission in the current CMS pixel detector, we present the design considerations and first results for this new 160/320 MHz serial link that may work with differential signal levels as low as 10mV.

## I. INTRODUCTION

The communication from the detector modules to outside the tracking volume needs special data link configurations. It is not possible to take a few (optical) high speed data links because the information should be collected from many different similar detector components at different locations. For the case of the CMS pixel detector, the distances of 1 to 2 meters are relatively short. We need many data links of some 100 MBit/s. Due to the material budget and power constraints, it is not reasonable to do this with optical links. Copper wires are preferred. For the cabling, we have to optimize the following properties:

- To minimize the material budget, we take thin twisted pair wires without a shield.
- To minimize the power consumption we should have a low voltage swing. This needs differential signals.
- To minimize the wiring effort we need a serial data link at a multiple of the 40 MHz clock frequency. We need 160 or better 320 Mbit/s if it is possible.

We need to know what works if we go to thin wires, low signals, and higher speed at the same time. A possible approach will be shown for an upgrade for the CMS pixel detector.

## II. THE CMS PIXEL DETECTOR

### A. Signal Cabling

The CMS pixel detector consists of 768 modules on a support structure where the cooling pipes are also integrated. All the power and signal cables from the modules are routed to flanges at the two ends of the detector structure (Figure 1). There, the cables are connected to 64 PCBs. The signal cables are flat band cable with 21 traces.

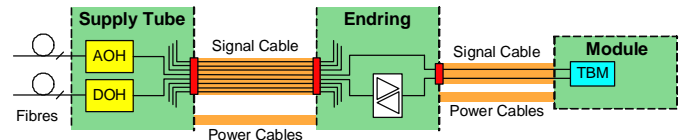


Figure 1: Signal and power connections from the modules.

From each of these PCBs, we have two wide flat band cables to the supply tube as shown in Figure 2. From there we have optical links. There are a total of 1664 connectors for power and signals on both flanges.

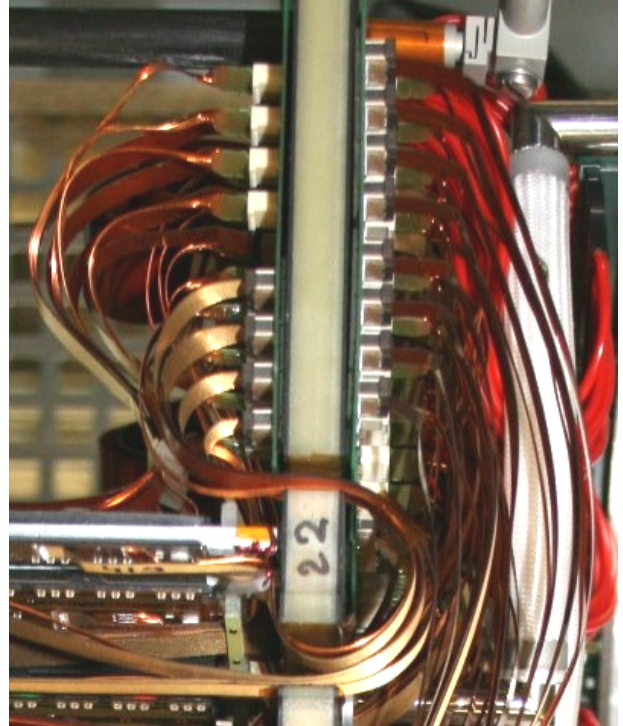


Figure 2: Cabling at one of the ending PCBs. The module cable comes from the bottom left and is connected to a PCB on each side of the flange.

### B. A possible new Concept

Figure 3 shows a schematic view of the signal path. From the supply tube we have clock, trigger, and control data. The signals are sent over a flat band cable to one of the 64 ending PCB's. From there, we go to one of the 768 modules. From the module, we have control and detector data which are sent through separate lines over the same path.

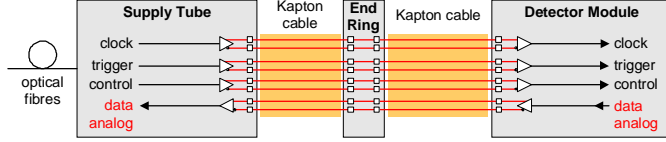


Figure 3: Existing Concept

As shown in Figure 4, for the new concept we would completely remove the PCB's on the endflange with all the connectors. We would replace the flat band cables with one or two micro twisted pair cables which go directly from the module to the supply tube. At each endpoint is a controller for the serial protocol and the cable drivers and receivers. This logic can be integrated in existing chips.

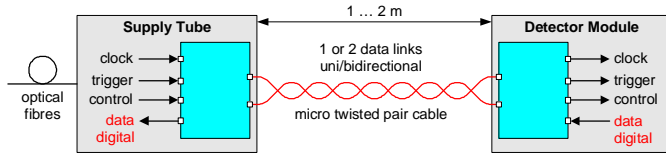


Figure 4: Possible new Concept

The data format for the existing link is a 7 level signal and analog level for the pulse height information. The new link is fully digital. No analog pulse height signals can be transmitted. For this reason we have to add an ADC to digitize the pulse height signals.

## III. MICRO TWISTED PAIR CABLE

### A. Choice of a Cable

A first choice for a cable we have tested is a micro twisted pair cable. It consists of two copper clad aluminium (CCA) selfbonding wires as shown in Figure 5 from Elektrisola (<http://www.elektrisola.ch>).

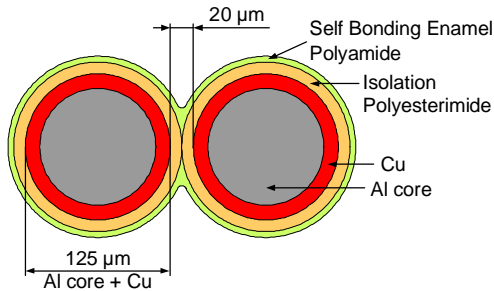


Figure 5: Cable Cross Section

This seems to be a good compromise between electrical resistance and breaking strength. Such a wire is easier to handle because you can bend it in each direction compared with the flat band cable that you can only bend in one direction.

One or two of these cables are bundled together with the power cables to build a module cable.

### B. Electrical Characteristics

We have calculated the impedance with the software ATLCL [1]. The resulting differential impedance is  $48 \pm 2 \Omega/\text{m}$ . The impedance decreases with increasing wire distance with  $2.3 \Omega/\text{m}$  per  $\mu\text{m}$ . We have verified the impedance calculation by a measurement with the cable. The measurement signal velocity is  $2/3 c$ . The impedance is very low because of the thin isolation and the consequential small distance between the wires. The return path consists of the power and ground wires. Because the geometry of this wire is not defined, the common mode impedance is not well defined. The calculated capacitance is  $C=100\text{pF}/\text{m}$  and  $L=250\text{nH}/\text{m}$ .

Thin wires also mean that we have a high series resistance and resultant loss. The DC-resistance of this cable is  $R_{DC} = 2.3 \Omega/\text{m}$ . We have also taken into account the skin effect. The skin depth is [2]

$$\delta = \sqrt{\frac{2}{\omega \cdot \mu \cdot \sigma_{Cu}}}$$

where  $\omega$  is the frequency and  $\sigma$  is the conductivity. For our wire,  $\delta = 8.5 \mu\text{m}$  @ 100 MHz. The resistance due to the skin effect is

$$R_{AC}(\omega) = \frac{1}{2 \pi d \delta}$$

where  $d$  is the wire diameter. This is an approximation for  $\delta \ll d/2$ . A good approximation [2] for the total frequency dependent resistance is

$$R(\omega) = \sqrt{R_{DC}^2 + R_{AC}^2(\omega)}$$

We get  $8.8 \Omega/\text{m}$  @ 100 MHz for this. Possibly the resistance can be increased by the proximity effect.

From the telegrapher equation we get the complex line impedance of a lossy line

$$Z_l(\omega) = \sqrt{\frac{j \omega L + R(\omega)}{j \omega C}}$$

and the propagation coefficient

$$\lambda(\omega) = \sqrt{j \omega C (j \omega L + R(\omega))}$$

Here,  $L$  is the inductance per meter and  $C$  the capacitance per meter. The real part of  $\lambda$  is the damping factor in Neper. From our calculations and measurements we get a power loss of about 50% for a wire of 2 m length.

## IV. ELECTRICAL TRANSMITTER AND RECEIVER

### A. Transmitter/Receiver

Figure 6 shows a unidirectional data link consisting of a transmitter, a receiver and the twisted pair cable. Typically at the receiver end is a differential termination of  $24 \Omega$  to ground at each end of the differential pairs. This type of data link is used in the existing CMS pixel detector to send clock, trigger and control signals to the module.

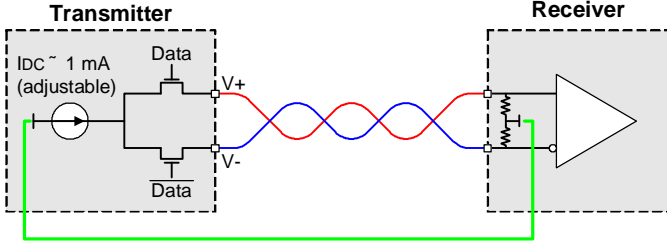


Figure 6: A single unidirectional data link with transmitter and receiver

The transmitter is a current driver. The current  $I_{DC}$  from the constant current source is switched to one of the outputs  $V+$  or  $V-$ . In this way the common mode current has the constant value of  $I_{DC}$ . This is important because there is no well defined common mode impedance. The DC path between transmitter and receiver is closed by the power/ground lines. To test at different signal levels, the current  $I_{DC}$  is adjustable in the first test version.

The differential receiver has high impedance inputs. For the measurements, the termination resistors are not implemented on the chip and must be placed outside on the test board.

### B. Bidirectional Transmission

We combine two driver and receiver pairs into a transceiver as shown in Figure 7. Here, we get a bidirectional link (half-duplex) with one physical line. At any time one driver is in a so called high impedance state. In order to let the common mode current stay constant, the current in this state is  $I_{DC}/2$  on each output so that the sum is exactly  $I_{DC}$ . Typically, this link has a termination on both sides. The data direction is given by the protocol.

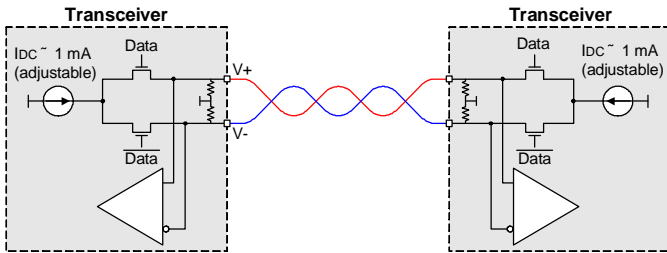


Figure 7: Bidirectional Link

## V. TEST SETUP

### A. ASIC Design

To make the following measurements, I have designed a test chip as a member of the newly founded Chip Design Core Team at PSI with a size of 2 by 2 mm with the following test structures:

- Driver, receiver and transceiver as described above. The  $I_{DC}$  of the driver/transceiver is adjustable from 0 to 2 mA (LINK).
- A four bit serializer and deserializer shift register connected to the transmitter, receiver, and transceiver.
- Two types of voltage controlled oscillators (VCO), and two types of frequency phase detectors (FPD). With these

blocks we can build a PLL for the clock multiplier from 40 MHz to 160 or 320 MHz which also can be used for clock recovery.

- A 4 bit SAR ADC to digitize the analog data signals. For the real data we need 8 bits but this block is for a low priority design study.
- A switched capacitor voltage divider for the analog voltage power supply. This block is not discussed here.

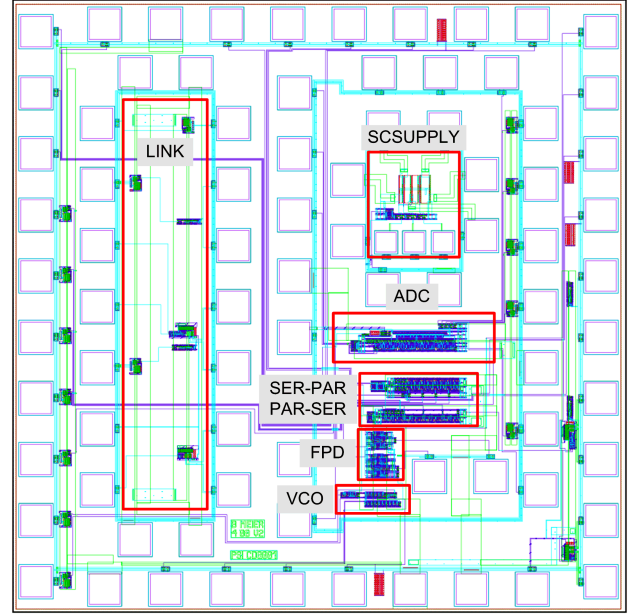


Figure 8: Layout of the 2 by 2 mm chip with the different Components. It consists of four different test structures. The most space is used for the pads.

The Chip, whose layout is shown in Figure 8, is fabricated in a 0.25  $\mu\text{m}$  technology from IBM the same as the CMS readout chip.

### B. Test System

To make the measurements, we have built a test system consisting of a chip adapter and a test board (see Figure 9). The main component of this board is a Cyclone II FPGA from Altera. To control the board by a PC, there is a NIOS II soft core CPU in the FPGA and an USB adapter.

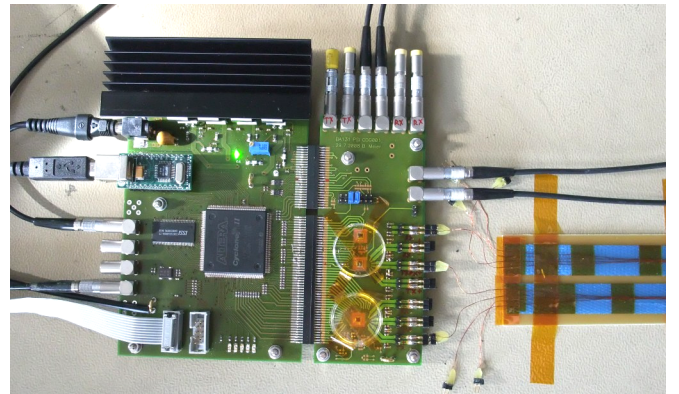


Figure 9: Test system consisting of the Test board (left) and the chip adapter (middle). On the right side are bundles of cables which can be connected to different drivers or receivers



## VI. DATA LINK TESTS

### A. Lossy Line Effects

Figure 10 shows a signal at the end of a 2 m data link at 160 Mbit/s. A typical effect of line loss is seen at the signal edges. This consists of a fast and a slow component. For low frequency, we see an RC-line and for high frequency, it is an LC-line. This can also be shown with a spice simulation with a simple lossy line model.

The single ended signals at V+ and V- on the top of Figure 10 show common mode noise. Most of this comes from digital signal noise from the testboard, but it is highly suppressed in the differential signal.

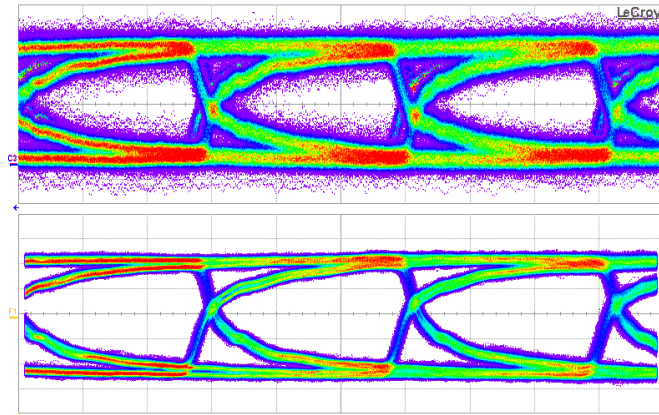


Figure 10: Eye Diagram of a 160 Mbit/s signal at the end of the micro twisted line of 2 m. The upper scope picture shows the signal at the V+ and V- nodes and the picture below shows the differential signal. The Amplitude is 45 mVpp The scale is 2 ns/div horizontally and 10 mV/dif vertically

### B. Bit Error Rate Measurements

To find a lower limit for the signal amplitude we made a bit error rate test (BERT) for a unidirectional link (Figure 11). At 80 Mbit/s, the bit error rate was below  $10^{-11}$ . Because of a design error in the receiver output, it is not able to go below 30 mV at 160 Mbit/s. At this rate we get the same limit in the bit error rate.

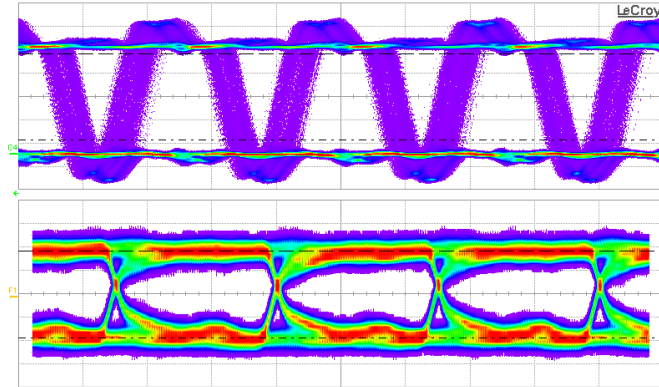


Figure 11: Differential signal at very low amplitude at the receiver input (bottom). The signal amplitude is only 7.4 mV. The signal on the top shows the receiver output. The different propagation delays of the rising and the falling edges are due to a design error.

### C. Crosstalk Measurements

Another important measurement is the crosstalk between parallel lines. The problem is that we have no shield and want to bundle the cable. For the measurement we repeated a BERT but sent a differential signal with a six times higher amplitude as an aggressor to a parallel line over a length of 2m. We could not see any difference in BER with and without the disturbing signal as shown in Figure 12. A reason for that can be the high capacitance of the cable. Field simulations have shown that the energy flows mainly in the small gap of the wire pair.

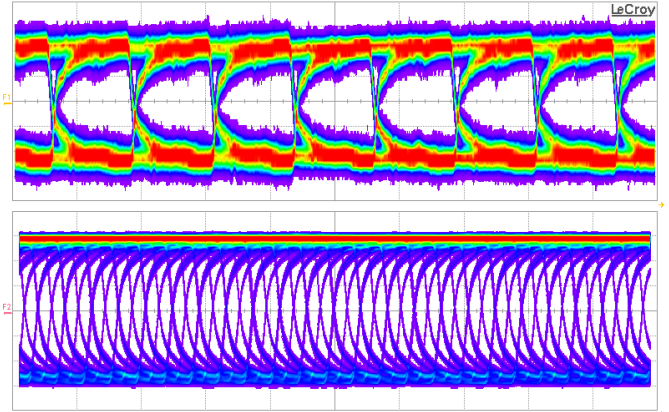


Figure 12: Signals of the crosstalk measurements. On top is the tested data link at a differential signal level of 9 mV. On bottom is the more or less asynchronous signal on a parallel line.

### D. Bidirectional Link

Important for the bidirectional link is the dead time after switching the direction, especially if we plan to work with small packets. For this test I have sent a data packet (Figure 13) and then switched the transmitter into a high impedance state.

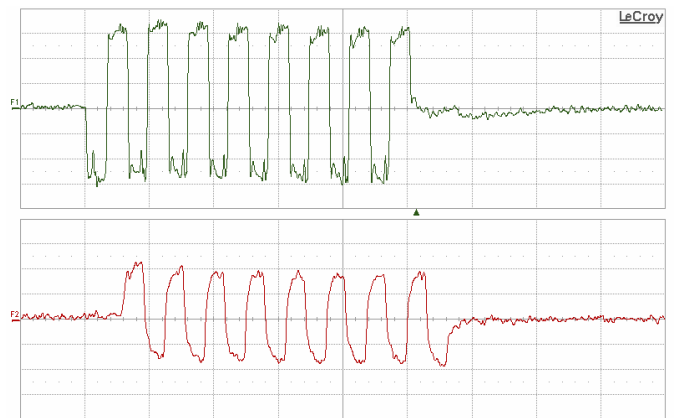


Figure 13: Signal of a short packet sent at 160 Mbit/s by a transceiver at sender side (top) and receiver side (bottom). Before and after the packet, the driver is in a high impedance state. The time scale is 10 ns/div

The signal on the line is stable before two signal line delays. This is the earliest time when the data arrives from the transmitter on the other side.

### E. Power Budget

If we assume that we can run with a signal level of  $V_{diff} = 20$  mV then we need a total driver current of 0.4 mA. The receiver has a current consumption of 0.2 mA. If we assume a supply voltage of 2 V we get a total power of a link of 1.2 mW. The energy per bit at 160 Mbit/s is then 7.5 pJ/bit.

The power for the data transfer to and from a module in the existing CMS pixel detector is approximately 30 mW at 2V. With the new concept we were able to replace the old link with a bidirectional link for one or two lines with a total power of 2.4 mW. In this calculation the power consumption of the PLL is not included.

## VII. DATA PROTOCOL

### A. Overview of a possible System

On the test chip, all front end components to build a complete communication link are available except the protocol implementation. We are able to implement this in the FPGA on the testboard. It is a full digital design that we can later transfer to an ASIC. Figure 14 shows such a system. The left side is the master on the supply tube at the interface to the optical links. The two wires could also be replaced by a single bidirectional wire. The problem with this configuration is that most data are sent back from the module. During the data transfer it is not possible to synchronize the clock for the detector. To increase the amount of data, it is also possible to run with two bidirectional wires or more than two wires.

The LHC clock is multiplied by 4 or 8 to generate the 160 or 320 MHz serial data clock. The Protocol logic combines the incoming trigger and control signals in packets and vice versa for the data signals. The protocol logic runs at 40 MHz and sends and receives 4 bit (at 160MHz) or 8 bit (at 320MHz) from/to the SER-DES.

On the module side is a clock recovery PLL to regenerate the 160 or 320 MHz clock from the data signal. The protocol controller works similar to the other one but in the other direction.

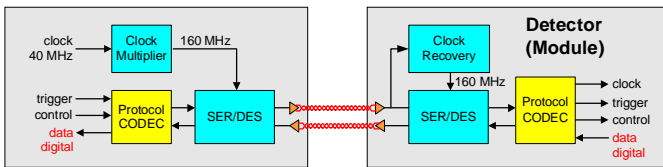


Figure 14: Overview of a possible communication link configuration between the supply tube to a detector module

## VIII. CONCLUSIONS

The measurements show that we can build a communication link with less than 10 pJ per bit. 160 Mbit/s is possible with these micro twisted pair cables. 320 Mbit/s should still be tested. Crosstalk is not a problem if we bundle the cables.

## IX. ACKNOWLEDGEMENTS

THE FOLLOWING STUDENTS WHO WERE SUPPORTED BY AN NSF PIRE GRANT HELPED WITH THIS PROJECT: TONY KELLY (UNL), DAVID MIGAS AND NICK SPIZZIRRI (UIC), SANDRA OLIVEROS (UPRM), AND IRAKLI CHAKABERIA (KSU).

## X. REFERENCES

- [1] ATLC – the *Arbitrary Transmission Line Calculator*, a free software <http://atlc.sourceforge.net>
- [2] *High-Speed Signal Propagation*, H. Johnson and M. Graham, Prentice Hall