TWEPP-08 Topical Workshop on Electronics for Particle Physics

Contribution ID: **106** Type: **Oral**

The SPI as an integrated power management device for serial powering

Wednesday 17 September 2008 16:15 (25 minutes)

For future hep experiments, especially for LHC upgrades new powering schemes are required. The SPI001 (Serial Powering Interface) chip has been designed and fabricated to explore the serial powering approach. Main features of the chip are a programmable shunt regulator (handling at least 1A) and two linear regulators providing module voltages, current mode ADCs monitoring shunt and linear regulator current, overpower protection and AC coupled communication interfaces. Bump bonding techniques are used for chip on board assembly to enhance connectivity and thermal issues.
The concept and design details of the chip are presented and first results are shown.

Summary

It is widely accepted that due to material budget and power dissipation issues LHC upgrade experiments cannot be operated in a standard parallel powered mode. More efficient powering schemes are needed and serial powering, where a current is used to power modules in series, is one very promising alternative proposal. Various approaches are presently discussed where error amplifier and regulator transistor are implemented either internally (meaning as part of ROC), externally or by mixing both scenarios. First studies have already proven the basic principle and modules have been successfully operated serial powered using commercial components.
However, these setups cannot satisfy all needs and an increase urge for an integrated solution using radiation tolerance CMOS technology existed. The SPI chip, fabricated using TSMC 025MM process, addresses this need. It is versatile allowing exploration and evaluation of different SP schemes.
The chip offers a programmable shunt element to provide a module voltage between 1.5 to >2.5V out of the supply current. The shunt is designed to sustain currents of at least 1A at full voltage, higher currents have to be verified in field tests. Simulations show that a dynamic impedance of the shunt element in the order of 100mOhm can be achieved which would exceed the performance of discrete setups by more than two orders of magnitude.
A separate error amplifier on the chip can be used to operate a set of external shunt transistors (distributed shunt concept). These shunt transistors can preferably be integrated in the readout chips on the module (as planned for the ABCn). Compared to a conventional shunt-per-chip approach this concept reduces dispersive effects significantly.
In addition, two independent linear regulators offer separate supply voltages covering a range of ˜1.2 to 2.5V. An idle feature is implemented as a first step towards pulsed powered schemes as anticipated for the ILC machine.
Furthermore the SPI chip provides a bank of 7 AC-LVDS comports. AC coupling is needed as the DAQ system and the module are at different DC potential.
6bit flash ADCs using current mirror techniques are implemented to probe the shunt and linear regulator currents. The LSB of the ADCs is adjustable so that the full dynamic range of the regulators or a smaller range with increased accuracy can be probed.
A programmable threshold can be set to trigger an over-current alarm which can be used to power the chip down. In this case the chip functionality is reduced to a mere switch in order to bypass the current to other modules in the power queue and maintain their operation. Such power down techniques are essential in worst case scenarios where major module components fail.
Each SPI chip can be addressed individually using a 5bit chip ID and is using a common bus in a multi drop configuration. By doing this up to 30 chips can be controlled using only 3 control lines.
To minimize any connection impedance and to provide the most reliable connection solder bump bonding of the chip is anticipated and in-house assembly is investigated.
The design and the features of the SPI chip are presented in detail and first results are shown.

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Session Classification: Parallel Session B5 - Power