Development of the readout ASICs for the NA62 Pixel Gigatracker

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We present the ASIC development of the readout electronics of the Gigatracker pixel detector of NA62. Gigatracker speed, noise and power performance are very challenging and 2 architectures, are in phase of R&D demonstration to further select the best approach. Circuits configuration of the constant fraction discriminator with on pixel TDC and of the time-over-threshold discriminator with end-of-column DLL based TDC are presented and discussed. Spice simulations and layouts of the demonstrator circuits developed in 130 nm CMOS technology are presented and discussed.

OUTLINE

• Introduction,

- ASIC specification, architecture principle

• Analogue performance

Noise, speed, power

• Description of pixel cells

- TDC on pixel
- EOC pixel
- Bus architectures
- Simulation and layout of demonstrators

• Conclusions

R&D on two ASIC demonstrators

- Very challenging specifications, several contradictory issues
 - Very high counting rate: 50 Mhits/s/cm²
 - Peak occupancy of 4.5 Mhit/s in one column
 - No trigger, all hits are red out, data stream of 5 Gbit/s/chip expected
 - Low signal, most probable detector charge / MIP: 3 fC
 - 200 μm silicon sensor, for diamond even worse
 - a minimum threshold of 0.5 fC implies a noise ENC<200 rms e- ,factor 10 below threshold (10σ)
 - Signal speed requirement close to physical limit of silicon sensor
 - Time resolution of 100ps rms in the ASIC, not negotiable
 - to get 150 ps rms at system level
 - Affordable power consumption
 - 1800 pixels 300 μ m x 300 μ m should has a power less than 3W
 - Gigatracker operates in vacuum and should have minimum material in beam, 0.3 Xo
 - Radiation effects, 3.10¹⁴ p/cm²/year
 - Bulk damage on silicon sensor, leakage current and signal degradation induced by charge trapping,
 - GTK stations expected to be replaced each year with silicon sensors
 - Single event upset in the digital circuits of the pixel area
 - Induced digital noise on analogue circuits
 - Already observed in current pixel detector
 - Much more acute with extremely fast discriminators
 - The main problem is its unpredictability
 - Experimental characterization mandatory

The two NA62 GTK architectures options reminder

EOC architecture

No processing in pixel
Time stamping and data pipelining in EOC
Time walk correction by TOT

On pixel TDC architecture

On pixel TDC architecture on pixel time to digital conversion Constant fraction discriminator, no time walk correction



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130 nm IBM CMOS8RF DM noise analysis, silicon sensor signal

Preamp noise ENC f(Cd)

Parallel and series noise Drain current 40 μA, leakage current 20 nA 5 ns peaking time – shaping equivalent to CR-RC²

Input transistor optimization Series noise only



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On-pixel TDC option

• The circuit complexity is in the pixel

- Charge amplifier circuit optimized for 0.2 pF
- Constant fraction discriminator
- "analogue" TDC
 - based on time-to-analog-conversion (TAC) with Wilkinson ADC
- Data pipelining (4 cells deep) and formatting in pixel
 - -1^{st} stage of derandomization
- Synchronous Bus , clocked at 160 MHz
 - Digital CMOS level
- Looks like "LHC pixel ASICs "
 - With a factor 50 in rate and asynchronous hits flow
 - With a factor 20 on time precision:100 ps time stamping
 - No trigger, all hit data read out, ending up to 5 Gbit/s/ASIC

on-Pixel- TDC: analog front end

- Fast charge preamplifier optimized for 250 fF, peaking time of 5 ns
- Constant fraction discriminator (CDF) solves time walk issue
 - Compare one delayed and one attenuated copy of the input signal..
 - The two functions (delay and attenuation) are merged into CFD filter



CFD spice simulation

Transient Response

- outn0 (qin = 1.00e+00)
 - outn0 (qin = 2.00e+00)
 - outn0 (qin = 3.00e+00)
 - outn0 (qin = 5.00e+00)
 - outn0 (qin = 5.00e+00)
 - outn0 (qin = 5.00e+00)
 - outn0 (qin = 3.00e+00)
 - outn0 (qin = 3.00e+00)
 - outn0 (qin = 1.00e+00)
 - outn0 (qin = 2.00e+00)
 - outn0 (qin = 2.00e+00)
 - outn0 (qin = 2.00e+00)



Transient Response

- $\ (qin=1.00e+00) \ (qin=2.00e+00) \ (qin=3.00e+00) \ (qin=4.00e+00) \ (qin=5.00e+00) \ (qin=5.$
- $\langle 0 \rangle + (qin=9.00e+00) \langle 0 \rangle + (qin=1.00e+01) \langle 0 \rangle (qin=1.00e+00) \langle 0 \rangle (qin=2.00e+00)$



• Output signal of the differential preamplifier (left) and CFD (right) for input charge pulses from 1 to 10 fC, peaking time 4 to 5 ns

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Simulation of Jitter and Time walk

• Jitter (red) and walk (blue) for input charge pulses from 1 to 10 fC



Jitter Monte Carlo simulation based on Landau fluctuations in 200µm Si. sensor



• Total resolution calculated through Monte-Carlo based on the jitter and residual walk measuremets of the first prototype.

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Analog TDC measures CFD-CLK edges



7-bit TAC based on modified Wilkinson TDC:

- Potential transfer from C to 4C allows for current ratio reduction from 1:128 to 1:32
- Better matching of same polarity current sources
- **1.** Current source I1 charges capacitor C for the time between the CFD signal and a clock front.
- 2. Capacitor 4C is charged to the potential at the output of the amplifier
- (VA) the charge transferred on 4C is 4 times the charge stored on capacitor C.
- **3. Capacitor 4C is charged back to Vref by current source I2.**
- During step 3 the counter is enabled.

Pixel digital processing

Pipelining

Time sequence



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EOC pixel cell, bus, walk, noise



• The processing complexity is in the bus and Time walk 150 ps rms end of column, not in pixel cells For 0.9 fC to 5.4 fC

- Analog front end:
 - Preamplifier, trans-resistance configuration
 - Shaping CR RC² 5ns peaking time
- Discriminator
 - Time over threshold
- Very low current swing, Asynchronous Bus
 - Differential line driver coupled to a differential transmission line
 - Low swing differential signal 10 mV/100 μ A
 - Pre-emphasis to boost signal transport speed

Noise simulation for 0.75 fC input, jitter 150 ps



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Worse case for diamond₁sensor

Low swing transmission line driver RF bus system



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Signal Pre-emphasis in lossy transmission lines

Near speed of light propagation

Pre-emphasis for 13.5 mm line



Low swing current receiver SPICE simulation of hits in bus



Transmission line, pixel cell design



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End of column processing



ASIC R&D

End of column logic Layout

9x2 receiver blocks sensing the 9 transmission lines of one column

TDC: End of column logic with 2x9x32-bit hit registers, 100 ps-32 bit delay line, charge pump

Options Comparison

On pixel TDC option

- Noise ENC: < 200 e-
- Timing : < 100 ps
- Power in pixel: 0.65 mW with local time digitization and data derandomization.
- Most power in pixel circuit
- SEU susceptibility
 - Addressed with special design techniques
- Susceptibility to digital noise
 - Needs special care because of CMOS activity in pixel area
- Output rate
 - Minimum with CFD

End of Column option

- < 200 e-
- <100 ps
- 0.25 mW/pixel
- Most power in EOC circuit
 - Not a concern at the pixel level
 - No CMOS digital activity in pixel area, except low swing bus
 - Bigger data rate due to TOT, local processing might reduced it

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Conclusions

• Simulations of both ASIC design options

Are encouraging and indicates good feasibility

• However devil is in the details

- On- pixel TDC design
 - CFD has a large bandwidth
 - SEU effects should be circumvented
 - Digital activity in pixel area should be carefully shielded
- EOC pixel design
 - waveguide design with pre-emphasis is not trivial
 - Modeling issue
 - Low swing RF bus system rather complex and unknown
 - EOC Pixel architecture never tested

Measurement of the prototype

• Measurements Jitter (left) and time-walk (right) for input charge pulses from 1 to 10 fC