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A Pixel readout architecture for the NA62 Gigatracker based on End Of Column TDC

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We present the ASIC development of the readout electronics of the Gigatracker pixel detector of NA62. Gigatracker speed , noise and power performance are very challenging and 2 architectures , are in phase of R&D demonstration to further select the best approach. Circuits configuration of the constant fraction discriminator with on pixel TDC and of the time-over-threshold discriminator with end-of-column DLL based TDC are presented and discussed. Spice simulations and layouts of the demonstrator circuits developed in 130 nm CMOS technology are presented and discussed.

Summary

The NA62 Gigatracker pixel ASIC comprizes an array of 1800 pixel of 300 um each and an End of Column logic on the periphery of the ASIC. The pixel array is stuctured into 40 columns of 45 pixel cells. The pixel circuit comprizes an ultra fast preamplifier and discriminator followed by a differential line driver designed to minimize both digital signal activity and power consumption. The End of Column logic comprizes differential line receivers, banks of TDC's and readout FIFO's that performs derandomisation and data pipeline before to send data off chip.
We present the design aspects of this challenging ASIC architecture, in particular design solutions that have been used to implement subnanosecond circuit in a low power architecture, and the integration of array of TDC's in a front end ASIC, to date the first one implemented.

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