Contribution ID: **105** Type: **Poster**

# The Alice Pixel Trigger Control and Calibration

*Thursday, 18 September 2008 16:15 (20 minutes)*

The ALICE Silicon Pixel Detector (SPD) optical data stream includes 1200 Fast-OR signals indicating the presence of at least one pixel hit in each of the detector readout chips. The Pixel Trigger (PIT) extracts the Fast-OR signals from the data lines and processes them to contribute to the Level 0 trigger in the ALICE Central Trigger Processor (CTP).
We present here the design, the implementation and the first operational experience of the PIT Control and Calibration system.
The PIT Control system includes original hardware and software solutions to implement coordinated operation of the PIT with the various ALICE systems to which it interfaces to.

## Summary

The ALICE Silicon Pixel Detector (SPD) comprises the two innermost layers of the ALICE inner tracker system. The SPD contains 120 detector modules each including 10 readout chips. Each of these pixel chips generates a digital Fast-OR output signal indicating the presence of at least one pixel hit in its pixel matrix.
The Pixel Trigger (PIT) System has been implemented to process the 1200 Fast-Or signals from the SPD and provides an input signal to the ALICE Central Trigger Processor (CTP) for the fastest (Level 0) trigger decision within a latency of 800 ns.
The PIT processor interfaces with several ALICE systems: it receives input data from the SPD, it accepts configuration commands from the CTP and sends status information to the Alice Experimental Control System (ECS).
The PIT control system required an accurate design of hardware and software solutions to implement coordinated operation of the PIT and the ALICE systems to which it interfaces to.
We present here the design, the implementation and the first operational experience of the PIT Control and Calibration system.
The hardware configuration and control are implemented via the ALICE Detector Data Link, on top of which a custom control system has been implemented.
A driver layer has been realized under stringent requirements of robustness and reusability. It qualifies as a general purpose hardware driver for electronic systems equipped with the ALICE DDL front end board (SIU).
Various testing and calibration procedures need to be performed on the SPD and the PIT systems in order to provide an optimized trigger signal to the CTP.
These include methods to compensate all signals propagation delays and automatic SPD DAC scans to tune the detector response.
The PIT control system has been tailored to implement automatically most of the former procedures, requiring coordinated and extensive information exchange between the interfacing systems.

**Primary authors:** KLUGE, Alexander (CERN); TORCATO DE MATOS, Cesar (University of Minho); RIBEIRO, Fernando (University of Minho); AGLIERI RINELLA, Gianluca (CERN); CHOCHULA, Peter (CERN)

**Presenter:** TORCATO DE MATOS, Cesar (University of Minho)

**Session Classification:** POSTERS SESSION