Contribution ID: **38** Type: **Poster**

Instrumentation for Gate Current Noise Measurements on sub-100 nm MOS Transistors

Thursday 18 September 2008 16:15 (20 minutes)

This work describes a laboratory instrument that was developed to characterize the gate current noise performances of CMOS devices with minimum feature size in the 100 nm span. As a consequence of the reduction of the gate oxide thickness, these devices are affected by a non-negligible gate current due to direct tunneling phenomena. In this paper, the analysis of this noise contribution is particularly aimed at evaluating the resolution limits of readout circuits that will be used in future high energy physics (HEP) experiments. The noise measuring instrument and some of the results of gate current noise characterization will be presented.

Summary

In the last decade, the requirements of high granularity in the design of the readout electronics for HEP experiments have led to an extensive use of deep-submicron CMOS devices. While approaching the 100 nm span, the CMOS technology has entered the sub-3 nm gate oxide thickness regime. In such a regime, MOSFET devices exhibit a non-negligible gate-leakage current, due to the finite probability of electrons directly tunneling through the insulating SiO2 layer. This current contribution, which originates from discrete charges randomly crossing a potential barrier, is affected by noise fluctuations which may degrade circuit performance in analog applications.

In particular, in detector readout circuits integrated in sub-100 nm CMOS technologies, the resolution, which is limited by the noise from the input transistor, may be degraded by the parallel noise source in the device gate current. In order to evaluate the effects of this noise contribution, and also to supply suitable design criteria, accurate characterization and modeling of gate current noise are mandatory.

The noise characterization is carried out by means of a purposely developed instrument with the required accuracy in an adequate frequency range, considering the dependence of the gate current from device geometry and bias conditions. This measuring instrument consists mainly of a transimpedance stage amplifying the noise due to the gate-leakage current, which is detected by a commercial spectrum analyzer. The constraint for the minimum detectable noise is essentially dictated by the noise of the amplifier and its feedback resistor: the value of such a component has been chosen as a compromise between accuracy and bandwidth of the measuring system. As a consequence, it was possible to carry out measurements from 1 Hz up to 100 kHz. Nevertheless, such a bandwidth allows us to fully characterize the gate current noise, which exhibits white, 1/f and Lorentian-like behavior in this frequency range.
After presenting the details of the interface circuit design, the setup and procedures for gate noise measurement, results relevant to transistors belonging to a 90 nm technology will be also presented and discussed.

The last part of this work will be devoted to evaluating the impact of gate current noise on the equivalent noise charge (ENC) performance of front-end circuit, especially at long (> 100 ns) shaping times, where such a contribution may become an issue.

Primary author: GAIONI, Luigi (Università di Pavia, I-27100 Pavia, Italy)

Co-authors: TRAVERSI, Gianluca (Università di Bergamo, I-24044 Dalmine (BG), Italy); RATTI, Lodovico (Università di Pavia, I-27100 Pavia, Italy); MANGHISONI, Massimo (Università di Bergamo, I-24044 Dalmine (BG), Italy); SPEZIALI, Valeria (Università di Pavia, I-27100 Pavia, Italy); RE, Valerio (Università di Bergamo, I-24044 Dalmine (BG), Italy)

Presenter: GAIONI, Luigi (Università di Pavia, I-27100 Pavia, Italy)

Session Classification: POSTERS SESSION