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Fast FPGA-based trigger and data acquisition system for the CERN experiment NA62: architecture and algorithms

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We present the design of the trigger and DAQ system for NA62, with
emphasis to the first level of trigger (L0).
The L0 level runs on-line and is designed as a segment of the DAQ chain.
FPGAs are used to evaluate fast trigger conditions, entirely on
the digitized information from read-out electronics.
In this way, the whole digitized information from detector is available
for triggering and no separate branchs of read-out electronics are
necessary.
We shall present our design for the L0 architecture, the implementation of
trigger conditions on the FPGAs, the hardware we developed and tests.

Summary

Here we present the design of the trigger and DAQ system for NA62, with
emphasis to the first level of trigger (L0).
NA62 is an experiment hosted at CERN, which aims to measure the branching
fraction of the ultra-rare K+—>pi+nunubar decay (expected at order of
10^-10).
The trigger is organized in three levels, performing a data bandwidth
reduction from an overall size of 1-2 TB/s produced by continuous
digitization of detector hits, down to few tens of KB/s for permanent mass
storage.
The L0 level of trigger runs on-line and is designed as a segment of the DAQ chain, where the evaluation of
fast trigger conditions is performed entirely on
the digitized information from read-out electronics.
In this way, the whole digitized information from detector is available
for triggering and no separate branchs of read-out electronics are
necessary (as usual in this kind of experiments).
This feature has relevant impact on trigger control, flexibility and cost effectiveness, that will be addressed in
the presentation.
The L0 level is implemented in hardware (further levels in software)
within a set of TELL1 boards, the same used for a common trigger and
read-out data flow in the LHCB experiment.
Mezzanine cards containing high performance TDCs plugged in the TELL1
process discriminated detector signals and provide the internal TELL1
FPGAs with digitized hit times. This information is used to evaluate fast
trigger conditions within the FPGAs.
We shall present our design for the L0 architecture, the implementation of
trigger conditions on the FPGAs, the hardware we developed and tests.

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