Digital part of PARISROC: a photomultiplier array readout chip

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Abstract

PARISROC is the front end ASIC designed to read 16 PMT for neutrino experiments. It's able to shape, discriminate, convert and readout data in an autonomous mode. The digital part manages each channel independently thanks to 4 modules: top manager, acquisition, conversion and readout. Acquisition is in charge to manage the SCA with a depth of 2 for charge and fine time measurement. Coarse time measurement is made with a 24 bits gray counter. Readout module sends converted data of hit channels to an external system. Top manager controls the start and stop of the 3 others modules. The ASIC was submitted in June 2008.

I. GENERAL OVERVIEW

A. Experiment overview

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the PMM2 R&D project dedicated to neutrino experiments [1]. This project is funded by the French National Agency for Research under the reference ANR-06-BLAN-0186.

Next generation of neutrino experiments which will take place in megaton size water tanks will require very large surface of photodetection and volume of data [2]. For the funded project, this large surface of photodetection is segmented in macro pixels made of 16 PhotoMultiplier Tubes (PMT) connected to an autonomous front end ASIC: PARISROC. A module with 16 PMT is shown in Figure 1.
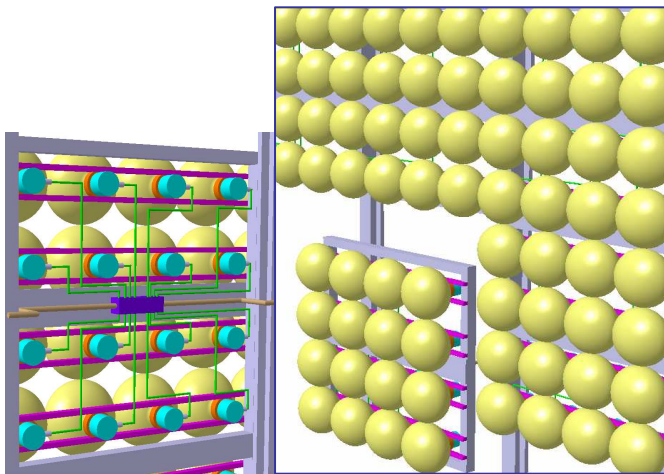

Figure 1: 16 PMT module

B. ASIC overview

PARISROC is able to read 16 PMT. It's a triggerless chip and can work in an autonomous mode [3]. The block diagram of the ASIC is given after in Figure 2.
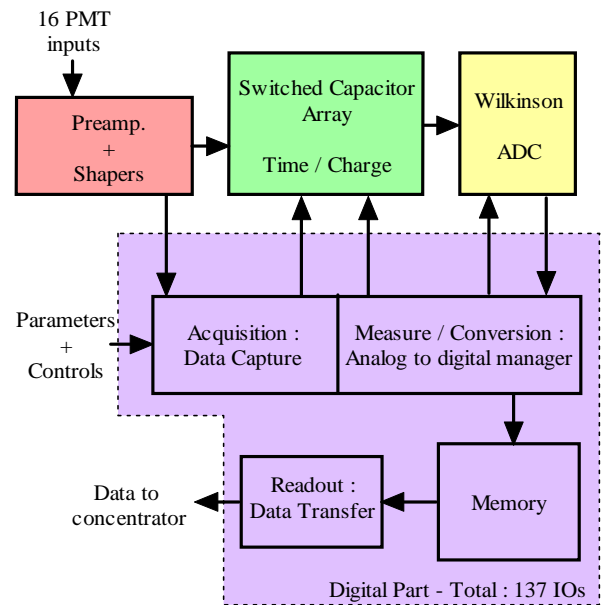

Figure 2: Block diagram of PARISROC

It allows time tagging and charge measurement. Time tagging is composed of a coarse and a fine time measurement. Coarse time is handled by a 24 bits counter at 10 MHz and fine time by a 12 bits TDC ramp. The main characteristics of the ASIC are in table 1 below.

Table 1: Main characteristics

Technology:	Austria-Micro-Systems (AMS) SiGe 0.35μm
Area:	17 mm^2 (5mm × 3.4mm)
Power Supply:	3.3 V
Package:	CQFP 160

C. Overview of the digital part

The digital part of PARISROC is built around 4 modules which are acquisition, conversion, readout and top manager. Actually, PARISROC is based on 2 memories: during acquisition, discriminated analog signals are stored into an analog memory (the SCA: switched capacitor array). The analog to digital conversion module converts analog charges

and times from SCA into 12 bits digital values. These digital values are saved into registers (RAM). At the end of the cycle, the RAM is readout to an external system. A simple view of operation is shown on Figure 3.
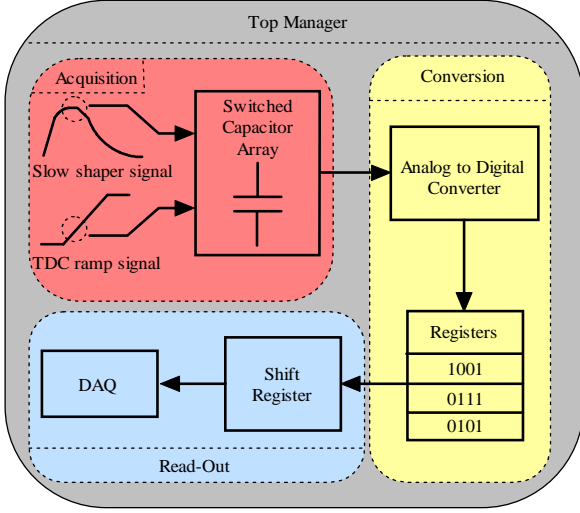

Figure 3: High level operation

II. ASIC DESCRIPTION

A. Low level block diagram

The low level block diagram of the ASIC is given below in Figure 4.
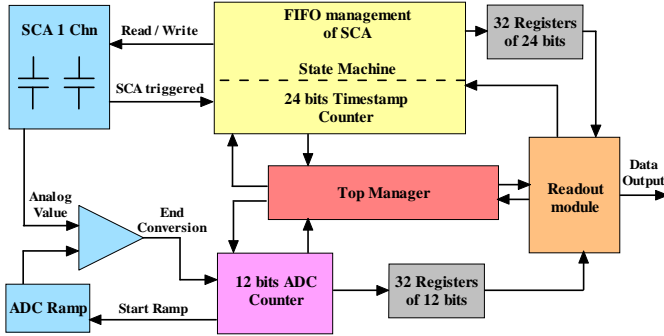

Figure 4: Low level block diagram

The 16 channels of PARISROC are managed independently, 2 state machines are dedicated to handle one channel: 1 for write pointer and 1 for read pointer. Besides, 32 registers of 24 bits are needed to save coarse time for each depth of SCA. We can consider that the SCA of one channel is controlled as an analog FIFO.

Conversion is common for all channels and needs 32 registers of 12 bits to store converted data: 16 for charges and 16 for fine time measures.

As the readout will only treat hit channels, this module will tag each frame with its channel number.

B. Detail of one SCA channel

The chip has 16 channels. Each channel has a depth of 2 for charge and 2 for fine time storage. The SCA column is selected, read and erased by the digital part. The detail of 1 SCA channel is shown below in Figure 5.
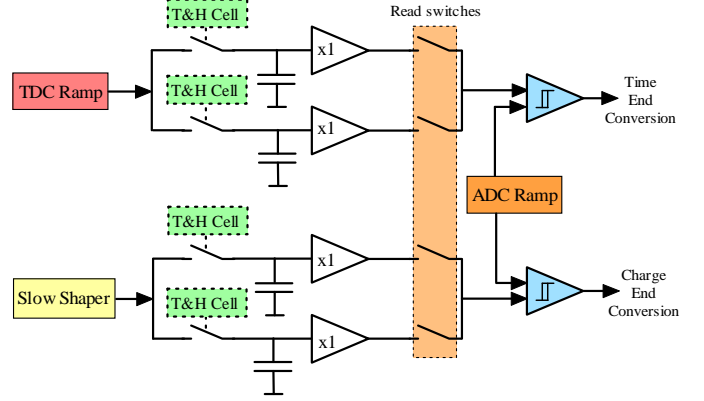

Figure 5: Detail of 1 SCA channel

"Track & Hold Cell" allows to lock the capacitor value only when a calibrated trigger occurs within the selected column. This operation is given below in Figure 6.
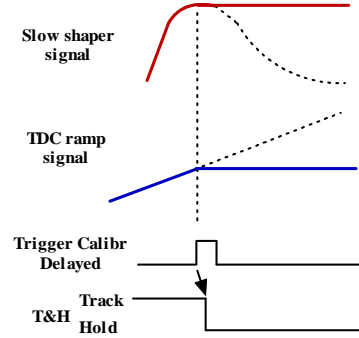

Figure 6: Operation of T&H cell
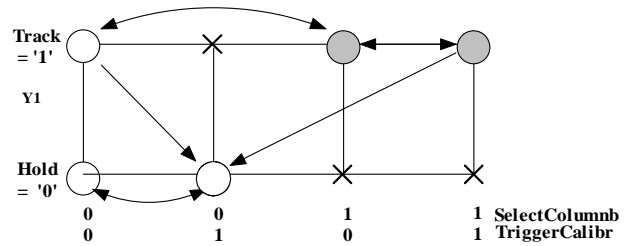
Detailed description is shown in Figure 7.

Figure 7: Detailed description of T&H cell

III. MODULES OF THE DIGITAL PART

A. The Top Manager

The top manager module controls the 3 others ones. It allows to start and to stop them in order to realize the right sequence for an autonomous working.

When 1 channel is hit, the top manager waits for a constant time to allow triggers on others channels. Then, it

starts ADC conversion and readout of digitized data. The maximum cycle length is about 200µs when all channels are hit.

During conversion and readout, acquisition is never stopped. That's mean that discriminated analog signals can be stored in the SCA at any time of the sequence if SCA is not full. This operation mode is managed by the state machine given in Figure 8.
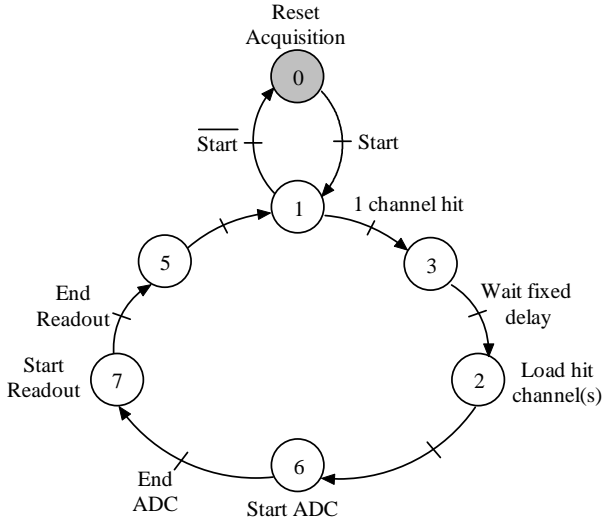

Figure 8: Top manager state machine

B. Acquisition

This module is dedicated to charge and time measurements. It manages the SCA where charge and fine time are stored as a voltage. It also integrates the coarse time measurement thanks to a 24 bits gray counter with a resolution of 100 ns.

Each channel has a depth of 2 for the SCA and they are managed individually. Besides, SCA is treated like a FIFO memory: analog voltage can be written, read and erased from the memory. The acquisition block diagram is given below in Figure 9.
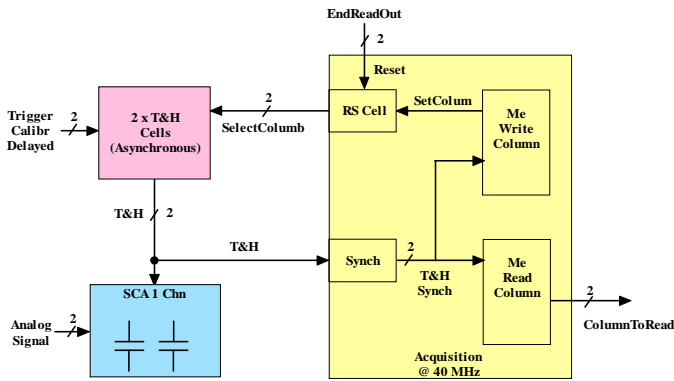

Figure 9: Acquisition module

Analog FIFO memory for one channel is managed by 2 state machines: 1 for write/erase and 1 for read operation. The state machines are shown in Figure 10 and 11.
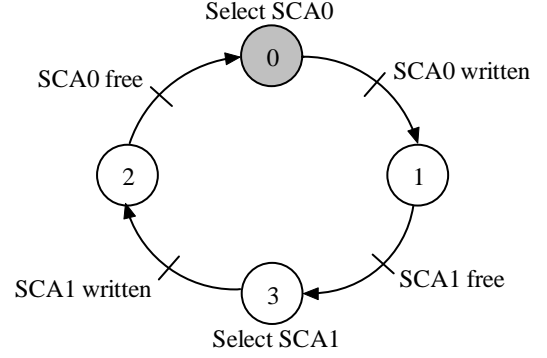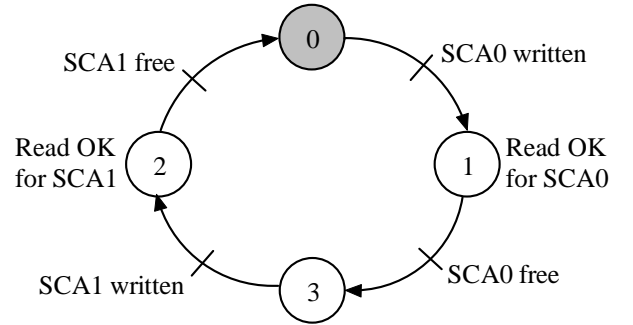

Figure 10:   Write/Erase operations

Figure 11:   Read operation

C. Conversion

The main purpose of this module is to convert analog values stored in the SCA in digital ones thanks to a 12-bit Wilkinson ADC. The ADC clock frequency is 40 MHz, it implies a maximum ADC conversion time of 103 µs.

Each ADC run converts the fine time and the charge of each channel even if it was not hit: 32 conversions in 1 run. Only the data of hit channel will be treated by the readout module. The block diagram is given after in Figure 12.
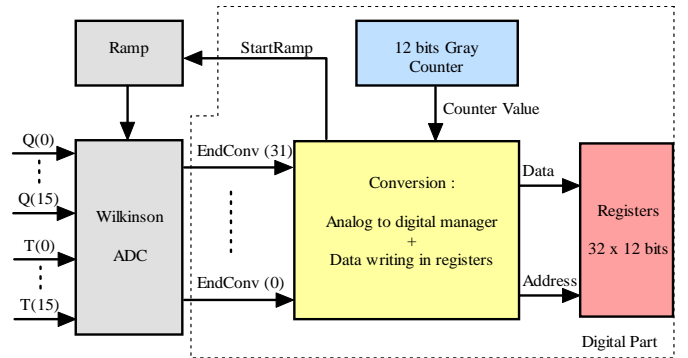

Figure 12:   Conversion module

D. Readout

The Readout module, shown in Figure 13, permits to empty the registers. It works as a selective readout: only hit channels are transferred. In the case of all channels hit, about 832 bits of data are transferred to the concentrator with a 10 MHz clock.

The pattern used is composed of 4 data: 4-bit channel number, 24-bit coarse time, 12-bit charge and 12-bit fine time. Each data is coded in gray and the length of one frame is 52 bits.

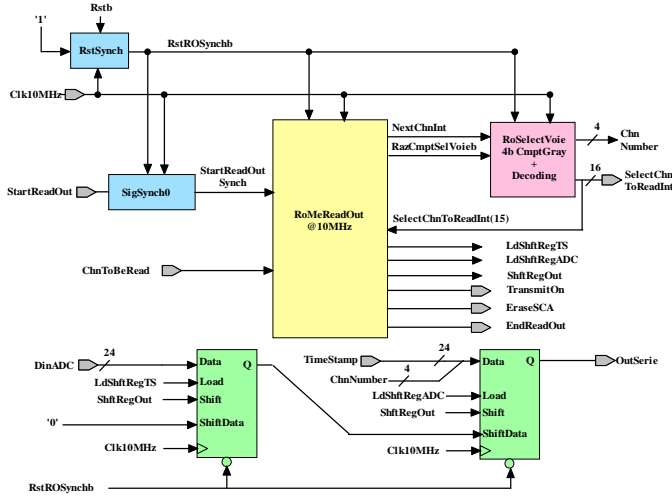When all channels are hit, the readout takes about 100 µs: the time between 2 frames is about 1 µs.

Figure 13:   Readout module

IV. DIGITAL PART LAYOUT

The layout of the digital part was realized in 0.35 µm technology from Austria Micro System (AMS) [4] and designed with Soc Encounter from CADENCE.

The layout is on 3 metals (blue, red and green) and its size is 1800 µm by 1000 µm.

The layout is composed by 10K standard cells (equivalent to 71K transistors).

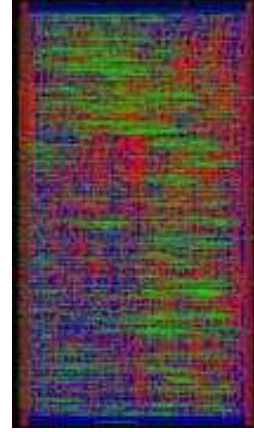It integrates 1152 memory registers and has a total net length of 1 meter. It's given in Figure 14.

Figure 14:   Digital part layout

V. CONCLUSION

PARISROC is a complete triggerless and autonomous ASIC for the PMM2 experiment. It was submitted in June 2008 and the first results are expected at the end of the year.

Digital part has many features included to manage the entire chip for acquisition, conversion and readout. As the acquisition module is completely new in order to have all channels independent, many tests will be performed on this new structure.

VI. REFERENCES

[1] http://pmm2.in2p3.fr/

[2] B. Genolini et al., *PMM2: LARGE PHOTOMULTIPLIERS AND INNOVATIVE ELECTRONICS FOR THE NEXT GENERATION NEUTRINO EXPERIMENTS*, NDIP 2008 conference.

[3] G. Martin-Chassard et al., *PMm2 ASIC: PARISROC*, TWEPP 2008 conference.

[4] http://www.austriamicrosystems.com/