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Digital part of PARISROC: a photomultiplier array readout chip

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PARISROC is the front end ASIC designed to read 16 PMT for neutrino experiments. It's able to shape, discriminate, convert and readout data in an autonomous mode. The digital part manages each channel independently thanks to 4 modules: top manager, acquisition, conversion and readout. Acquisition is in charge to manage the SCA with a depth of 2 for charge and fine time measurement. Coarse time measurement is made with a 24 bits gray counter. Readout module sends converted data of hit channels to an external system. Top manager controls the start and stop of the 3 others modules. The ASIC will be submitted in June 2008.

Summary

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the PMM2 R&D project dedicated to neutrino experiments. Next generation of neutrino experiments that will take place in megaton size water tanks will require very large surface of photodetection and volume of data. For the funded project, this large surface of photodetection is segmented in macro pixels made of 16 Photomultiplier tubes (PMT) connected to an autonomous front end ASIC: PARISROC.

The digital part of the ASIC is made of 4 modules which are acquisition, conversion, readout and top manager. Actually, PARISROC is based on 2 memories. During acquisition, discriminated analog signals are stored into an analog memory (the SCA: switched capacitor array). The analog to digital conversion module converts analog charges and times from SCA into digital values. These digital values are saved into registers (RAM). At the end of the cycle, the RAM is readout to an external system.

The SCA of each channel are managed independently like a FIFO. During acquisition data are written into the SCA. In fact the voltage is held into the capacitor thanks to a "track and hold"cell. When analog to digital conversion is in progress, analog signals are read and compared to a ramp of a Wilkinson ADC. Finally, after the readout, data are erased from the SCA. Then, the SCA is operational for another acquisition (track mode). As the SCA depth is 2, during conversion and readout discriminated signals can still be stored in the SCA.

For the readout, only hit channels are send out with a pattern of 4 data: channel number, coarse time, charge and fine time. Each data is coded in gray and the total number of bit for one frame is 52 bits.

The top manager module controls the 3 others ones (Acquisition, Conversion, Readout). When 1 channel is hit, it waits a constant delay to allow triggers on others channels. Then ADC conversion and readout are respectively launched. The maximum cycle length is about 200µs when all channels are hit.

The layout of PARISROC is made in AMS 0.35µm SiGe process. The dimension of the digital part is about 1800 x 1000µm with a total number of I/O of 137. The ASIC will be submitted in June 2008 and first tests results are expected at the end of 2008. PMM2 is funded by the French National Agency for Research under the reference ANR-06-BLAN-0186.

Primary authors: Mr DE LA TAILLE, CHRISTOPHE (Laboratoire de l Accelerateur Lineaire); Mr DULUCQ, FREDERIC (Laboratoire de l Accelerateur Lineaire); Mrs MARTIN-CHASSARD, GISELE (Laboratoire de l Accelerateur Lineaire); Ms CONFORTI, SELMA (Laboratoire de l Accelerateur Lineaire)

Presenter: Mr DULUCQ, FREDERIC (Laboratoire de l Accelerateur Lineaire)

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