Microelectronics User's Group @ twepp2008

Topical Workshop on Electronics for Particle Physics

Naxos, Greece

16/9/2008

Agenda

- Presentation:

  "Access to ASIC design tools and foundry services at CERN for SLHC"

- Open discussion

Access to ASIC design tools and foundry services at CERN for SLHC

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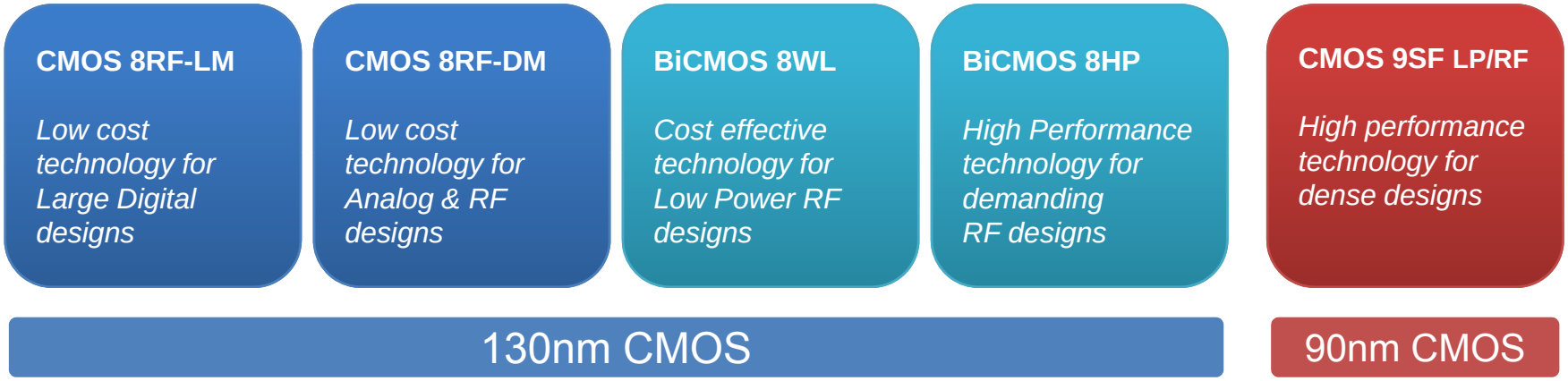
Introduction

- Access to advanced technologies through CERN
- The 130nm Digital Design Kit
- Access to Foundry Services through CERN

Overview of Technologies



- 130 (CMOS and BiCMOS) and 90 nm contract available since 6/2007.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.

CMOS8RF Technology Features

Standard Features

- **130 nm lithography, twin-well on 1-2 Ω-cm non-epi P- substrate, low K dielectric**
- **Thin Oxide (22Å gate) FETs (1.2 /1.5V)**
- **Thin Oxide MOS Varactors**
- **Forward bias diodes**
- **N-well resistor**
- **5 to 8 levels of metal**
  - Thin and thick Cu metal (~0.3/0.55 μm)
  - Last metal options:

    LM: Cu 0.55μm DM: 3 μm Cu + 4 μm Al
- **Vertical Natural Capacitor**
- **Spiral inductors, RF Transmission lines**
  - Series & Symmetrical inductors in DM wiring option only
- **Electrically programmable fuses**
- **Wire bond or solder bump (C4) terminals**

Optional Features

- **Triple-well NFETs**
- **Thin Oxide Low power FETS**
- **Thin Oxide Low-Vt FETs**
- **Thick Oxide (52Å) 2.5V FETS**
- **Thick Oxide (52Å) 3.3V FETS**
- **Thin and thick Oxide Zero-Vt NFETs**
- **Thick Oxide MOS Varactors**
- **Hyperabrupt Varactor**
- **Polysilicon and diffused resistors**
- **TaN metal resistor**
- **Single and dual-layer MIM capacitor (DM option only)**

CMOS8RF Wiring options

	LM Last Metal						DM Last Metal				
	8	7	8	7	6	5	6	7	7	8	8
DM Option							MA	MA	MA	MA	MA
							E1	E1	E1	E1	E1
							LY	LY	LY	LY	LY
LM Option	LM	LM	LM	LM	LM	LM					
2X Levels	MG	MG							MG	MG	
	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ
1X Levels			M6								
	M5		M5	M5							
	M4	M4	M4	M4	M4						M4
	M3	M3	M3	M3	M3	M3		M3		M3	M3
	M2	M2	M2	M2	M2	M2	M2	M2	M2	M2	M2
	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
Code	5-2	4-2	6-1	5-1	4-1	3-1	2-1	3-1	2-2	3-2	4-1

Access to Technology Data

- What you need to start designing.

- Distributed by CERN

Technology	Process	Distributable
CMOS8RF-LM	130nm	IBM PDK, Digital Kit
CMOS8RF-DM	130nm	IBM PDK
BiCMOS8WL	130nm (SiGe)	IBM PDK
BiCMOS8HP	130nm (SiGe)	IBM PDK, IBM PDK
CMOS9SF	90nm	

- IBM PDK : Physical Design Kit for Analog and full custom design.
- Digital Kit : Design Kit that supports Digital design.

Digital Design Kit

Challenges

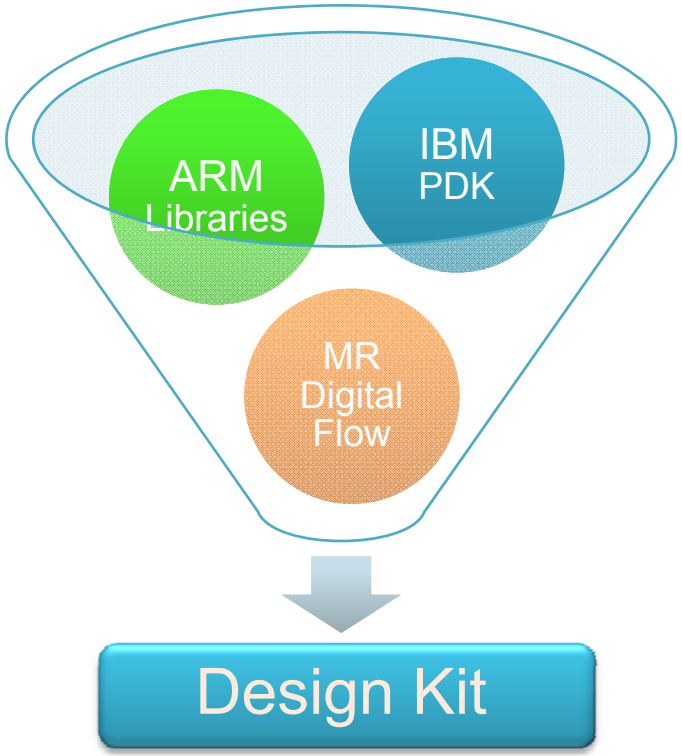
- Technology
  - Complex physical design rules and Manufacturability constrains.
  - Multiple corners for design simulations.
  - Tough Signal Integrity issues, and difficult final Timing Closure.
  - Expensive prototyping.
- CAE Tools
  - Multiplicity of tools and complicated - non linear - design flows.
  - Numerous data formats used when interfacing tools from different tool vendors.
- Designs
  - Demanding Power analysis and power management.
  - Chip level integration and assembly.
  - Large chips require to extend design efforts to multiple teams across geographically distributed institutes.

Objectives

- Formalize the digital design flow in our design environment.
  - Allow designers of the HEP community to become familiar with complex tools, necessary to master large designs in a modern technology.
- Assist large digital design with an automated flow.
- Common design platform across multiple institutes.
  - Enhance team productivity.
- Provide a silicon accurate methodology.
  - Increase silicon reliability.

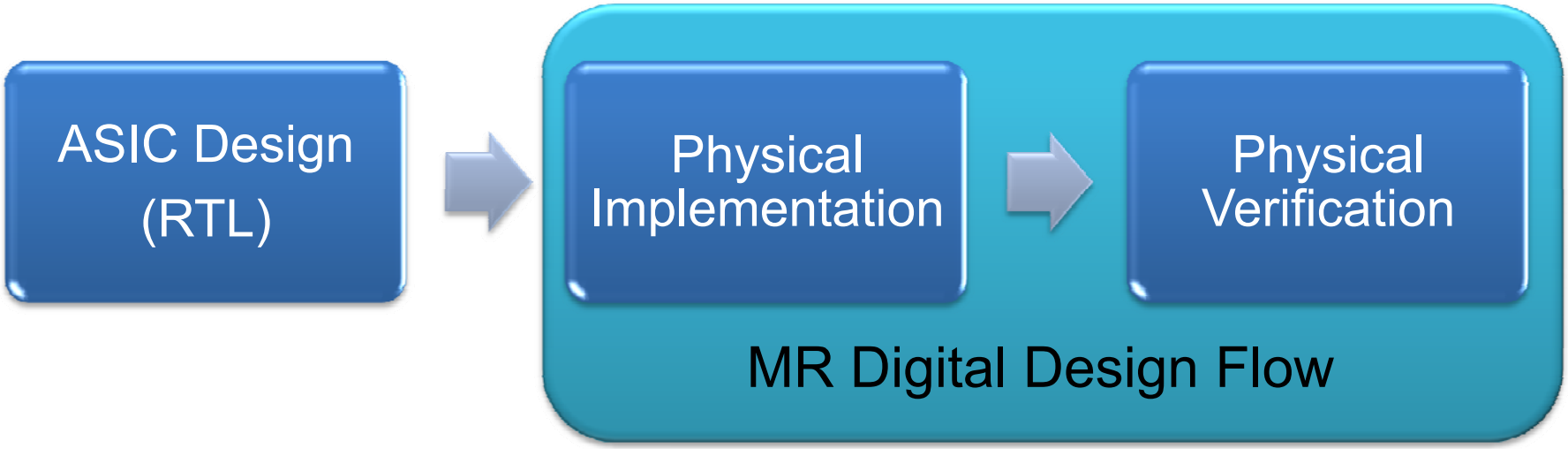
The CMOS8RF Design Kit

- Target process: CMOS8RF-LM (130nm)
- Features:
  - Integrate the ARM core & IO library cells.
  - Consolidate the usage of CAE tools.
  - Provide a complete and automated Digital design flow.
- Distribution:
  - CERN
  - External Institutes
    - Already installed in 7 labs.
- Training:
  - 5 training courses organized @ CERN



The MR Digital Flow

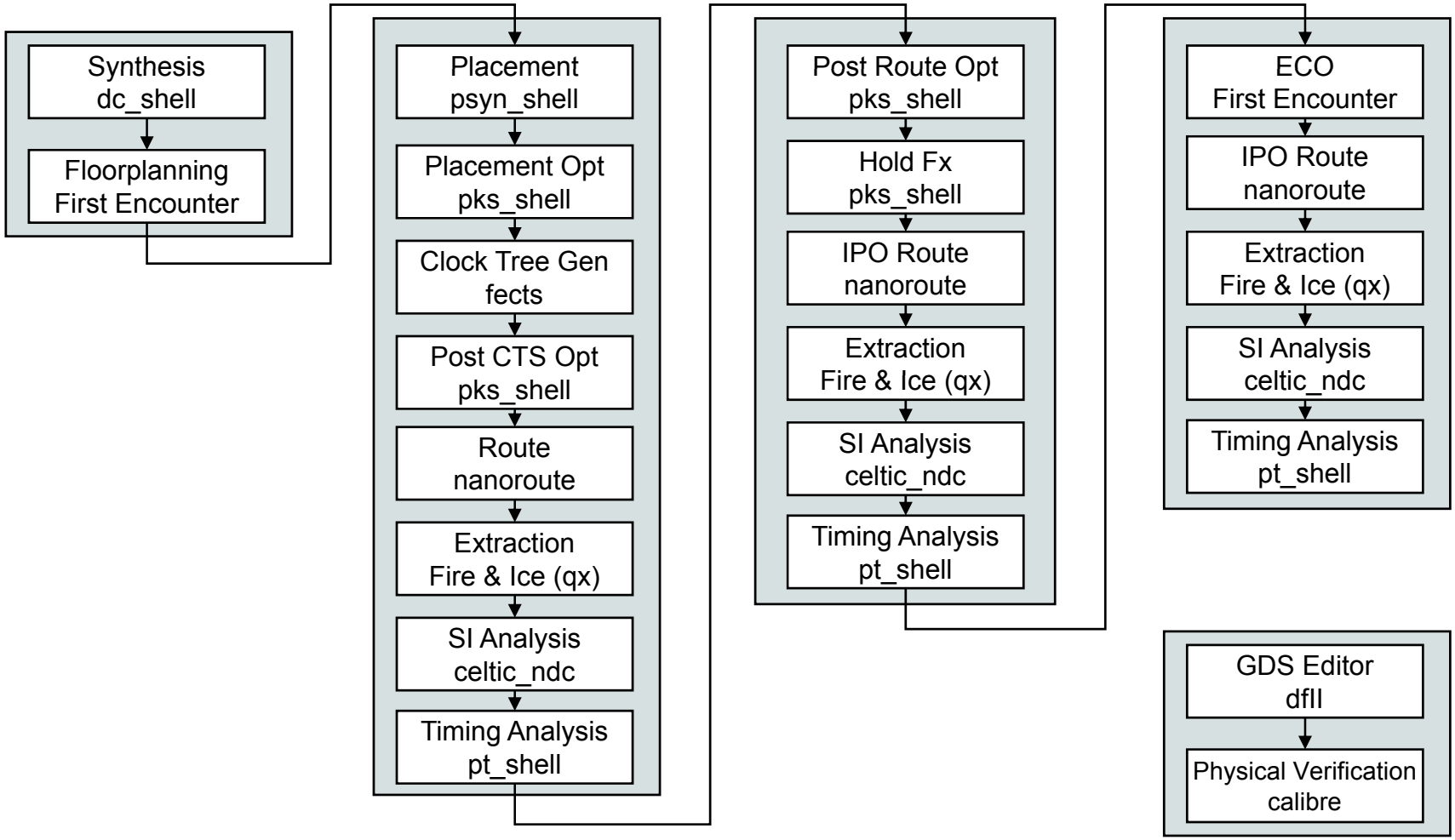
RTL – TO – LAYOUT



Formalize the Digital Design Flow in our work environment.

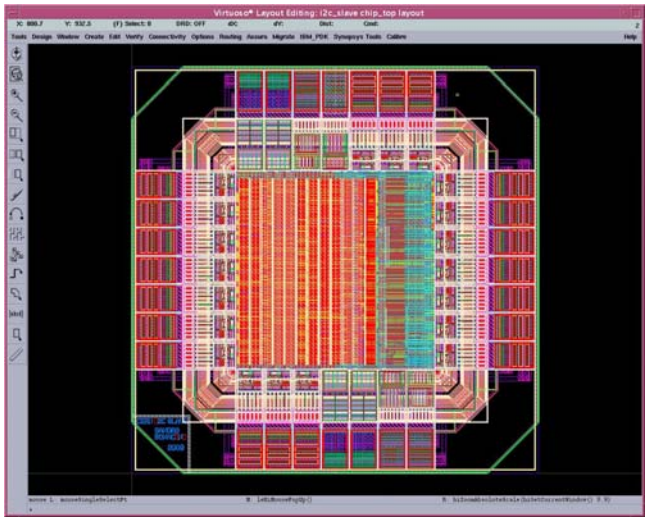
Provide a common platform for design tools.

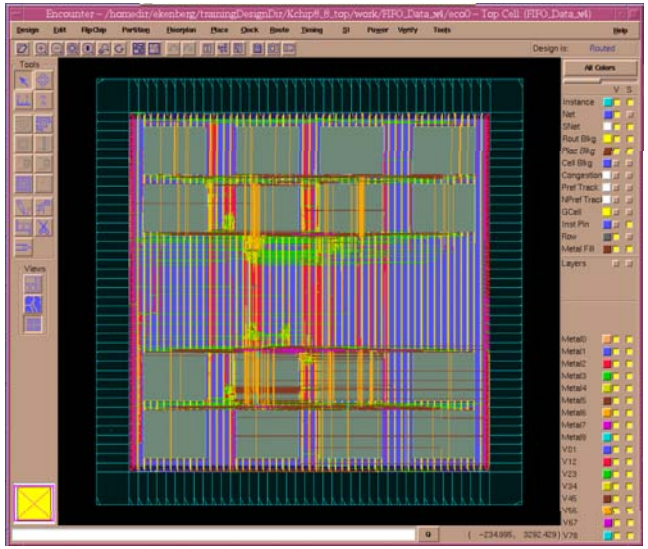
The MR Digital Flow in detail



V1.4 Design Kit validation

- Validating the kit:
  - I^2C interface chip
    - Full digital chip.
  - Preshower Kchip
    - Third party IP core integration (DP SRAM).
    - FIFO controller P&R O.K.
    - Implemented in 6LM and 8LM metal stacks.
    - Used as example in training courses.





Development Roadmap

V1.4 (current version)

- Change list
  - Integrate the IBM PDK V1.4.0.3
  - Integrate the ARTISAN GPIO 2007q3V2
  - Bug fixes.

V1.5 (4Q2008)

- Change list
  - Integrate the IBM PDK V1.4.0.10
  - Integrate C4 IO pads
  - Support latest Europractice distribution of CAE tools.
  - Bug fixes

END Of LIFE

- Evolution in industry (MR inc. and ARM) is forcing us to discontinue the development work and eventually the technical support of the Digital Design kit.
- A **New Design Kit** solution is currently being studied.
  - Cover broader spectrum of functionalities (Analog, Digital & Mixed Signal design.)
  - Based on a commercially available solution.
  - Depending on demand, the kit could be made available for distribution in 2Q,2009.
  - Cost is expected to be higher than the previous solution.

New Design Kit Functionalities 1/2

Preliminary information

- Design Environment Setup
  - Integrates foundry PDKs, and Physical IP libraries.
  - Initialises the CAE tools design environment (env. variables, files, and directory structures) to meet the target technology configuration. (ex. BEOL options).
  - No additional coding or scripting necessary.
  - Configuration management per designer and per project.

- Analog & Mixed Signal (AMS) methodology.
  - Top-down design Partitioning.
  - Top-down mixed-Signal Simulation & design Concept Validation
    - Concurrent use of behavioural models, transistor-level schematics and simulation testbenches.
  - Multiple power supply management.
  - Semi-automated Flow for digital implementation
  - Hierarchical design Floorplaning and Physical Assembly
  - Design Performance Validation and Physical Verification

New Design Kit Functionalities 2/2

Preliminary information

- Automated Digital Flow
  - RTL-to-GDSII path, for rapid development of larger digital designs.
  - Based on platform independent tcl-code.
  - GUI and command mode interfaces.
- IP integration workflow
  - Ability to seamlessly integrate IP from multiple sources in the Design Kit.
  - Generates all necessary data structures “views” need by the CAE tools.
- Compatible to “Europractice” CAE tools distribution.
- CERN could provide:
  - Training courses
  - Maintenance through CERN
  - Technical Support

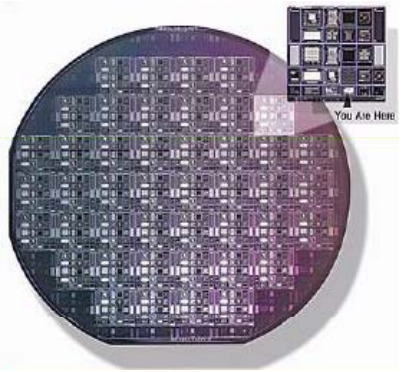
Design Kit Distribution

- Acquiring the IBM PDK and/or the Digital Design Kit
  - Contact Bert.Van.Koningsveld@cern.ch
    or Kostas.Kloukinas@cern.ch
  - You will be given an account on CERN's LXPLUS.
  - You will be able to "sftp" the Design Kit.

- Users Support
  - Limited to the distributed Design Kit version, running under the supported versions of the CAE design tools.
  - Distribution of:
    - Design Flow patches for bug fixes.
    - Technology file updates for DRC verification.
    - Updates to accommodate for foundry and IP vendor newer releases as well as CAE tools upgrades.
  - SUN SOLARIS platform only will be supported (no Linux, sorry!).

Foundry Services

Access to Foundry Services



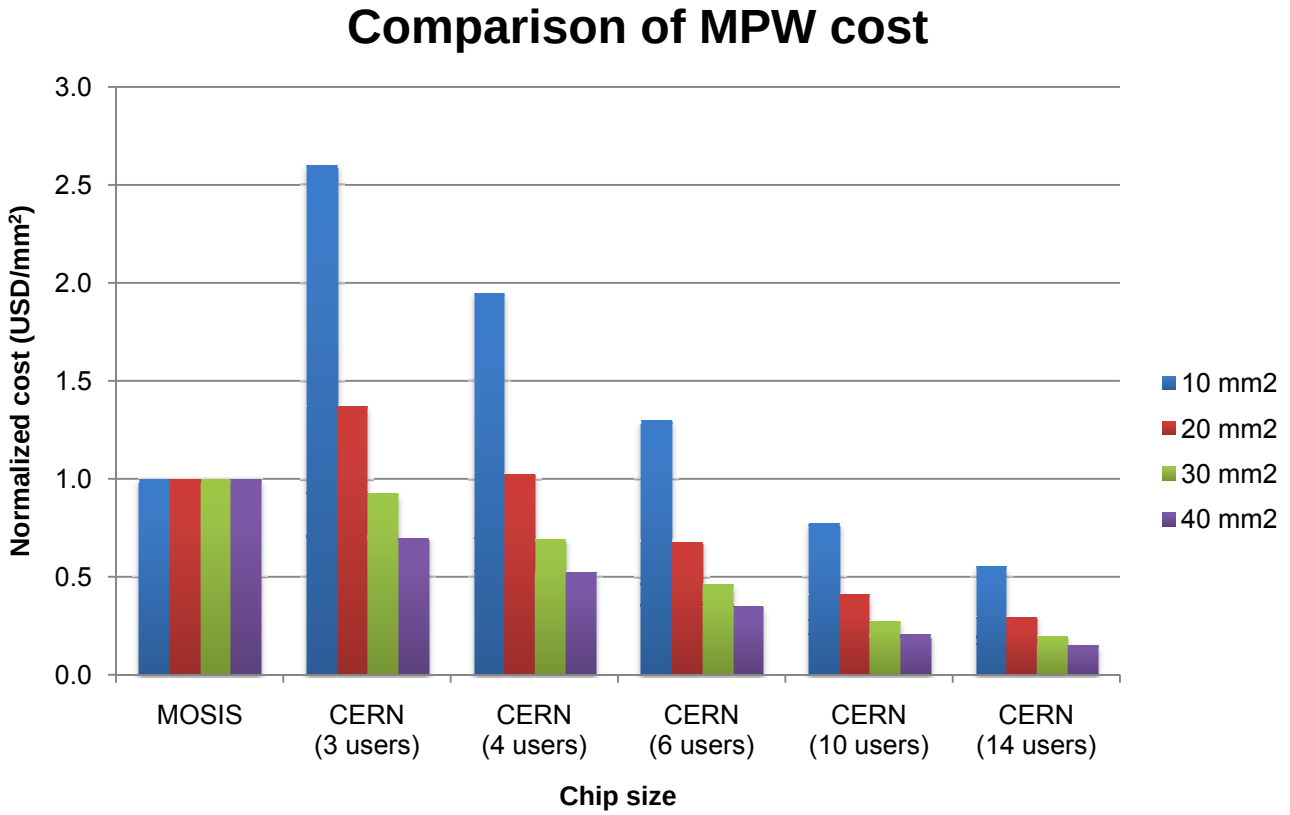
- Technologies:
  - IBM CMOS6SF (0.25μm), legacy designs
  - IBM CMOS8RF (130nm), mainstream process
  - IBM CMOS8WL & 8HP (SiGe 130nm)
  - IBM CMOS9SF (90nm), option for high performance designs

- MPW services:
  - CERN offers to organize MPW runs to help in keeping low the cost of fabricating prototypes and of small-volume production by enabling multiple participants to share production overhead costs
  - CERN has developed working relationships with MPW provider MOSIS as an alternate means to access silicon for prototyping.

CERN MPW run details

- CMOS8-RF process including:
  - poly and diff resistors
  - triple well
  - Low-Vt N and PMOS
  - Zero-Vt NMOS
  - e-fuses
  - Thick (5.2 nm) transistors for IO @ 2.5 V
- 6 metals with LM upper stack, all Cu
  - Vertical metal to metal cap: 1.3 fF/um^2
  - 8 metals possible for private runs (+ 70K$)
- C4 bonding if desired (run split possible).
- Hundreds (or thousands!) of chips from proto run.
- Preferred chips sizes: multiple of 2x2 mm^2.
- Cost below MOSIS at about 80-90 mm^2.

130nm MPW Pricing

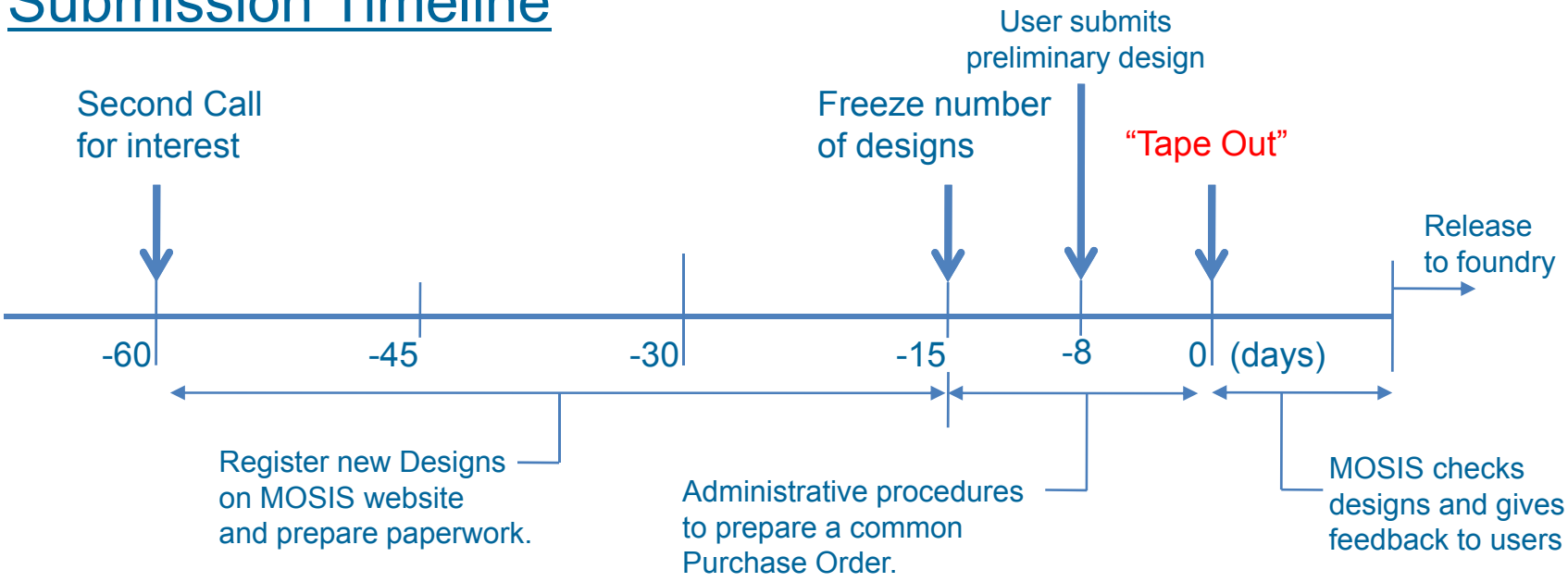


- At present the level of demand is below threshold for CERN-organized MPW
  - Last MPW had 3 users sharing 20 mm^2 silicon area. (Submitted to MOSIS for fabrication.)

Fabricating through MOSIS

- Our alternate path for prototyping

Submission Timeline



- Turn Around Time: ~70 calendar days from release to foundry
- Number of prototypes: 40 pieces

Fabrication Through MOSIS

MOSIS MPW Fabrication Schedule (indicative*)

	2008		2009											
	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
CMOS8RF-DM[1]	17		20		16		11		20		21		9	
BiCMOS8WL				23			18			24			16	
BiCMOS8HP		8			16			22			28			14
CMOS9LP/RF				23				22				26		

(*) as published on the MOSIS web site: http://www.mosis.com/ibm/ibm_schedule.html
([1]) 8RF-LM 0.13 µm designs can be added to 8RF-DM runs with sufficient advance notice

- Early scheduling is essential for cost effective prototyping.
- Communicate your submission plans with: Kostas.Kloukinas@cern.ch
- *There are some advantages to submit to MOSIS via CERN.*

Wrap-Up

- Centralized foundry services.
  - Provide access to advanced technologies by sharing expenses.
  - Provide standardized common design flows.
  - Provide access to shared tools and common IP blocks.
  - Organize common Training and Information sessions.
- Availability of foundry and technology services is modulated by user's demand.
- Your feedback is welcomed. Please contact:
  - Organizational issues, contracts etc.:
    - Alessandro.Marchioro@cern.ch
  - Technology specific:
    - Kostas.Kloukinas@cern.ch
  - Access to design kits and installation:
    - Bert.van.Koningsved@cern.ch

THANK YOU

Agenda

- Presentation:
  "Access to ASIC design tools and foundry services at CERN for SLHC"

- Open discussion


CERN

CAE Tools Requirements

Design Tools Required to use the Digital Kit V1.4

Tool	Version
CADENCE DFII	IC5.1.4.1
First Encounter	4.1.USR5
Fire & Ice	SEV_3.2
Prime Time	X-2005.12-SP2
CeltIC	TSI42_USR1
Calibre	2004.3_9
Synopsys DC, PC	2005.09.SP3
CADENCE Incisive Simulator	IUS_5.7


User support is limited to installations using these versions only.

US Export License

- Radiation hardness is required for the SLHC and this technology could be considered as a “military asset” by the US authorities.
  - This could entail restrictions in the process of obtaining an export license from US for those state-of-the-art technologies.
- Delicate negotiations are ongoing with US authorities.
  - Allow HEP labs to access US based technologies.
  - Allow US collaborators to continue working on common HEP projects utilizing those technologies.
- Survey for an alternate, EU based, foundry is ongoing.

Key Technology Features

	8RF-LM	8RF-DM	8WL	8HP	9SF	9LP/RF
Process	130nm	130nm	130nm SiGe	130nm SiGe	90nm	90nm
Vdd (V)	1.2/1.5	1.2/1.5	1.2	1.2	1.0/1.2	1.0/1.2
Pad cell (V)	2.5/3.3	2.5/3.3	2.5/3.3	2.5/3.3	2.5	2.5
Level of Metals	6-8	6-8	6-8	6-8	4-10	4-10
Metalization	Cu	Cu + Al	Cu + Al	Cu + Al	Cu	Cu
Analog Thick Metal	No	Yes	Yes	Yes	No	Yes
Density (Kgates/mm2)	200	200	200	200	400	400
Power (μw/MHz/gate)	0.009	0.009	0.009	0.009	0.006	0.006
Ring Osc. Delays (ps)	27	27	27	27	21	21
Bipolar beta	-	-	230	600	-	-
Bipolar ft (GHz)	-	-	100	200	-	-
MIMcap (fF/μm^2)	n/a	2.05	4.1	1.0	n/a	
VNCAP (fF/μm^2)	n/a	1.3	1.3	n/a	n/a	
Resistors	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. p poly tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum
efuse	yes	yes	yes	yes	yes	yes

Tools Used in Standard Flows

- Design Compiler - dc - dc_shell -tcl
  - Used to convert functional RTL to gates using WLM to size output drivers
- Physical Compiler - pc - psyn_shell
  - Can synthesize RTL and perform placement simultaneously using steiner routes to estimate parasitics instead of WLM.
  - Can perform placement of gate level netlist
  - Can perform placement based optimization
- First Encounter - fe - encounter
  - Used for prototyping digital designs, producing physical information for optimizing logic, complete power-grid realization, and hierarchical controls for partitioning and budgeting, and hierarchical clock tree synthesis.
- Physically Knowledgeable Synthesis - pks - pks_shell
  - Optimizes the critical paths, taking congestion information into account, and uses true global routing to determine interconnect timing.

Manhattan Routing Inc.

Tools Used in Standard Flows

- Nanoroute
  - All-purpose router for top-level and block-level routing
- Qx/Fire & Ice - qx
  - 2.5D extractor based on validated tech files available from major foundries. Outputs RCs in DSPF/SPEF format for timing, signal integrity, power, and reliability sign-off verification
- Celtic
  - SI-aware delay calculator that provides a unified timing solution that accurately accounts for the impact of crosstalk and IR drop on both delay and functionality. CeltIC NDC combines crosstalk analysis from CeltIC signal-integrity analyzer with the delay calculation capabilities of SignalStorm® NDC. Celtic NDC can be used to complement both Cadence and non-Cadence static-timing analysis and place-and-route flows.
- PrimeTime - pt - pt_shell
  - Full-chip, gate-level static timing analysis tool optimized to analyze millions of gates in a short time, allowing multiple analysis runs in a single day
- Calibre
  - Industry standard physical verification tools. DRC/LVS

Manhattan Routing Inc.