A Readout ASIC for CZT Detectors

Lawrence Jones

ASIC Design Group
Science and Technology Facilities Council
Rutherford Appleton Laboratory

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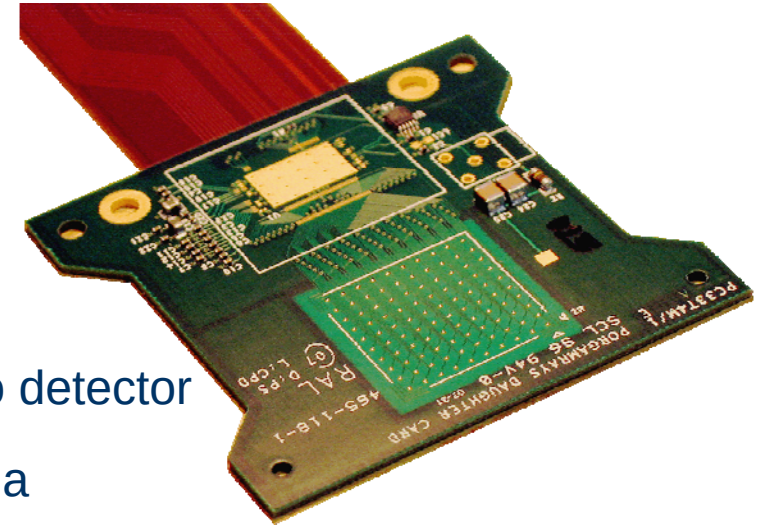
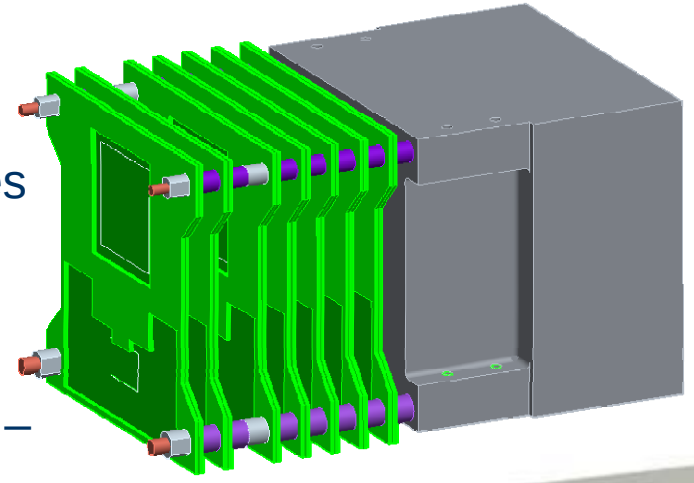
Introduction

- PORGAMRAYS is a collaborative project between the Universities of Manchester and Liverpool, and The Science and Technology Facilities Council (STFC)
- The Project has been jointly funded by EPSRC and the DTI Technology Programme in the UK
- Aim is to develop a demonstrator portable compton gamma camera
- Capable of imaging radiation sources and identifying the isotope
- It will use Cadmium Zinc Telluride (CZT) room temperature semiconductor
- Small size makes it portable and able to operate in hostile environments

The PORGAMRAYS Project

- Compton gamma camera
- 10x10 pixellated CZT
- 100 Channel readout ASIC
- CZT gold stud bonded to a daughter card
- ASIC wire bonded to daughter card and routed to detector
- Several daughter cards form the compton gamma camera
- CZT is 2mm thick
- Signal is formed from fast electrons and slower holes
- Charge collection time is determined by depth of interaction
- Causes variations in amplitude depending on depth – have to correct for this





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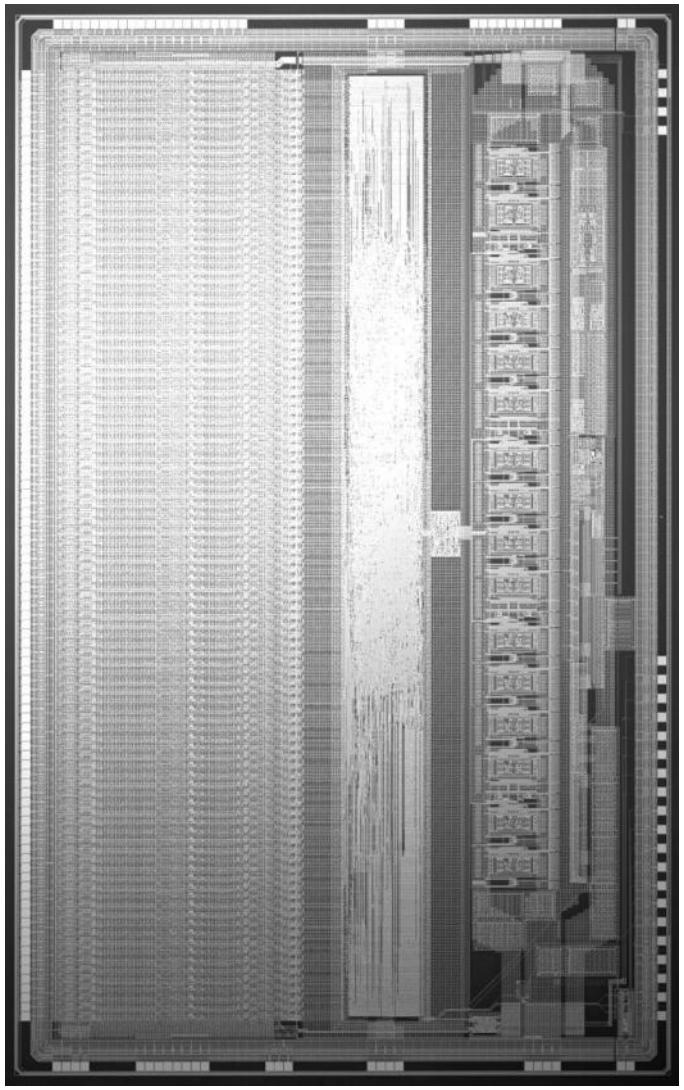
PORGAMRAYS ASIC



Specification

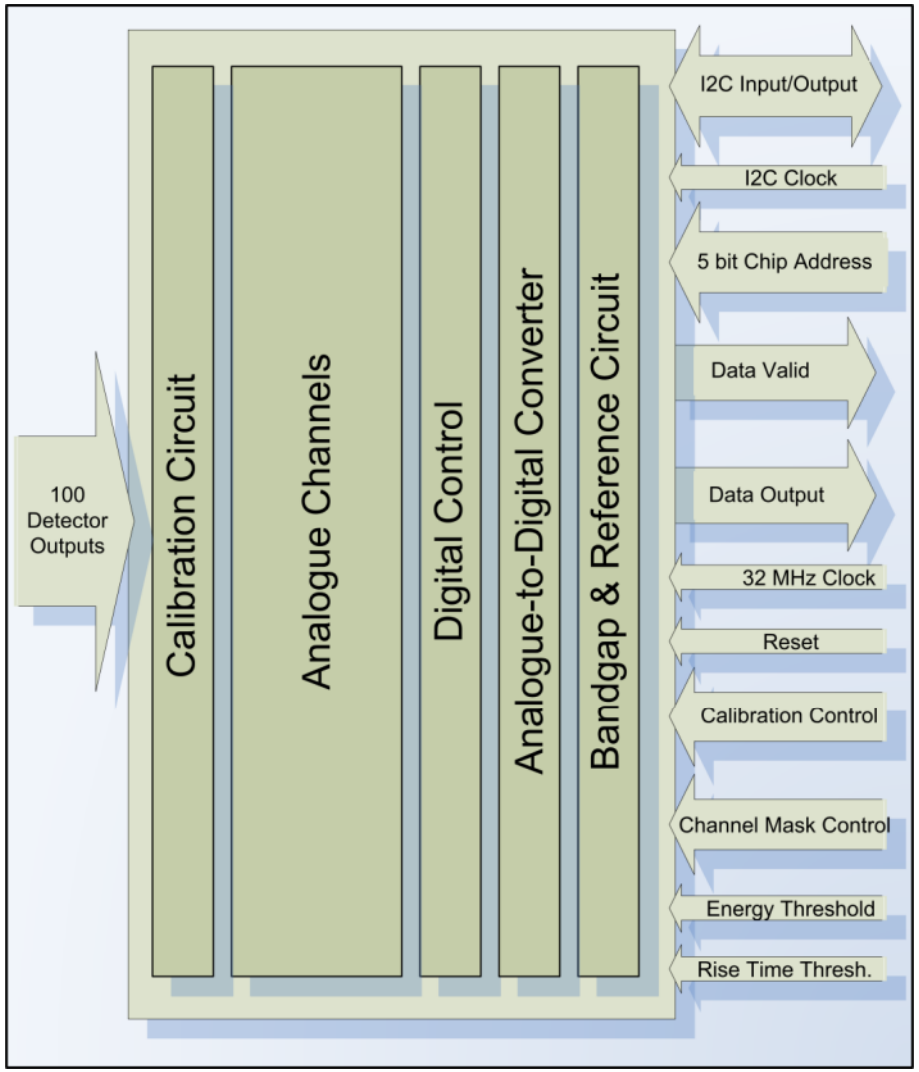
Functional

Power supply: 3.3V
Clock frequency: 32MHz
100 data channels
One further channel for timestamp monitoring
DC input coupling
Leakage current compensation: up to 150nA
Selectable gain - input range: 80k or 400k electrons
Selectable shaping time: 0.5μs to 7.5μs - 4bit resolution
ENC (400k):160e^- rms at 0pF, 210 at 6pF + 13/pF (2μs shaping)
ENC (80k): 120e^- rms at 0pF, 175 at 6pF + 12.5/pF (2μs shaping)
2 Off-chip comparator thresholds
A/D converter: 12 bit pipelined, 1MSample/s
Sparsified data readout
Nearest neighbour readout
Power Consumption: 650mW

Physical

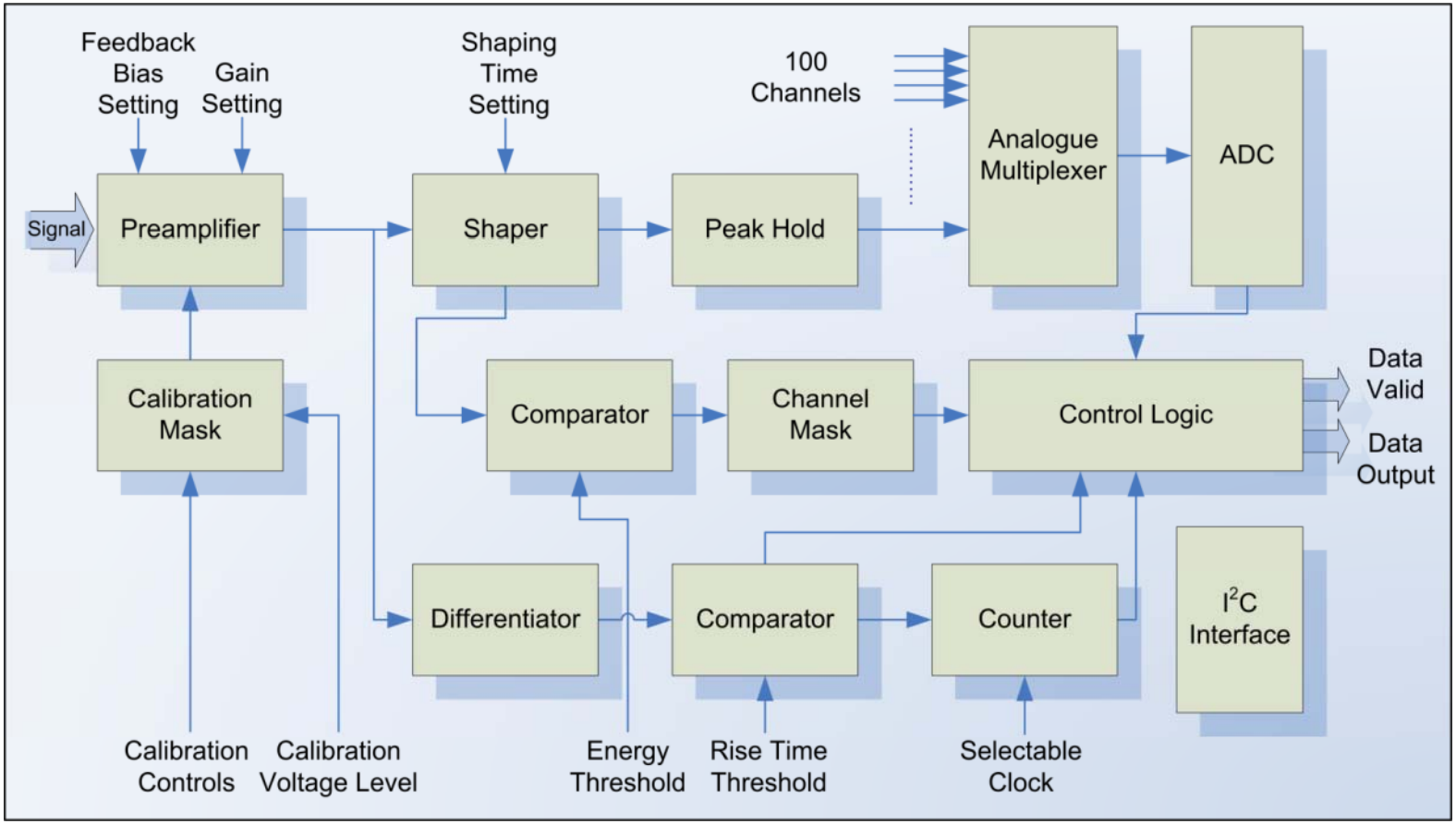
Process: 0.35μm standard N-well CMOS, 2P4M
Size: 6200 x 10200 μm^2
Pad size: 95 x 95 μm^2

PORGAMRAYS ASIC Block Diagram

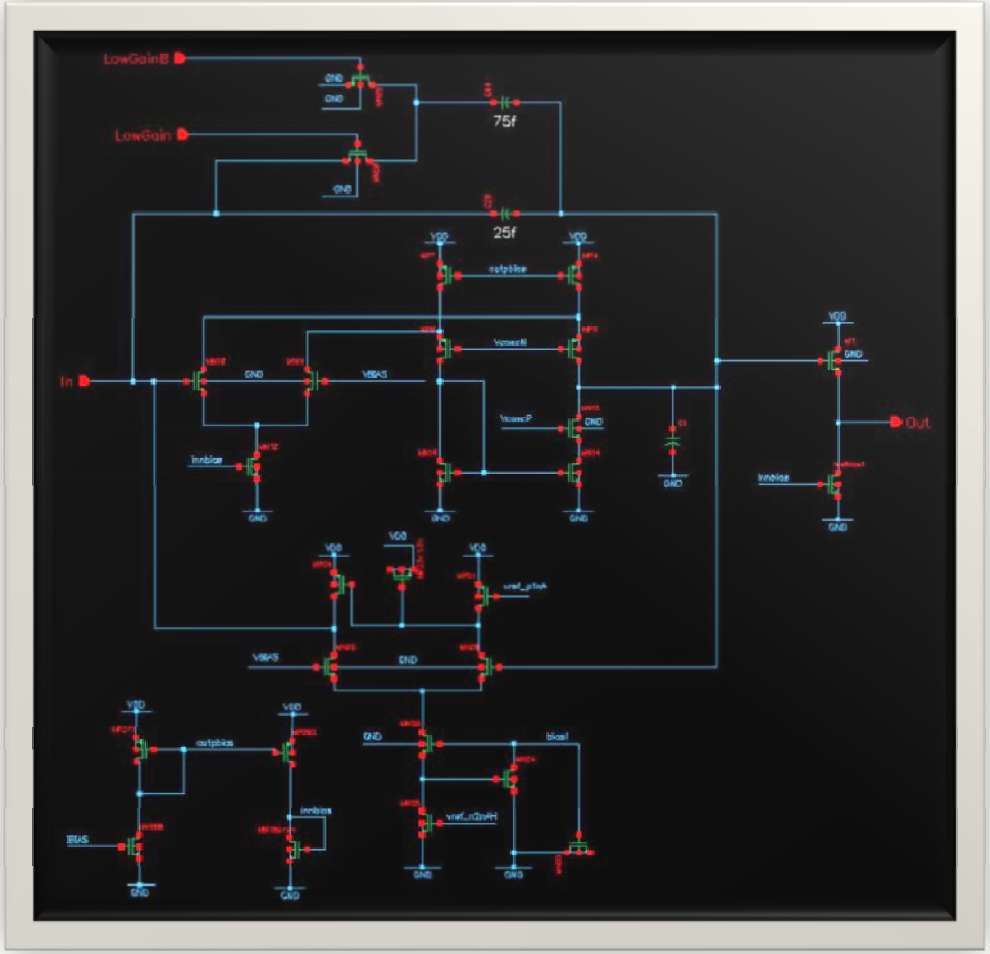


- 100 Channels
- 10x10 pixellated CZT
- Calibration Circuit
- Analogue processing chain
- Digital control
- Data driven readout with nearest neighbours
- 12 bit pipelined ADC
- 32 MHz clock
- Channel Mask
- I^2C interface

Readout Channel Block Diagram

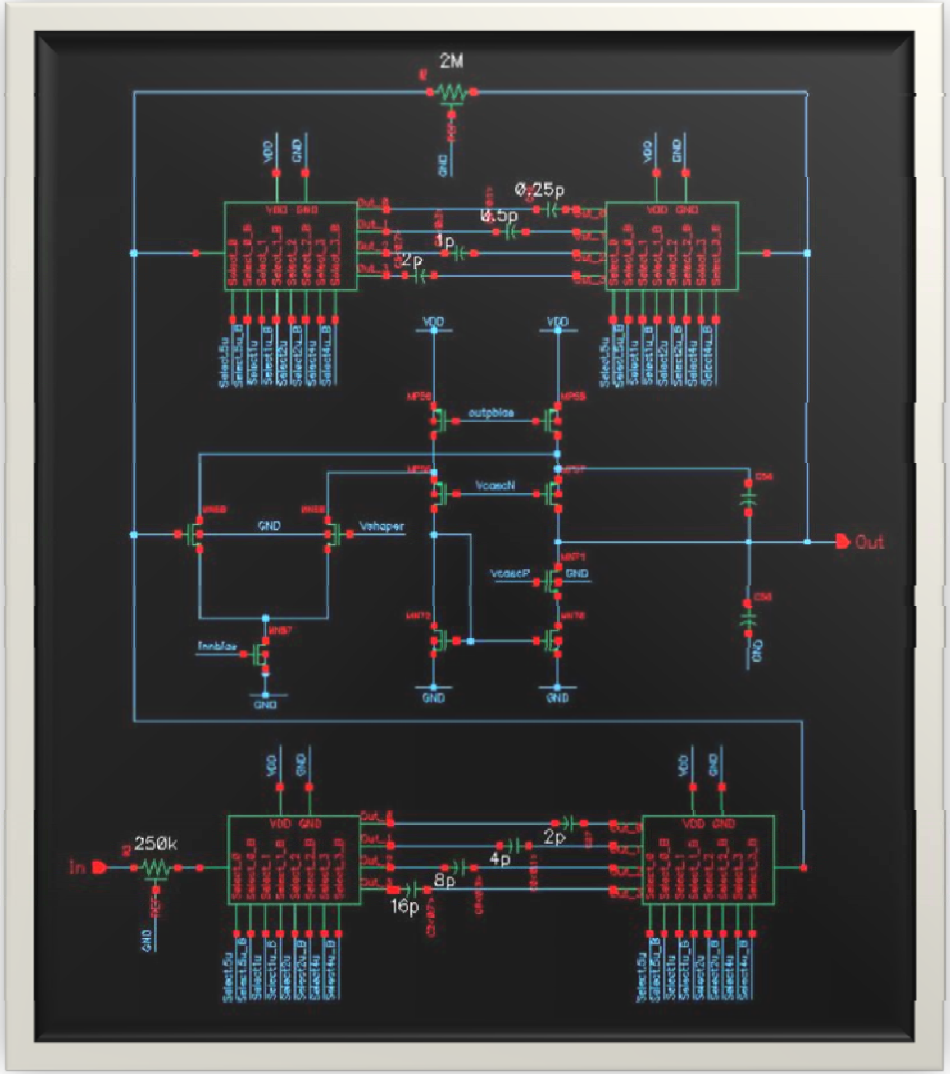


Preamplifier Schematic



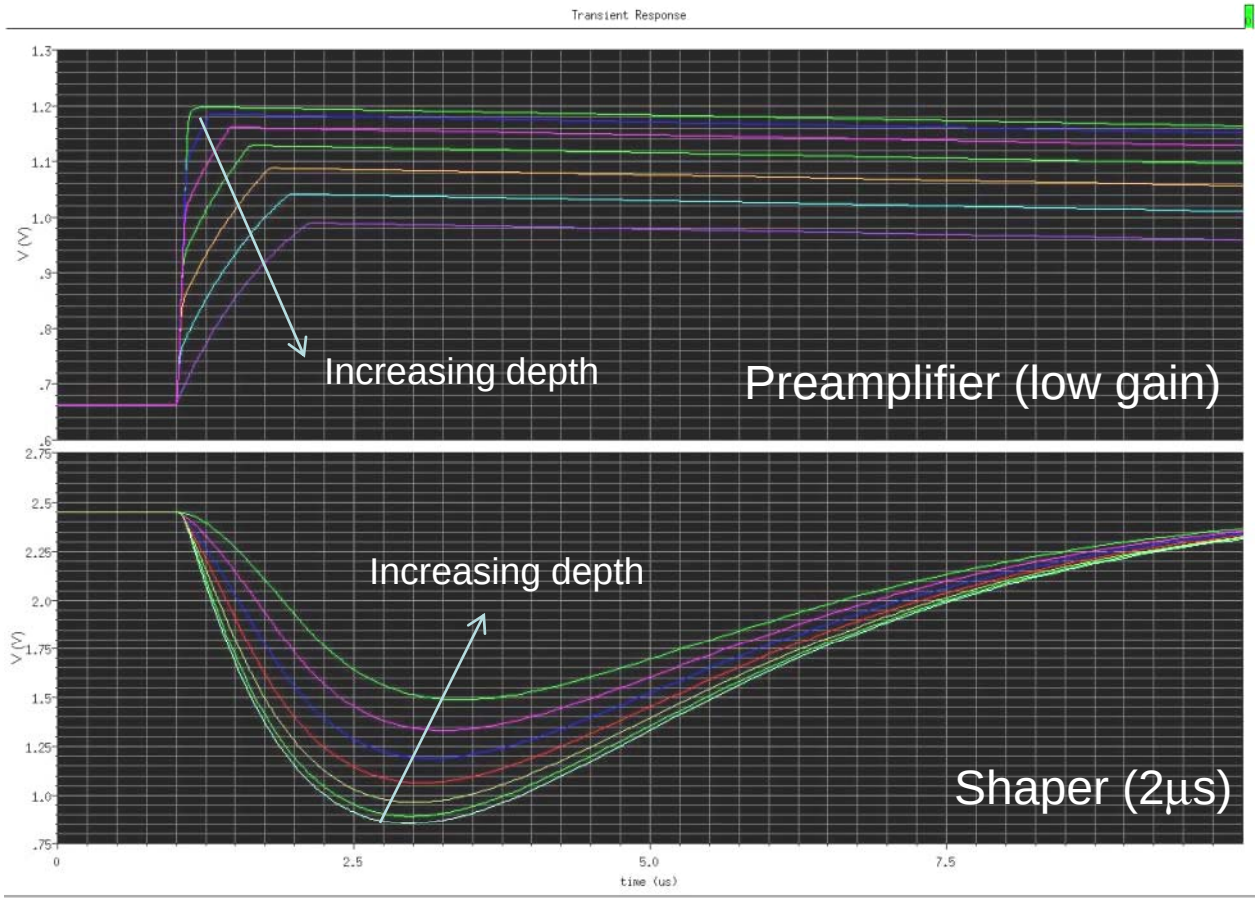
- Differential, folded cascode amp
- Selectable feedback capacitor
- 80 000 or 400 000 electrons range
- DC coupled to CZT
- Low frequency feedback
- Compensates up to 150nA leakage current
- ENC 210 electrons for low gain mode with 6pF input capacitance after 2µs filtering (nominal settings)
- ENC 175 electrons for high gain mode with 6pF input capacitance after 2µs filtering (nominal settings)

Noise Filtering



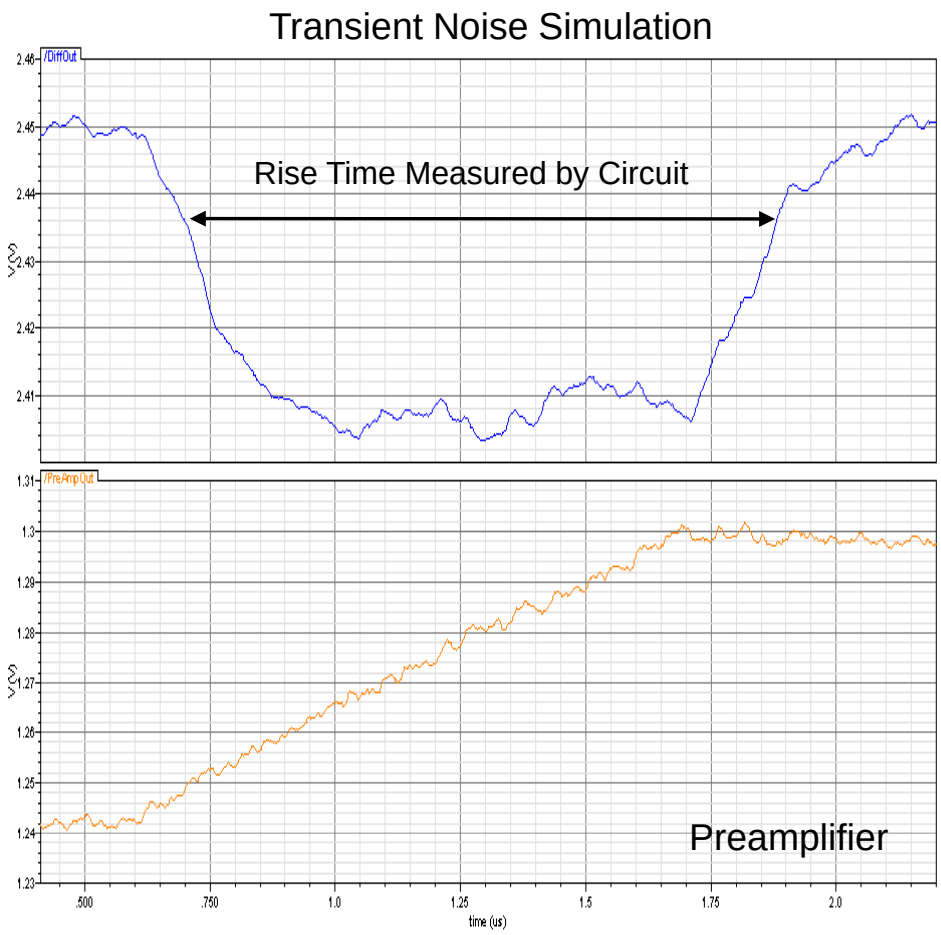
- Differential folded cascode amplifier
- CR-RC band pass filter
- 4 bit programmable shaping time
- Variable 0.5µs – 7.5µs
- Gain of 2.94

Circuit Response to Signal Interaction Depth



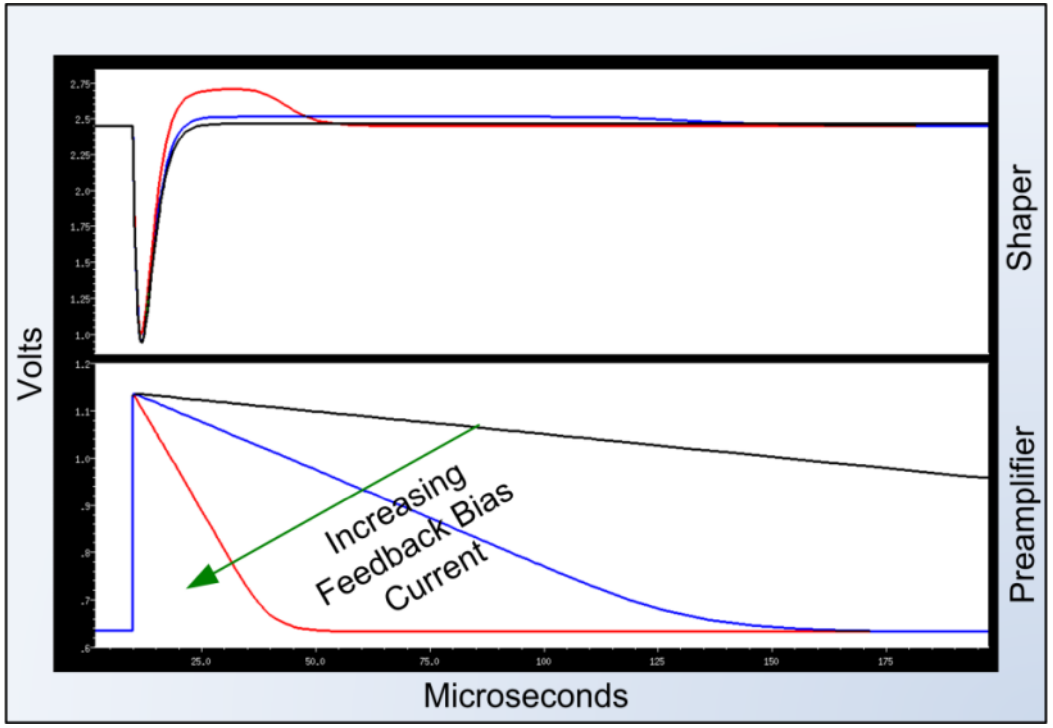
- Low gain mode
- 64 fC signal
- Varying depths within CZT gives varying charge collection times
- Preamplifier rise time 100ns – 1µs
- 2µs shaping time
- Amplitude depends on interaction depth

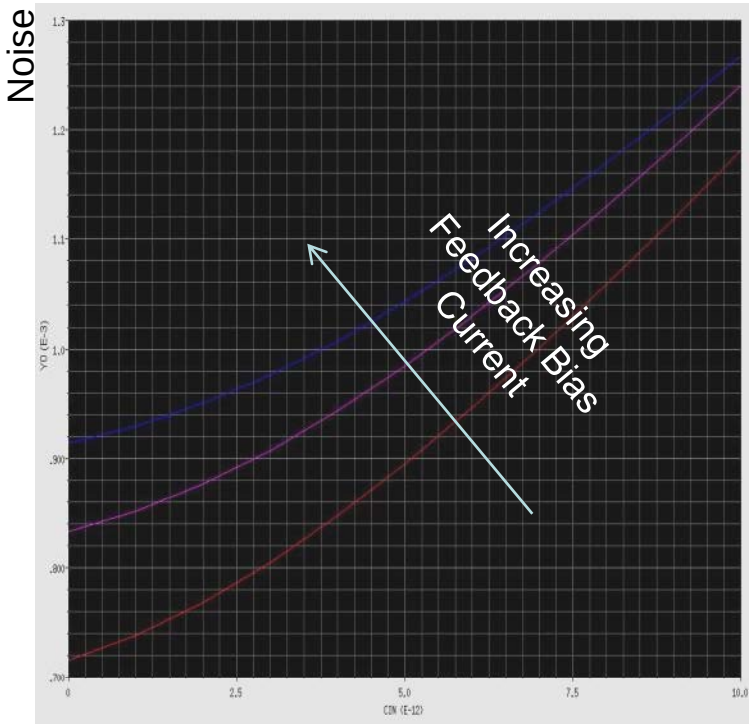
Rise Time Estimation



- Measure rise time can correct for variation in amplitude due to interaction depth
- Differentiate preamplifier output to give pulse proportional to rise time
- Differentiation amplifies the noise
- For longer rise times, pulse height is smaller
- Instead of ideal differentiator use fast CR-RC shaper (32ns)
- Set a threshold and use comparator
- Used to generate timestamp

Noise Dependence on Preamplifier Feedback Bias





- Preamplifier recovery time dependent on preamplifier feedback bias current
- Noise increases with increasing bias current
- Due to a transistor in the feedback circuit

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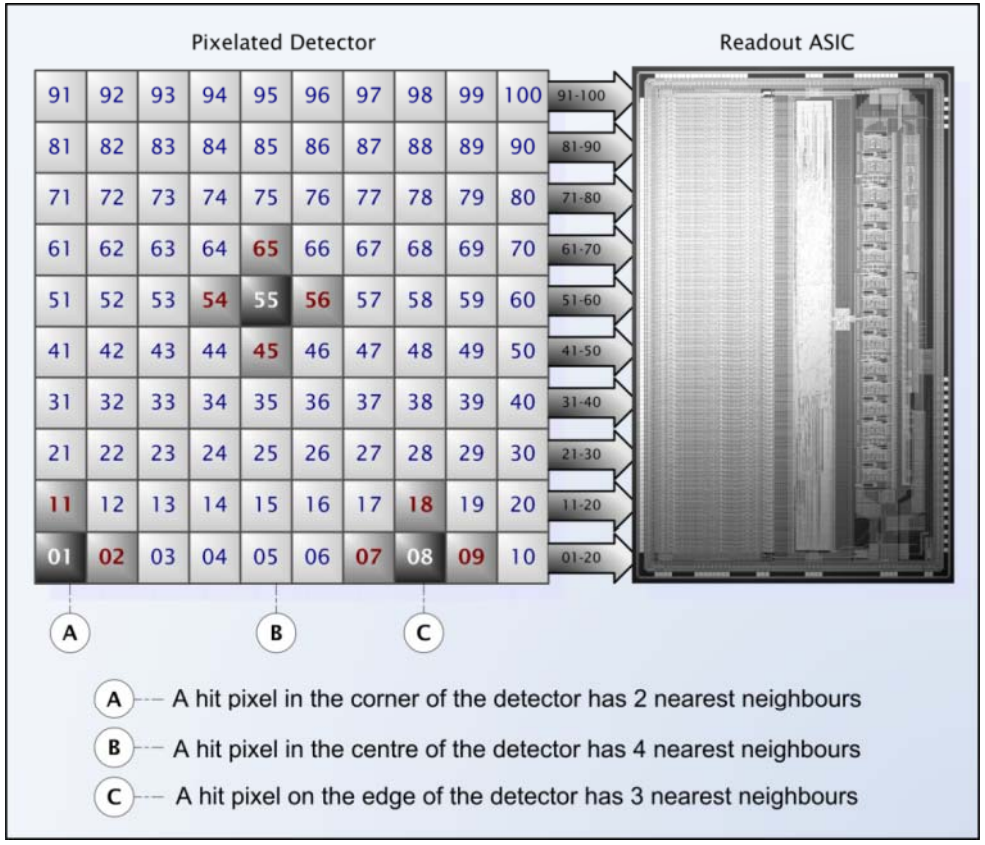
Charge Sharing and Nearest Neighbour Readout

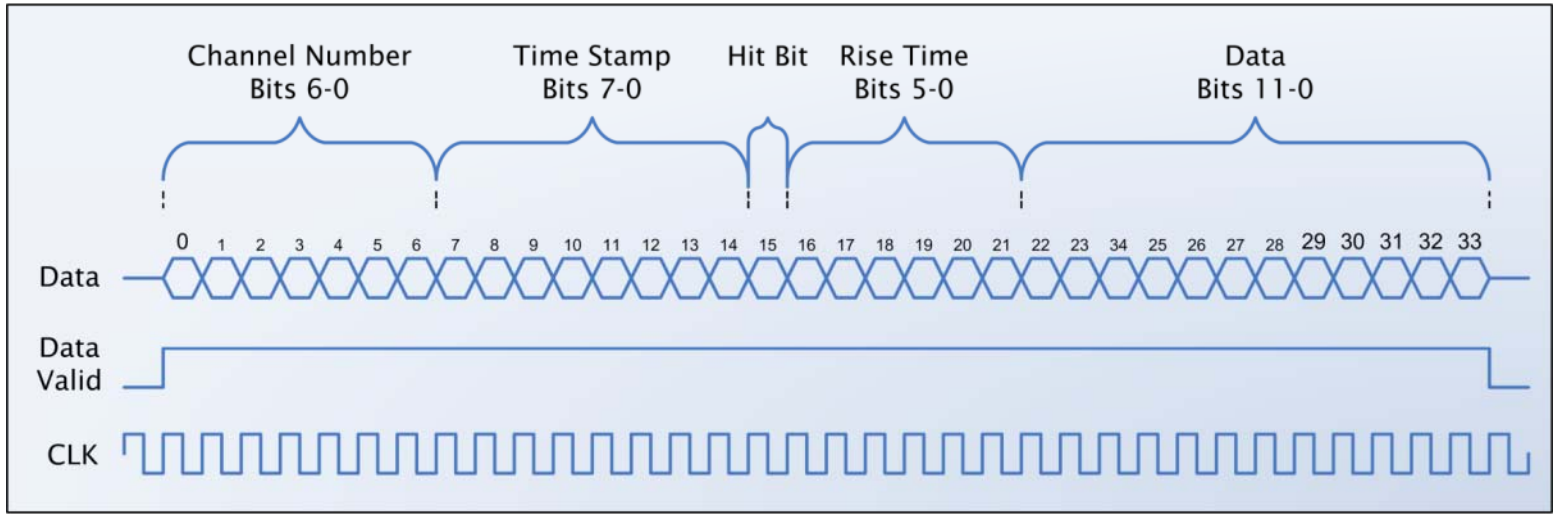


- The charge generated in a CZT detector may be shared between several pixels
- If a pixel is above the readout energy threshold then its nearest neighbours are also read out
- Mapping between pixel number and channel number is shown on the left
- Neighbouring pixels are not necessarily neighbouring channels

Data Sampling and Conversion

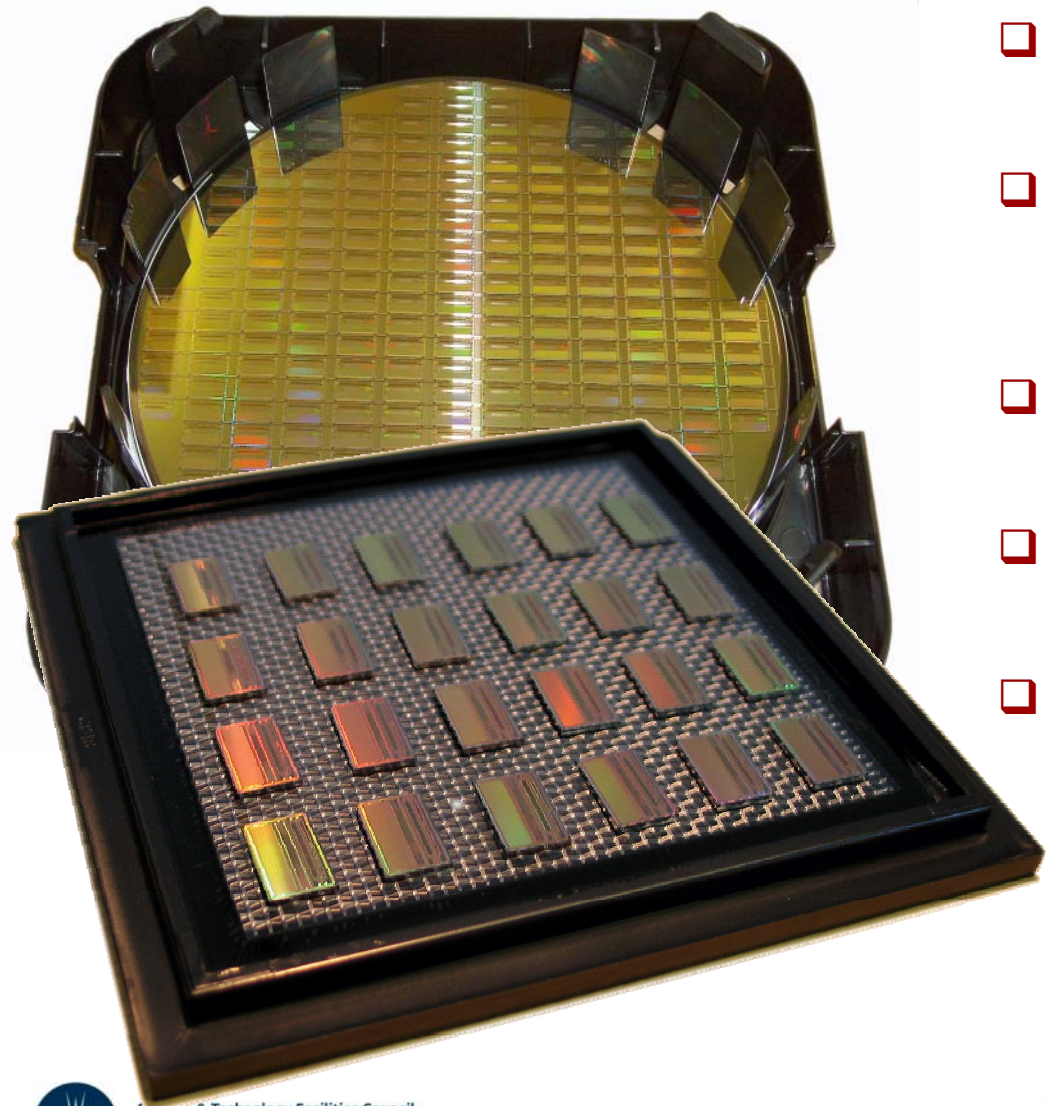
- Shaper output is held using a standard Peak Hold circuit
- If the data is above threshold (a hit) it will be sampled and converted
- The analogue multiplexer runs continuously at the ADC sample rate
- The ADC samples those hit channels
- All channels not hit are skipped
- The ADC is pipelined and converts to 12 bits resolution
- All data (Channel No., Rise Time, Time Stamp and ADC) are synchronised
- A parallel to serial register shifts the data off chip

Output Data Format



- Data driven readout
- DAQ watches for Data Valid signal
- 32 MHz clock
- 34 bits of data synchronised to ADC sample rate (0.94 MHz)
- No need for FIFO
- Time stamp resolution programmable
- Rise time resolution programmable
- Hit Bit = 1 data above energy threshold
- Hit Bit =0 data read as nearest neighbour
- Data can be output continuously with no break Data Valid

Present Status of PORGAMRAYS ASIC



- 2 versions of the ASIC have been manufactured
- 1st version had a problem with the ADC which was fixed for the 2nd version
- 2nd version had 6 wafers manufactured
- Picked one wafer for testing and found a different problem
- Problem not seen in the first version and unrelated to the changes made

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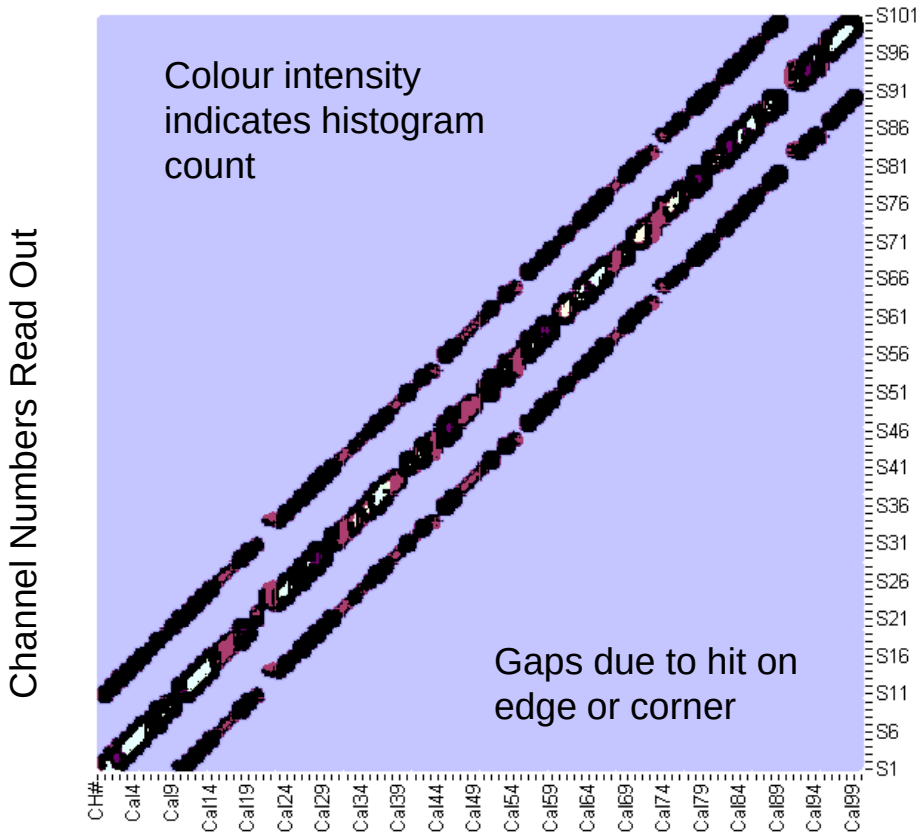
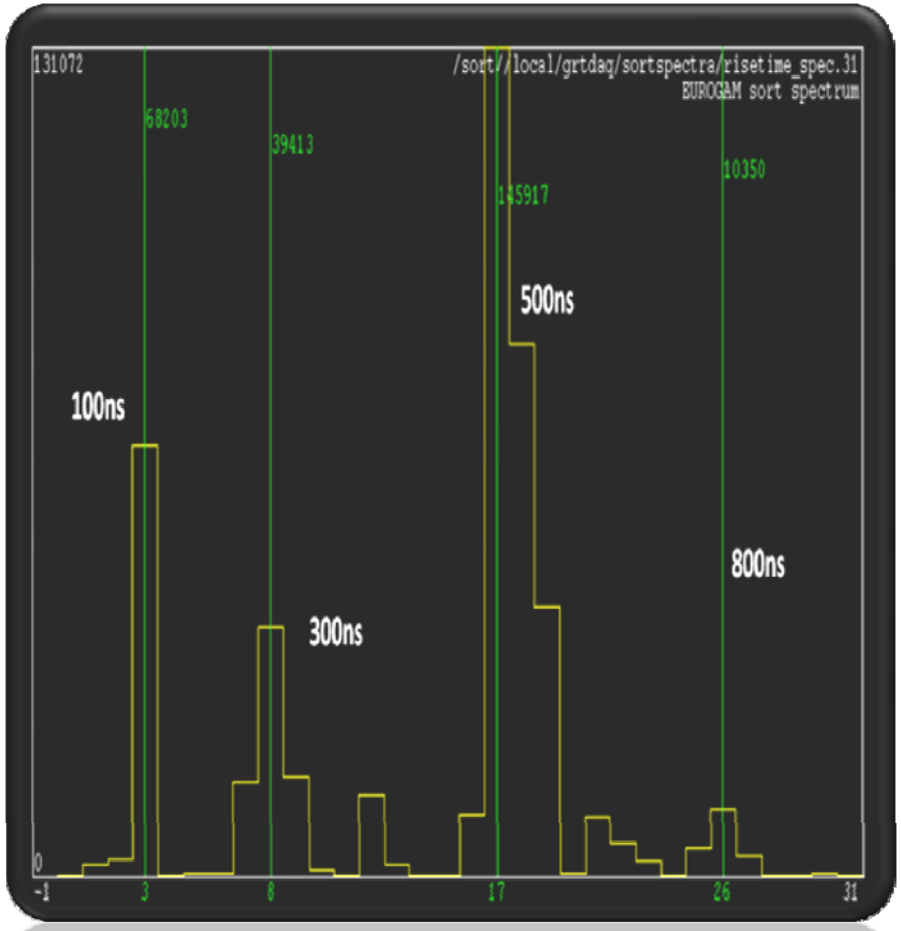
1st Version – Nearest Neighbour Readout



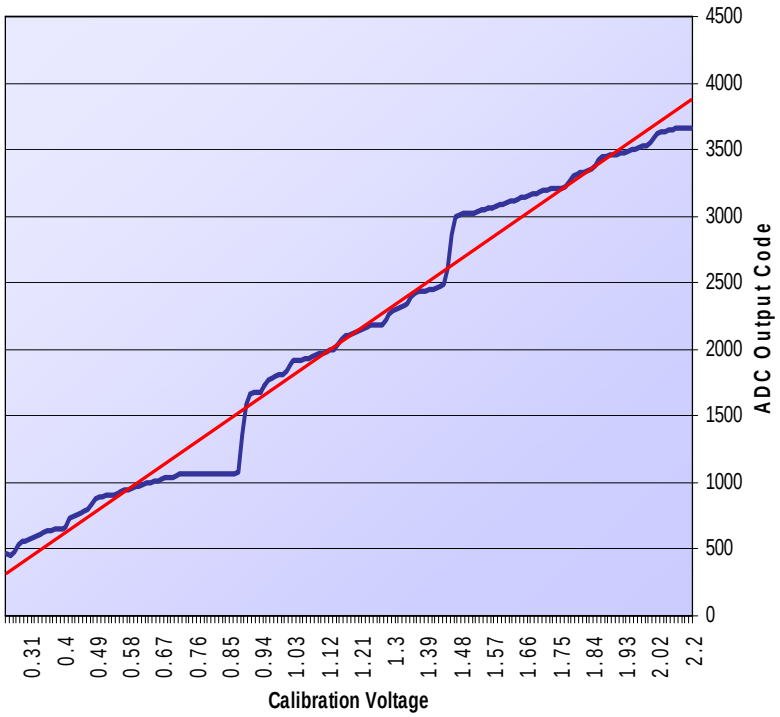
- Test front end sensitivity to the calibrate signal and verify the nearest neighbour readout
- Send a calibrate signal to each of the channels
- Set the amplitude and energy threshold so that a hit occurs in each channel
- Histogram the channel number s that are read out
- Can see from the results that the channels are responding to the calibrate signal
- Nearest neighbour logic is working

1st Version - Rise Time Measurement



- It is possible to send an analogue step voltage through the calibrate circuit
- Vary the rise time to measure the digitised rise time read out by the ASIC
- Histogram results for one channel
- The X-axis is in 32MHz clock cycles = 31.25ns
- 100ns input gives 3 clocks = 94ns
- 300ns input gives 8 clocks = 250ns
- 500ns input gives 17 clocks = 531ns
- 800ns input gives 26 clocks = 812 ns
- Rise time circuit is responsive to input

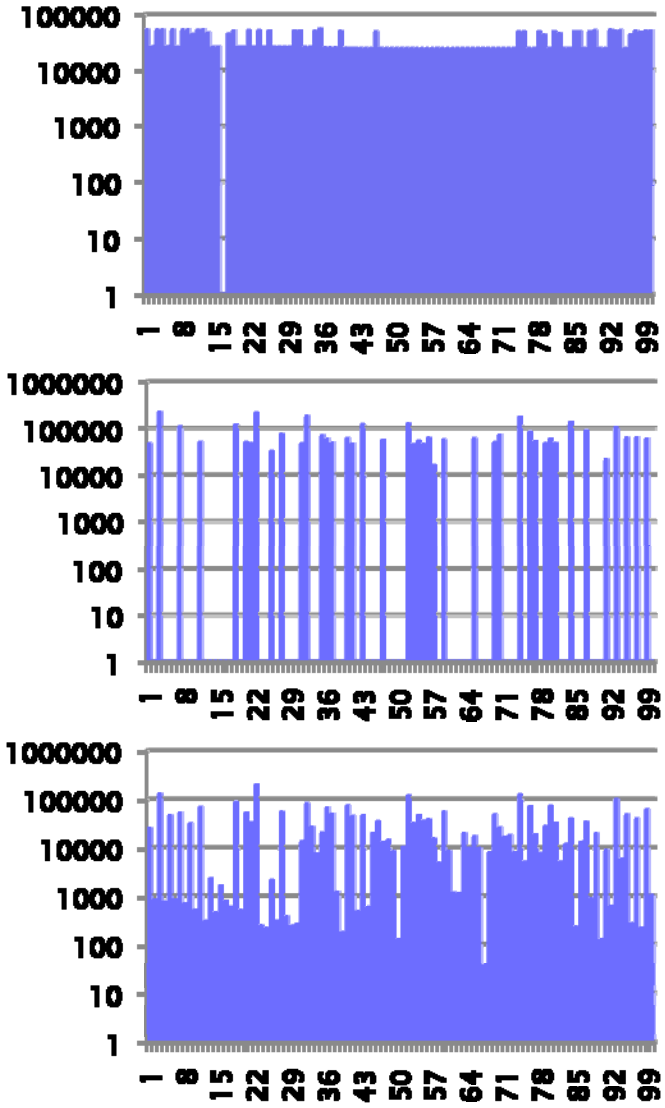
1st Version - Problem with ADC



ADC Output Code to Calibration Voltage

- ADC had large blocks of missing codes
- Traced to two missing logic delay cells
- Had been optimised out during synthesis
- Caused timing errors in sampling of data within the pipeline
- Didn't stop testing the functionality of the rest of the ASIC

2nd ASIC Test Results



Old Chip

New Chip

New Chip Cooled

- Had 6 Wafers manufactured
- Chose 1 to be diced and tested
- Histogram number of hits on each channel
- Shows missing channels
- Compared to 1st version there are lots of missing channels
- Chip was cooled
- More channels appeared
- Number of missing channels is sensitive to temperature

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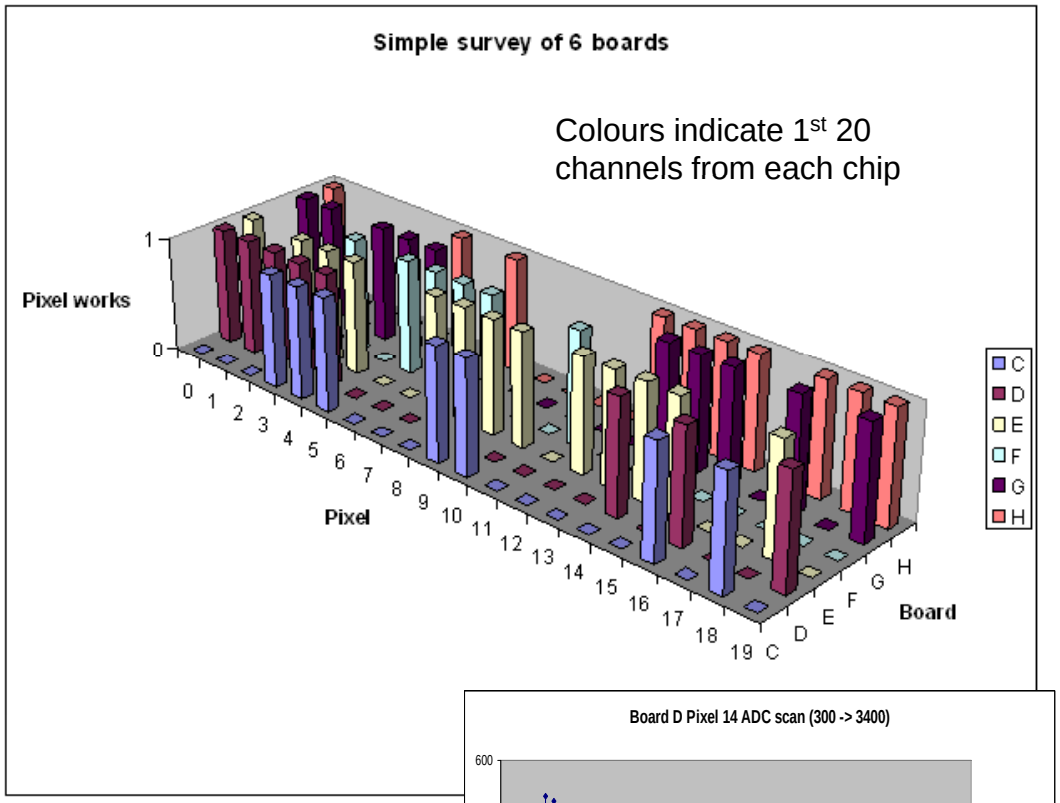
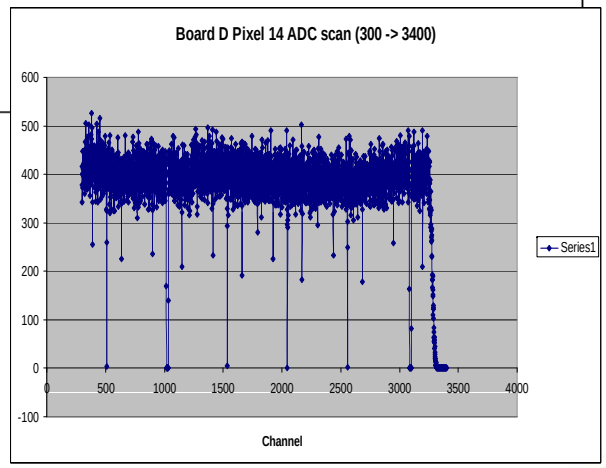
2nd ASIC test results





- Survey of 6 chips
- First 20 channels
- Missing channels appear random
- Suspect a manufacturing problem rather than design fault
- Histogram data from one channel over the full ADC range
- New ADC is a great improvement over the 1st version
- Still a few missing codes

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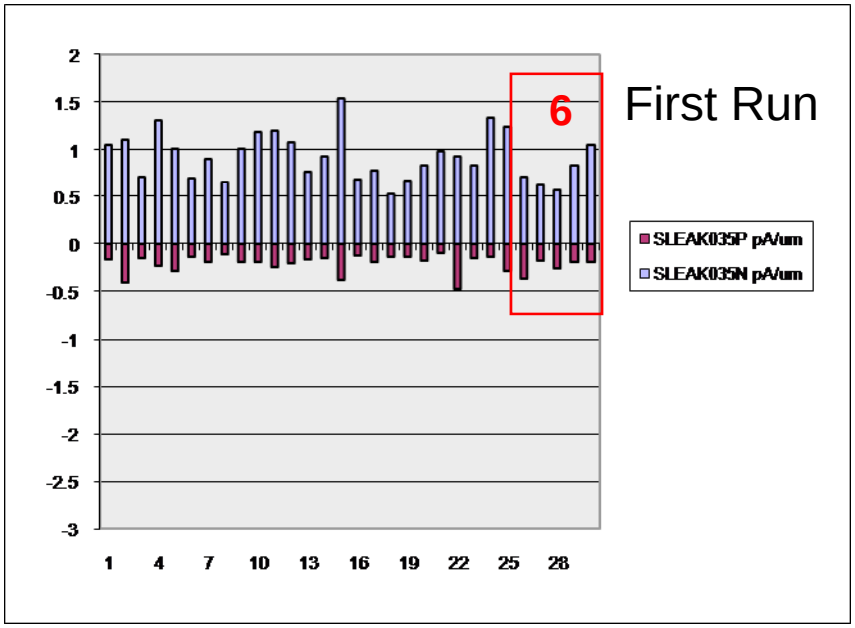
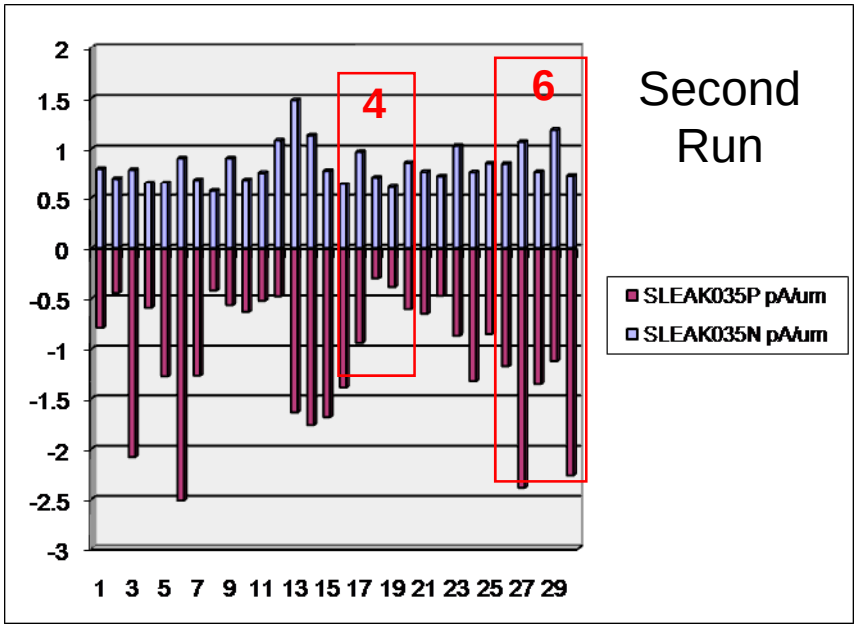
Sensitive to Subthreshold Leakage Current



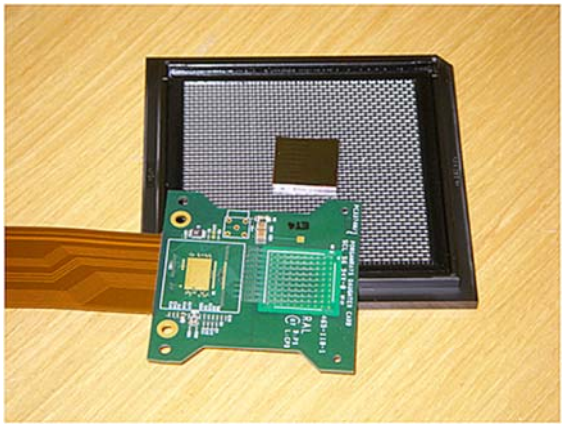
Wafer 6 Diced and Tested



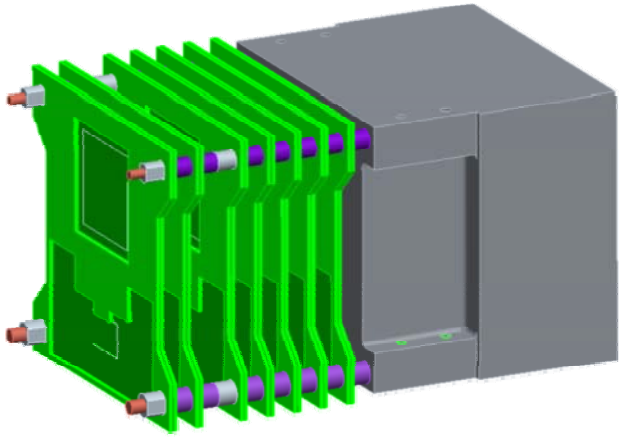
Wafer 6 Diced and Tested

- Subthreshold leakage current for PFETs is consistently low in first run
- Subthreshold leakage current in PFETs is variable and a higher in second run
- Unfortunately our preamp design seems to be more sensitive to this than simulations predicted
- Wafer 4 has been sent for dicing and will be tested

Future Plans



Daughter card and CZT



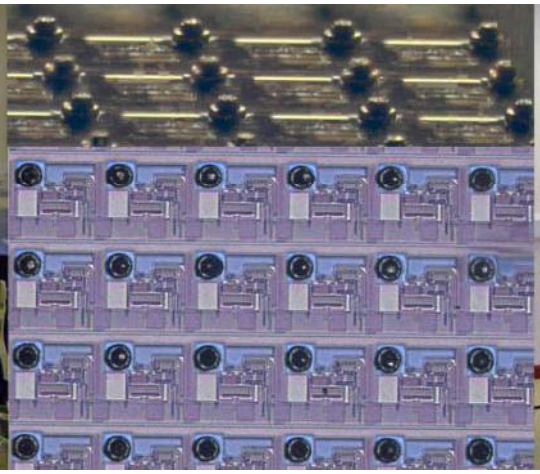
Daughter cards in gamma camera

- To get wafer 4 from the second run diced and tested
- If the chips are found to work then the CZT detectors will be gold stud bonded onto the daughter cards
- It will then be possible to mount the daughter cards in the full gamma camera system
- If the chips are still found to have a problem there is a backup plan involving a different ASIC (Nucam *)

* Nucam: A 128 Channel Integrated Circuit with Pulse-Height and Rise-Time Measurement on Each Channel Including on-Chip 12bit ADC for High-Z X-Ray Detectors. Seller P; Hardie A.L; Jones L.L; Boston A.J; Rigby, S.V. Nuclear Science Symposium Conference Record, 2006. IEEE Volume 6, Issue Oct. 29 2006-Nov. 1 2006 3786 – 3789.

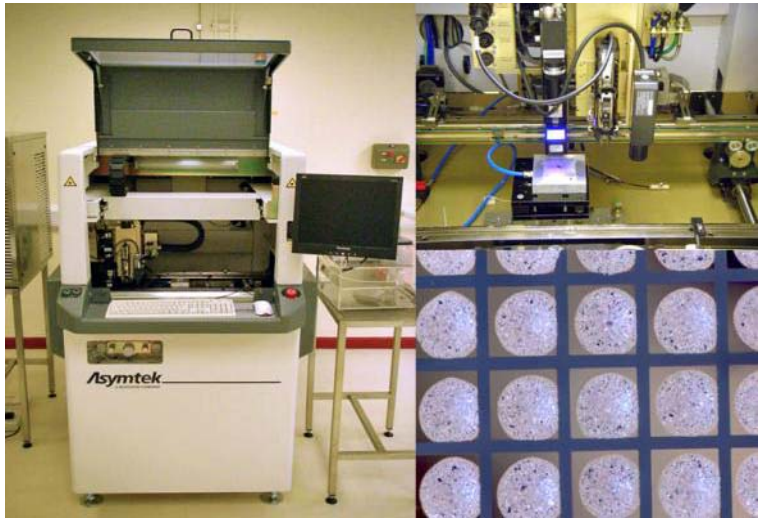
Gold Stud Bonding

Wire bonder

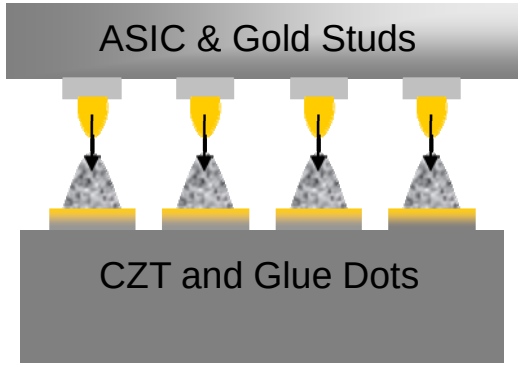


Gold studs

Flip chip bonder



Conductive glue dot dispenser



Flip chip gold stud bonding

Thanks for Listening

Thanks to Ian Lazarus, Paul Seller, Patrick Coleman-Smith

Contact Details

Lawrence Jones
IC Design Engineer, ASIC Design Group

Science and Technology Facilities Council
Rutherford Appleton Laboratory, Harwell Science and Innovation Campus,
Didcot, OX11 0QX United Kingdom

Tel +44(0)1235 446508 Fax +44(0)1235 445008
Email: l.l.jones@stfc.ac.uk

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