A Readout ASIC for CZT Detectors

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Abstract

Spectrometers that can identify the energy of gamma radiation and determine the source isotope have until recently used low temperature semiconductors. These require cooling which makes their portability difficult. The material Cadmium Zinc Telluride (CZT) is now available which operates at room temperature and can be used to measure the energy of gamma radiation. In a compton camera configuration the direction of the radiation can also be determined. A read-out ASIC has been developed for such a system and features 100 channels of electronics, each with a charge amplifier, CR-RC shaper, and peak-hold. A 12 bit ADC converts the data which is sparsified before being read out. The energy, signal rise time, and timestamp of any hit channel is read out together with the data from all of its neighbours. The ASIC has a selectable lower dynamic range which could be used for lower energy interactions.

I. THE ASIC

A. Overview

A portable gamma camera has been developed which will be used to detect both the position and isotope of material emitting gamma radiation. As part of this, a layered and pixellated CZT detector has been designed. Battery powered, the detector requires low power and low noise read-out electronics to detect and process the generated charge before it can be developed into an image.

Figure 1 shows a top level representation of the ASIC. The CZT detector is a 10x10 pixellated array which is gold stud bonded to a daughter card. The 100 channel read-out ASIC is wire bonded to the card and is DC connected to the detector via board routing. Within the ASIC are 100 channels of charge read-out and processing electronics (which can be stimulated using a calibration circuit), a 12 bit ADC, digital control logic, and bandgaps and voltage reference circuits. The ASIC is loosely based on the Nucam ASIC, a 128 channel read-out chip for CdTe Detectors [1-2].

Gamma radiation incident on the CZT detector generates charge proportional to the energy deposited. This charge is then read from the detector and processed by the ASIC. For every event above a defined energy level (the threshold is externally adjustable) the ASIC stores the channel number, amplitude, charge collection time, and the event time in digital form. Readout is data driven, and when data becomes available it is transmitted off-chip. Since charge generated within the CZT detector may be shared between several neighbouring pixels, data from these pixels is also read out as part of the same event.

Read-out from the chip through the *Data Output* is 1 bit serial and data driven. When data becomes available, the *Data Valid* signal goes high for the length of time the data is output. The data transfer speed is 32MHz and a data packet consists is 34 bits. Consecutive data packets are output without a break in the Data Valid signal or the Data Output.



Figure 1: Top-level representation of the ASIC

There is no communication between read-out ASICs in the system. Each is wired point-to-point to an FPGA on the mother board. Therefore each ASIC must be addressed separately, and has a 5-bit hardwired address that is used when programming the on-chip control registers via the I²C-type interface. In addition, there is a channel mask register to mask any faulty channels from triggering the read-out logic

B. Electronics

Figure 2 shows a block diagram of the electronic components which make up each channel of the ASIC, together with the on-chip read-out circuitry and control logic.

There are two branches to note. The analogue chain from input to output comprises of: Preamplifier, CR-RC Shaper, Peak-Hold, Analogue Multiplexer, ADC. In addition there is a second branch which comprises of: Differentiator, Comparator, Counter. These two branches will be explained below.



Figure 2: Block Diagram of Electronics

C. Analogue Readout Channel

1) Charge Amplifier

The preamplifier takes the charge generated within the detector and integrates it on a feedback capacitor to give a voltage. The charge to voltage gain is inversely proportional to the size of the feedback capacitor of which there are two sizes available. This is to allow two different input ranges. The largest capacitance gives an input range of approximately 400 000 electrons. The second gives an input range of 80 000 electrons and could be used with lower energy interactions. These two settings are accessed through the I^2C interface.

The preamplifier has a leakage current compensation circuit [3] which can source a current of up to 150nA from the input of the preamplifier to the detector. The circuit also acts as a DC stabilising feedback across the preamplifier and also ensures the output from the preamplifier returns to its zero signal level thus avoiding pile-up saturation.



Figure 3: Effect of Feedback Bias on Preamp & Shaper

The rate at which this returns to zero depends on the bias current supplied to the leakage current compensation circuit (figure 3), and this is selectable from 0.25nA to 4nA using the I^2C interface. This bias current affects the electronic noise of the preamplifier, with the lowest bias setting giving the lowest noise.

2) Shaper

The shaper is used to filter noise, improve two pulse resolution, and provides a convenient voltage pulse shape for processing. The form of shaping is a variable time constant CR-RC which can be programmed via the I^2C interface. There are 4 bits of resolution, allowing shaping times from 0.5µs up to 7.5µs.

The amplitude of the voltage pulse from the shaper is proportional to the energy of the ionising event in the detector. The lowest energy that will be detected by the chip is defined by a comparator which is connected to the shaper output and to an external threshold voltage. When the shaper output voltage exceeds the threshold voltage, a digital signal is generated by the comparator which defines the event as a hit and the signal is processed and read out from the chip.

3) Peak Hold

The peak amplitude of the shaper output needs to be held long enough for the ADC to sample its value - signals arriving from the detectors by their very nature are random and asynchronous, while the ADC runs at a fixed sampling frequency. For this reason the peak value of the shaper voltage needs to be held until the hit has been detected and the ADC has sampled its value.

4) Analogue Multiplexer

Between each channel and the ADC is the analogue multiplexer. This circuit directs the output from the peak hold circuit onto the ADC input for each channel that has detected a hit. It runs continuously (provided there are events to read out) at the same sampling frequency as the ADC.

5) Analogue-to-Digital Converter

The ADC is a 12 bit converter, fully pipelined, and employing a fully differential architecture. It runs at a sample rate of approximately 0.94 MSamples/s. This value comes about due to the fact that the chip outputs a 34 bits frame of data at a clock rate of 32MHz, and the ADC is synchronised to the frame rate, which is 32/34 MHz.

D. Rise Time Measurement

A measure of the depth of interaction of the gamma radiation within the detector can be determined by measuring the charge collection time [4]. This is done by measuring the rise time of the preamplifier output. To achieve this, the preamplifier output is differentiated to give a pulse whose width is proportional to the rise time (figure 4). A comparator then cleans this signal up and is used to gate the clock of a counter to give a digital representation of the rise time.



Figure 4: Rise Time Measurement

By its very nature, differentiating an analogue signal is intrinsically noisy. Therefore, instead of using a standard differentiator circuit, some noise filtering was achieved by using a band-pass filter with very fast time constants. The output of the differentiator comparator was also used to generate a timestamp of when the signal occurred.

E. Digital Control Logic

The digital control logic performs several functions, by far the most complicated part comprises the *Nearest Neighbour Logic*. In addition, there are other functions and these are listed in the following sections.

1) Clock Division

The ASIC has a 32MHz clock input. However several different clock frequencies are required on-chip. The rise time measurement has a selectable 16 or 32MHz. The timestamp has a selectable 1,2,4 or 8MHz clock.

2) Data Synchronisation

The output from the ADC has to be synchronised with the outputs from the timestamp and the rise time circuits before being transmitted off chip. This is done using a bank of flipflops.

3) Data Sparsification

Only data corresponding to hit pixels and their neighbouring pixels are readout. The control logic keeps the analogue data stored on the peak hold circuit until it can be read out through the analogue multiplexer. The multiplexer is synchronised to the ADC sample rate which is 0.94MHz.

4) Time Stamp Verification

If several ASICs are being used in a system it is necessary for them to remain in synchronisation with respect to the time stamp. To ensure this an extra channel (channel 0) has been reserved for time stamp verification. Channel 0 does not connect to any of the detector pixels, but during operation of the ASIC, the calibration circuit is programmed to point to channel 0. A calibration pulse can then be sent to all ASICs and the time stamp read out from all channel 0's can be monitored.

5) Nearest Neighbour Logic

The charge generated by an ionising event within a pixel in the detector may be shared with the neighbouring pixels. This charge may be below the threshold set for registering as a hit and would otherwise be lost. To overcome this, the readout ASIC has been designed with nearest neighbour readout. The mapping of detector pixel to readout channel is shown in figure 5. This is hardwired into the ASIC and cannot be reconfigured.

When a pixel has a signal over threshold (hit), for example pixel 55 in fig. 5, then pixels 45,54,55,56 and 65 will all be read out. A "hit bit" in the data stream from the chip indicates which of the pixels registered the initial hit above threshold.



Figure 5: Mapping of Detector Pixel to Read-out Channel

F. Interface & Control Registers

Using the I^2C type interface it is possible to access the onchip registers and to modify their default settings. There are two registers, and each register can be written to or read from via the interface. Table 1 shows the functions controlled by the two registers

Table 1. Control Registers								
REGISTER 1								
Bit	7	6	5	4	3	2	1	0
	Preamp Gain	Shaping Time				Leakage Comp. Bias		
REGISTER 2								
Bit	7	6	5	4	3	2	1	0
	Rise Time	Time Stamp		Chip Bias Current				

G. Data Output Format

When data becomes available it will be immediately output from the chip, via a single serial output (LVDS). A data frame is 34 bits in length (figure 6) and contains the channel address (7 bits), the time stamp (8 bits) a hit bit (1bit), the rise time measurement (6 bits) and the amplitude measurement (12 bits).

The channel address can range from 0 to 100, with channels 1 to 100 being the detector channels, and channel 0 used for time stamp verification. The hit bit identifies the event as occurring in that channel, in which case it is set high. If set low, the hit bit indicates the channel to be one neighbouring that in which the event occurred.



Figure 6: Output Data Format

II. READOUT SYSTEM

As mentioned previously, the CZT detector is gold stud bonded onto a daughter card (figure 7) and the readout ASIC wire bonded to the daughter card.

Several daughter cards then connect to a mother board via flexible connectors. The mother board contains the FPGA used to control the ASICS and for data acquisition. Several daughter cards a aligned to form a compton camera.



Figure 7: Daughter Card

III. STATUS

The present status of this project is that two versions of the ASIC have been fabricated on a standard 4-metal 0.35μ m process (figure 8). The first version has been extensively tested. However, due to an error in the ADC which caused large blocks of missing code, the ASIC can not be used in a full compton camera system to image gamma radiation. However, all other functions of the ASIC were found to be operating.



Figure 8: Fabricated ASIC



Figure 9: Test of Nearest Neighbour Read-out

Figure 9 shows a scan of all channels of the ASIC by applying a calibrate signal to each input in turn and histogramming the channel numbers that appear at the output of the ASIC. It can be seen that for each CAL input there are several channels that are read out This corresponds to the pixel to channel mapping shown in figure 5.



Figure 10: ADC Transfer Curve

Figure 10 shows the transfer characteristic of the 12-bit pipelined ADC on the first version of the chip. The non linearity and blocks of missing code are caused by timing errors within the ADC. The cause of these errors is fully understood and has been corrected on the second version of the ASIC.

IV. CONCLUSIONS

A read-out ASIC for CZT detectors has been fabricated and tested. Tests have confirmed basic functionality but have also revealed problems due to a faulty ADC.

A second iteration has been fabricated and is undergoing testing. Initial tests have confirmed that the fault in the ADC has been corrected.

V. REFERENCES

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