Readout Electronics of the ATLAS Cathode Strip Chambers

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Readout Electronics of the ATLAS CSCs

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Muon Spectrometer precision tracking: Monitored Drift Tubes (MDT)

- MDT safe operation up to 150 Hz/cm²; exceeded for \(|\eta| > 2\)
- CSC considered safe up to 1000 Hz/cm², sufficient up to \(|\eta| = 2.7\)
- Annual neutron flux for CSCs up to \(1.8 \times 10^{12}/\text{cm}^2\) (1 MeV equivalent); total ionizing dose up to 11 Gy/year
The ATLAS Cathode Strip Chambers (II)

- Cover high-rate, high-radiation region in endcaps
- $2.0 < |\eta| < 2.7$
- $1 \text{ m} < r < 2 \text{ m}$
- $|z| \sim 7.5 \text{ m}$
- 16 chambers each side

ATLAS Muon Side C Endcap region during installation
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Measure charge induced on cathode strips.

Interpolate between charge of neighboring strips to determine track position in plane.

Target resolution 60 $\mu$m in precision coordinate.

Small gas volume, use Ar/CO$_2$: no hydrogen, low neutron sensitivity.

Four such layers per chamber: four measured points per track.
### On-Detector Electronics
- High radiation environment
- Avoid complex digital circuits
- Sample, shape, store
- Digitize on demand only
- Read out all strips
- 30720 channels total:
  - 4 layers with (192+48) strips each
  - 960 channels per chamber
  - 16 chambers per endcap

### Off-detector Electronics
- Low radiation environment
- Perform bulk of data processing
- One “Readout Driver” (ROD) handles 2 chambers
- 8 RODs per crate
- RODs fully control frontend readout
- Required bandwidth for readout links 160 Mbyte/s
Drift time 30 ns, shape to bipolar pulse, first peak 70 ns after rising edge.

Sample continuously at 20 MHz: 4 samples cover positive lobe.

Samples pipelined up to 144 deep, sufficient for 2.5 µs trigger latency.

Upon level 1 trigger, digitize and read out 4 consecutive samples.
CSC Readout Electronics Overview

- RCC 1 per endcap
- TIM 1 per endcap
- ROD 8 per endcap
- CRB
- Transition Module
- Chamber
- S-LINK
- Data
- Clock, SCA Control, Etc.
- 160 Mbyte/s capacity
- 105 Mbyte/s
- 16 chambers per endcap
- 8 per endcap
- Custom J5/J6 Backplane 1 per endcap
- 160 Mbyte/s capacity
- 1 per endcap
GPU = Generic Processing Unit (DSP+FPGA module)
13 GPUs per ROD: 1 host (HPU), 12 for data processing (DPUs)
300MHz TI TMS320C62x DSP + 2 Xilinx Spartan FPGAs
### ROD
- Infrastructure for data processing
- Motherboard for 13 GPUs
- Two high bandwidth buses
- Controlled via VME64x backplane
- FPGA based *(Xilinx Spartan/Virtex2)*

### GPU
- Data processing (in various roles)  
  *Sparsification, cluster identification, fragment building, neutron rejection*
- Mezzanine board with DSP  
  *(300 MHz TI TMS320C6203)*
- DSP programmable in C++
- Interface to ROD buses via FPGAs  
  *(Xilinx Spartan2)*

### CTM
- I/O (frontend, trigger, DAQ)
- Connects to trigger/timing system via custom backplane
- Controls frontend electronics
- Duplex fiber optic connections to frontend
- GLink protocol implemented in FPGAs  
  *(Xilinx Virtex2 w/RocketIO)*
- Fiber optic connection to DAQ via mezz card *(‘HOLA’ SLink, ATLAS standard)*
ROD Software (I): DSP Roles

**HPU**
- Orchestrates SPUs, RPUs, DX
- Attaches trigger info to event
- Asserts RODBUSY if necessary

**SPUs**
- Verify frontend data integrity
- Remove noise (subtract pedestals)
- Apply timing cuts
- Identify clusters

**RPUs**
- Assemble SPU fragments
- Remove non-track hits
- Provide event length to HPU
ROD Software (II): HPU Tasks

- **time critical**
  - Retrieve and buffer trigger information
  - Transfer events from SPU to RPU
  - Poll RPU for * events ready * their length
  - Assemble event and send to ROL

- **low priority**
  - Check ROD sub-systems status
  - Check SPU status
  - Perform monitoring tasks
  - Check for pending commands

- Optional
- Low priority
- Time critical

DSP software written in C++, time critical parts in assembly language

Supporting firmware written in Verilog

Important to maintain continuous pipeline flow, **queue everything, no waiting**

HPU main loop over critical tasks needs to be very fast (10 \( \mu s \))

Cycle-heavy parts of data processing parallelized (SPUs)
CSC Commissioning Status (I)

- All hardware installed, connected, and operational.
- Debugging of ROD software/firmware was substantially delayed; several factors involved, expert personnel thinly spread.
- Still tackling stability and rate problems at this point.
- Some infrastructure problems on the way only made things worse.
VME power supply oscillation

- Under certain load conditions, 3.3V and 5V voltage oscillates.
- Eventually leads to PS shutting itself down.
- Can only run max. 3 RODs per crate (need 8).
- Manufacturer now provides fix.

`jumper selectable regulation circuit time constant`

- These are detached water-cooled PS, attached to rear rack door. Problem not observed with standard PS integrated in bin.
- Connection to VME crate via \( \sim 1 \text{ m long cables} \).
- Apparently the extra cable length, together with load pattern, affects voltage regulation.
VME power supply malfunction

- Damaged control cable leads to internal fuse blowing in power supply
- This in turn must have resulted in surge on VME SYSRESET line (!)
- Fatally damaged VME buffer ICs on 8 RODs, 2 SBCs
  
  *one ROD with two blown traces!*

- Fortunately, replacing the ICs (and jumpering the traces) was sufficient to put RODs back in service.
Conclusions

- Muon tracking in the forward region of ATLAS is performed by cathode strip chambers.
- On-chamber readout electronics are kept as simple as is practical.
- Noise reduction measures are entirely performed off-detector.

- Off-detector electronics use DSPs for noise reduction and event building.
- Status: hardware installed, firmware/ software still being debugged.