Readout Electronics of the ATLAS Muon Cathode Strip Chambers

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Abstract

The ATLAS muon spectrometer employs cathode strip chambers (CSC) to measure high momentum muons in the forward regions ($2.0 < |\eta| < 2.7$). Due to the severe radiation levels expected in this environment, the on-detector electronics are limited to amplifying and digitizing the signal while sparsification, event building and other tasks are performed off-detector.

I. INTRODUCTION

The CSC system is designed to measure high momentum muons in the forward regions (pseudo-rapidity $2.0 < |\eta| < 2.7$) of the ATLAS detector [1]. Its principle of measurement is to determine the hit coordinates by interpolating charge deposited on adjacent strips. Multiple layers of strips allow for tracks to be formed from these hits. At an expected strip hit rate of up to 600 kHz a signal-to-noise ratio of 150:1 is required to obtain a single layer resolution of ~ 60 μm.

A total of 32 chambers are arranged in two endcaps, as part of the ATLAS 'Small Wheels' which are positioned between barrel calorimeter and endcap toroidal magnets. Two versions of chambers, differing slightly in active area, are used ('large' and 'small') alternately for seamless coverage of the desired η region. A chamber has four identical layers, each providing a precision measurement in the (radial) bend direction and a coarser measurement of the transverse (azimuthal) coordinate. Each chamber has a total of 768 precision coordinate strips and 192 transverse coordinate strips. The precision strips have a readout pitch of 5.31 and 5.67 mm for large and small chambers, respectively. The strip capacitance ranges from 20–50 pF, depending on strip length which varies due to the chamber's trapezoidal shape.

Because of the severe radiation levels anticipated for the CSC environment, a minimum of the electronics is located on the detector. The on-detector electronics amplifies and shapes the cathode strip signals, and stores the analog pulse height information during the first-level trigger latency. When a trigger is received, four consecutive time samples are digitized and transmitted via fiber-optic links to the off-detector electronics. Sampling and digitization are performed on-detector but are controlled by the off-detector electronics.

The off-detector electronics processes the data in two stages. The sparsification stage suppresses hits below threshold and hits not associated with the current bunch crossing. The rejection stage identifies tracks and removes isolated background hits. The remaining data are formatted and sent to the ATLAS Trigger/DAQ System (TDAQ) for further processing.

II. THE CSC READOUT ELECTRONICS

A. The on-detector electronics

The CSC on-detector electronics [1, 2] consists of two layers of amplifier-storage module (ASM) boards. Each strip is connected to a preamplifier and shaper circuit, implemented as a radiation-tolerant custom ASIC, which forms a bipolar pulse with a 70 ns peaking time to mitigate pile-up effects. The shaped pulses are sampled every 50 ns, and the analog pulse height information is stored in a custom radiation tolerant CMOS switched capacitor array (SCA) for the duration of the first-level trigger latency, which for the CSCs is estimated to reach 188 bunch crossings in the worst case scenario. The SCA provides an effective pipeline depth of 288 bunch crossings. Following a trigger, those cells of the SCAs specified by the ROD are time multiplexed and digitized using 12-bit Analog Devices AD9042 ADCs. Custom ASICs multiplex the data from 16 ADCs to two G-Link serializers configured to operate with 16-bit input words at 40 MHz single frame rate.

Eight preamplifier/shaper ICs supporting a total of 96 channels reside on a printed circuit board (ASM-I). Two ASM-I boards piggyback on one

ASM-II which contains the 16 SCAs, ADCs, multiplexors serving 192 channels total, and two fiber optic G-Link transmitters. One HP-1024 fiber optic receiver handles incoming control signals from the ROD. A total of five such ASM-I/ASM-II combinations are needed to read out one chamber – four for the precision coordinate strips and one for the transverse coordinate strips from all four layers. Four ASM-I/ASM-II configurations are attached to the narrow edge of the chamber and share a common Faraday cage and cooling fixture. The transverse strip ASM-I/ASM-II package is attached to the broad side of the chamber, together with circuitry for injecting a pulse onto the wires of each layer for calibration purposes.

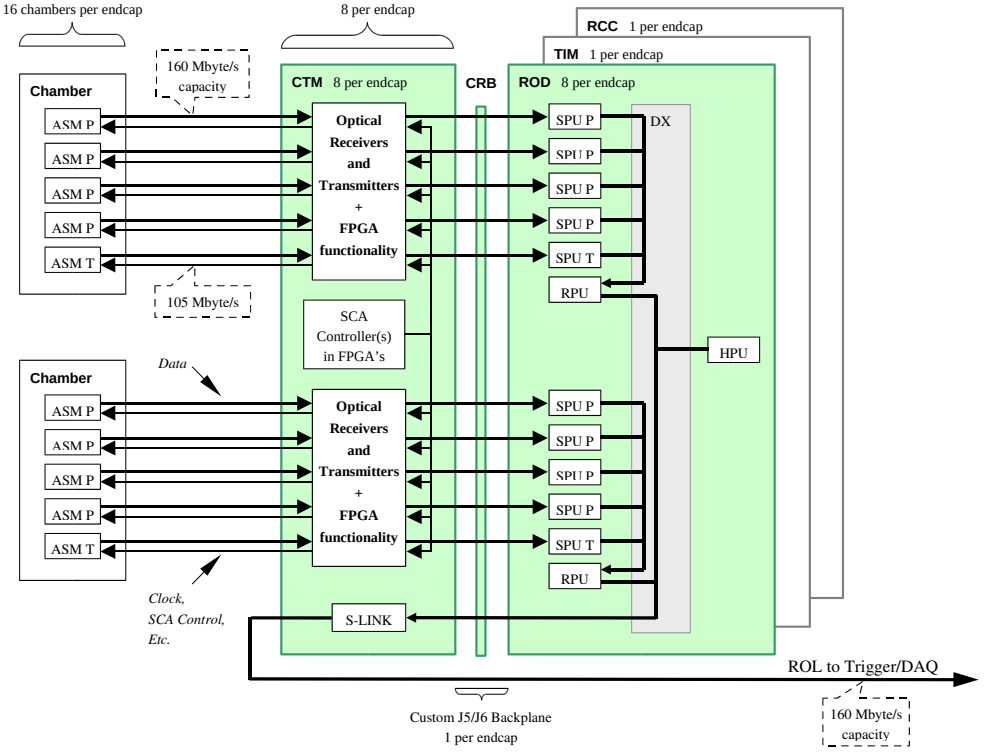

Figure 1: Principal design of the CSC off-detector electronics.

B. The off-detector electronics

The off-detector electronics [3] consists of 16 readout drivers (RODs), each coupled with a transition module (CTM). Each ROD/CTM pair handles the incoming data of two chambers, i.e. from 10 ASM-II boards (Fig. 1). It also controls the ASM-II, in particular the readout of the SCA when a trigger has been received. In addition the ROD provides data monitoring functionality, and controls the calibration pulser module. Eight RODs are housed in one 9U VME64x crate equipped with an additional custom backplane. The CTM contains all optoelectronics for readout and control of the ASM-II boards as well as for sending the processed data to the data acquisition system. It connects to the ROD directly via the custom backplane. A timing interface module (TIM) [4] in each VME Crate distributes clock and trigger signals to the CTMs. Each crate contains a Concurrent Technologies VP-110 single board computer which acts as ROD crate controller (RCC). It communicates with the TDAQ via Ethernet, and is responsible for relaying control commands from the TDAQ to the RODs. It also is used to collect information from the RODs for monitoring purposes.

While most of the ROD's control and data routing functionality is implemented in Xilinx Spartan-II field programmable gate arrays (FPGAs), processing of the ten 160 Mbyte/s data streams from the ASM-II boards is handled by digital signal processors (DSPs).

One 300 MHz Texas Instruments TMS320C6203 DSP with 2 MBytes off-chip memory supported by two Xilinx Spartan-II FPGAs for interfacing are grouped together on a small plug-in module. The ROD hosts 13 such modules, 10 for sparsification and cluster identification, two for event building and further background rejection, and one host module (HPU) which supervises the others and communicates with the RCC via the VME bus.

Most of the CTM's functionality is implemented in Xilinx Virtex-II Pro FPGAs. This includes the multi-gigabit transceivers for communications to the frontend, which couple with Zarlink ZL60101/2 12-channel parallel fiber optic modules (one transmitter and two receiver modules per CTM). Fiber optics communications to the ATLAS DAQ are provided by a HOLA S-Link [5] mezzanine card which plugs into the CTM.

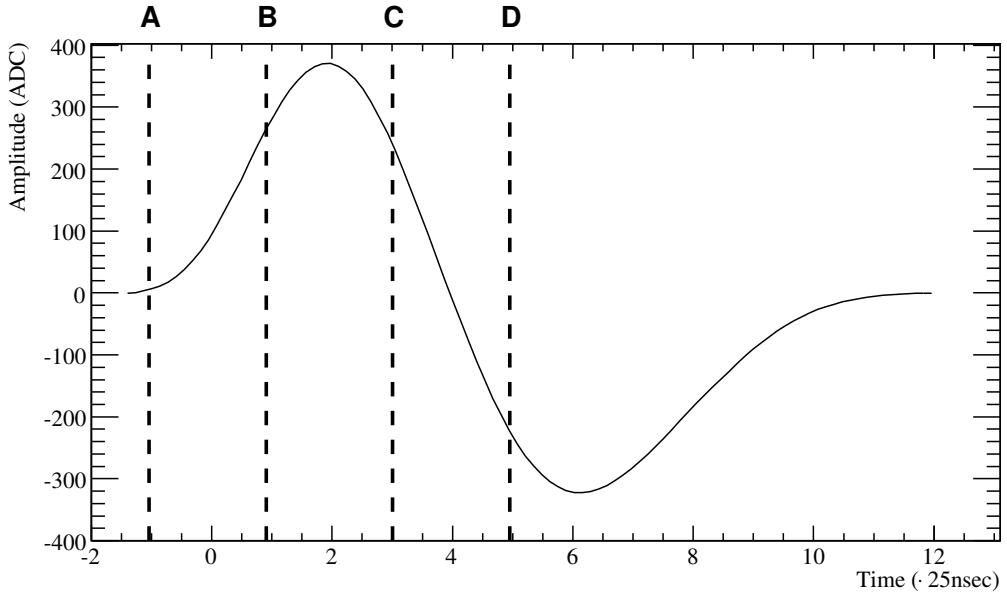

Figure 2: Typical CSC pulse shape, with sampling times (of arbitrary latency) indicated by dashed lines.

C. Off-detector electronics software

Signals associated with a particle trajectory must be correlated both in space (adjacent strips) and time (synchronized peaking times). The four consecutive time samples (Fig. 2) retrieved from each strip provide pulse shape information, i.e. charge and time. The effective trigger latency is adjusted so that the second and third sample are closest to the peak of the positive lobe.

Receipt of a first-level trigger automatically leads to readout of the four samples associated with the event. At the same time, the trigger information is propagated to the HPU.

The ten sparsification processing units (SPUs), one per ASM-II, reduce the raw data size by suppressing strip signals below a threshold determined by the channel's measured pedestal value, and by rejecting signals outside the timing window correlated with the trigger. The SPU applies calibration constants to the data, organizes the hits into clusters and determines their peaking time [6].

Data from the frontend is distributed to the SPUs via a bus system connecting to the DSP's expansion bus (XB). Data flow between SPUs and RPUs, and to the S-Link, is handled by a separate bus system called the data exchange (DX). It connects to the extended memory interface (EMIF) of the DSP. For each event, the fragments produced by the SPUs are moved to the associated rejection processing unit (RPU) in sequence. It performs a track search based on the clusters identified by the SPUs. Isolated clus-

ters are then removed from the event. The remaining data are transferred via the DX and the 160 Mbyte/s S-Link to the readout buffers of the ATLAS TDAQ system, where the data is stored during subsequent second-level trigger processing and event building.

The HPU controls and maintains the readout pipeline, i.e. it has the capability of throttling the data flow at various points of the pipeline. While raw data events are delivered to the SPU input buffers automatically, all subsequent steps – the actual processing of the data, transport from SPU to RPU, transport from RPU to S-Link – are only performed if requested by the HPU. Frontend readout can only be throttled by inhibiting triggers via a busy signal propagated to the ATLAS trigger. The event header and trailer – containing trigger, size, and status information – is inserted by the HPU directly. The assembly of the complete event fragment from two chambers is completed by sequencing header, payload, and trailer accordingly on the DX.

III. Commissioning

The complete readout chain from chamber to ROD had previously been tested with cosmic rays and with $>$100 GeV muons.

The chambers with attached frontend electronics were assembled on the Small Wheels in 2007 and commissioned one chamber pair at a time. The Small Wheels were installed in the ATLAS experimental cavern early in 2008. A full system readout has not been possible at the time of this conference due to a limitation of the VME power supplies, the solution for which is awaiting implementation by the manufacturer.

In the meantime, vigorous debugging efforts are made to remove the last stability and rate limitations in the ROD firmware and software. The system is expected to be ready in time for first collisions at the LHC.

IV. Conclusions

Muon tracking in the forward region of ATLAS is performed by cathode strip chambers. Because of the harsh radiation environment, the on-chamber readout electronics are kept as simple as is practical. Noise reduction measures are entirely performed off-detector. The off-detector electronics use DSPs for noise reduction and event building. At this time all hardware is installed. Firmware and software of the off-detector electronics is being debugged.

Acknowledgements

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