Status of the Reference Link

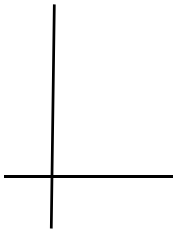
Jingbo Ye

Department of Physics

SMU

SMU

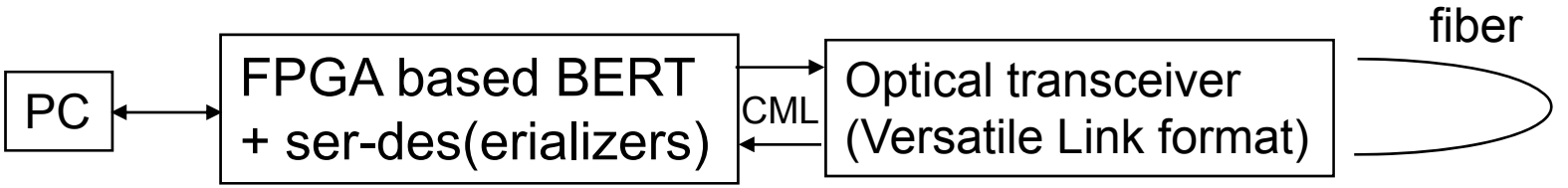
History of this project



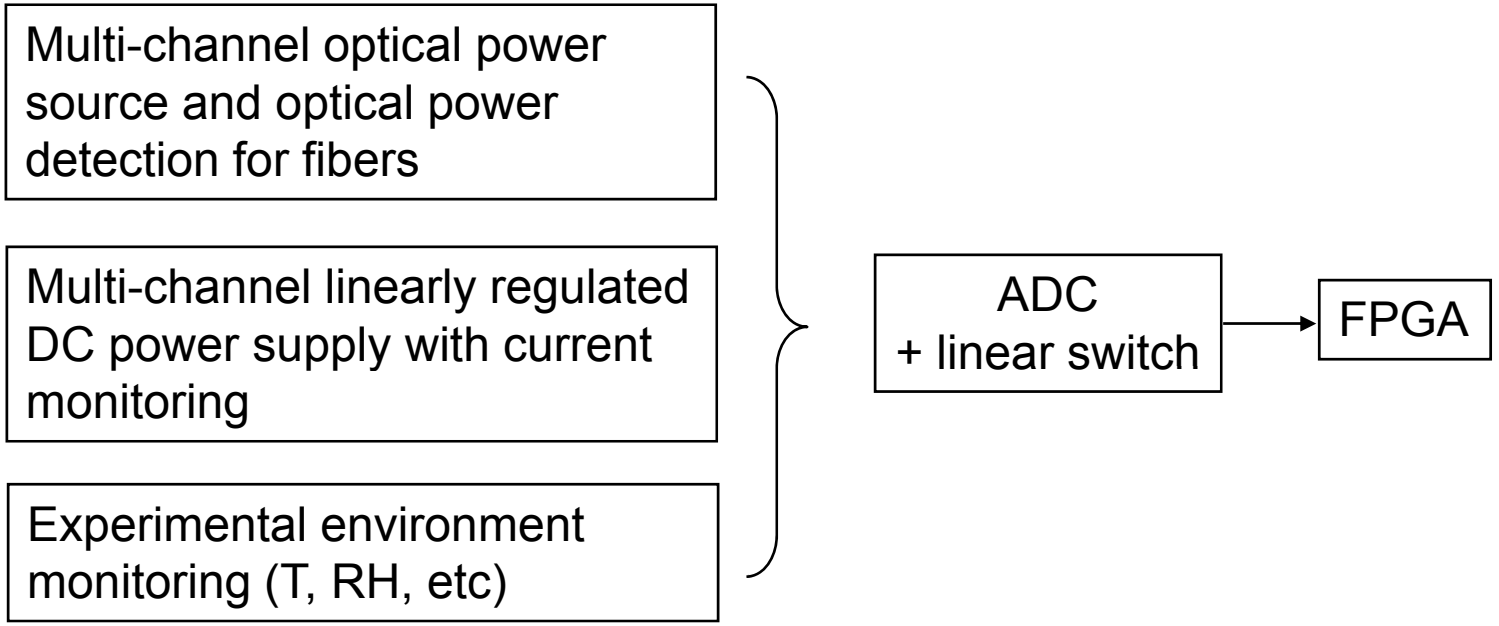
- Based on the working document from the Joint ATLAS-CMS optoelectronics working group subgroup C (https://edms.cern.ch/document/882784/2.0), the reference link has been proposed and proposals have been submitted to CMS and ATLAS.
- Meeting at SMU with OSU and UMN in Dec. 2007 as a kick-off to this project.
- It was decided to start with the Stratix II GX FPGA chip and its evaluation board, which has been purchased by SMU.
- The concept was to provide a standard reference link to optical link and its component development. This reference link would also serve as standard test bench hardware, on which firmware and software may be developed by “user” groups and shared. This way we may be able to standardize our test procedure and evaluation criteria. This will also make the results comparison easy among collaborating groups. Several institutes expressed interest to use such a test bench in their R&D projects.

The Reference Link block diagram

The core of the reference link:



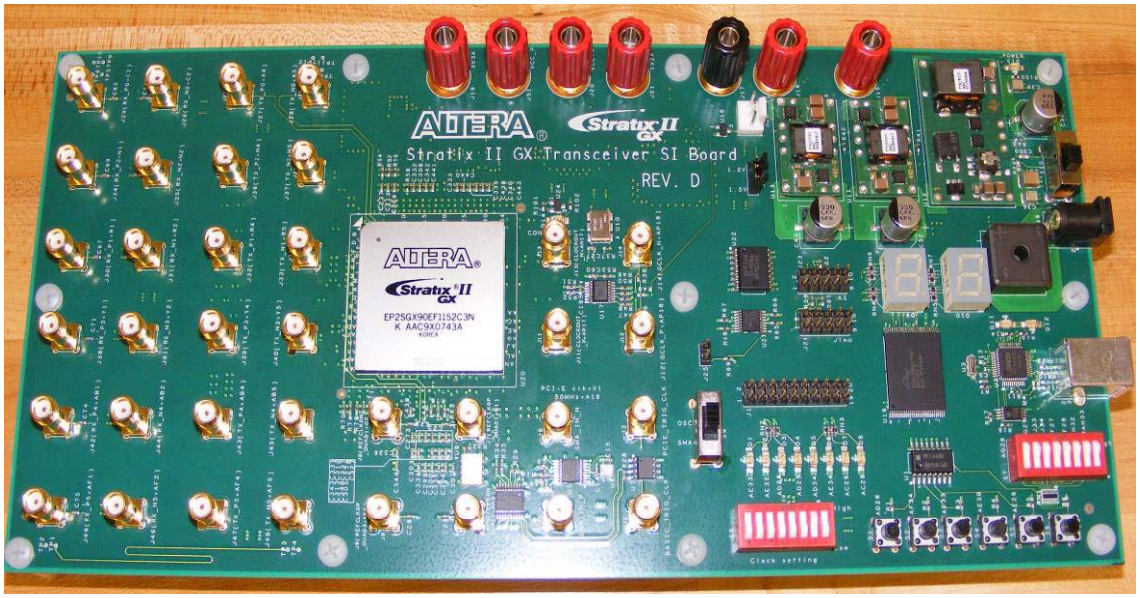
Added functions mostly for irradiation tests:



FPGA based BERT
+ ser-des(erializers)

The FPGA BERT + Ser-des

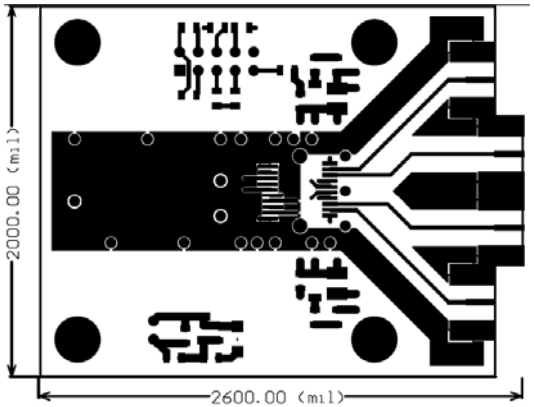
- Stratix II GX was chosen and the plan was to start with its evaluation board:
  - 6 channel ser-des from 0.6 to 6 Gbps.
  - Evaluation board ~$1k, cheaper than the chip itself.
  - We have most part of the BERT firmware developed for another Altera chip and can be ported into this chip.



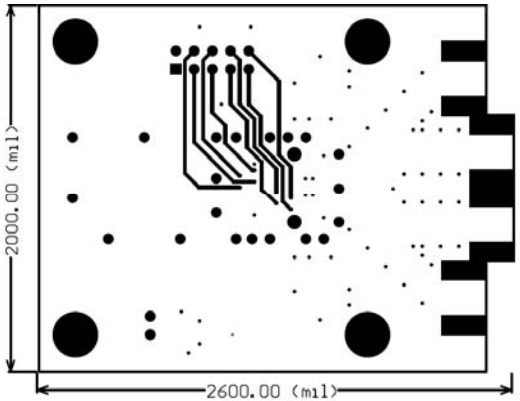
Optical transceiver
(Versatile Link format)

The SFP+ board

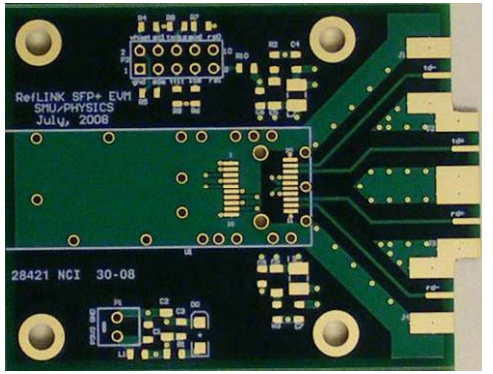
SFP+ has been chosen to be candidate for the Versatile Link standard

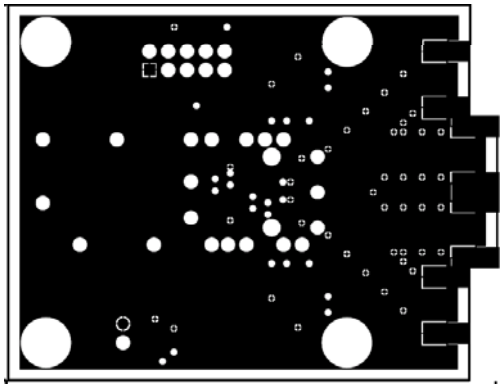


Top Layer

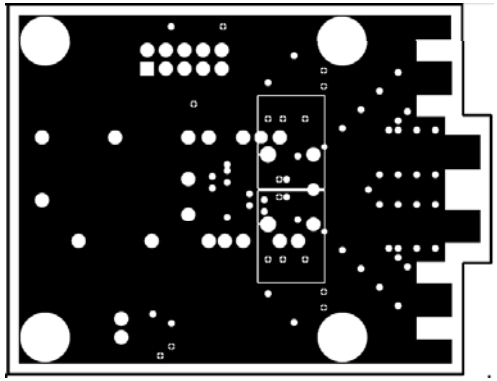


Bottom Layer

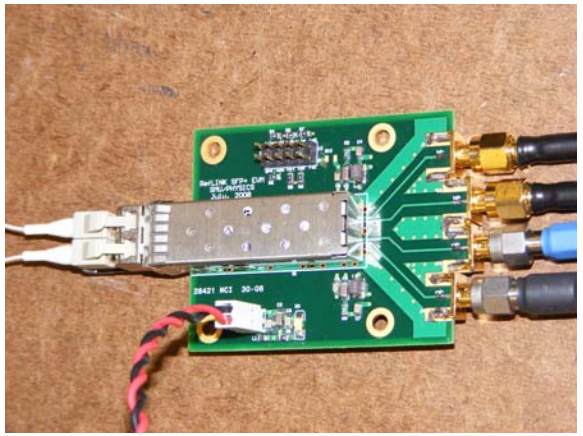




Ground Layer



Power Layer

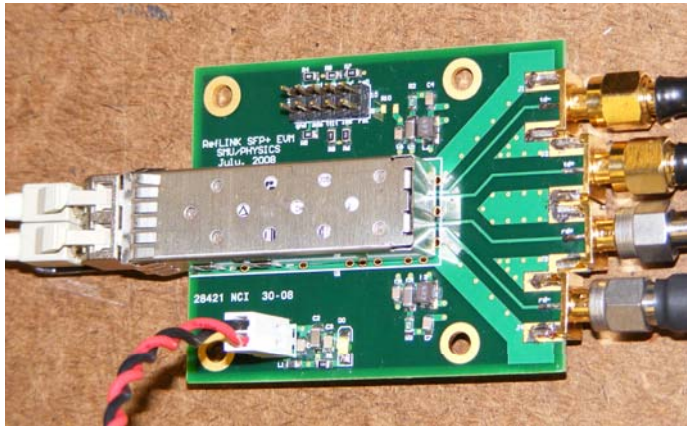


Preliminary tests on the SFP+ board

- Eye diagram tests at 3, 5, 8 and 10 Gbps.
- The setup:
  - Signal generator: the 12G BERT
  - Module under test: AFBR-700SDZ (10Gb, 850 nm) from Avago.
  - A short fiber is used to loop the optical signal from TX to Rx.
  - The Scope: 20GHz real-time w/ the 8GHz differential probe. Measurement carried out at the RX of the SFP+.
  - In the future, a sampling scope with higher bandwidth will be used and measurements will also be carried out at the TX of the SFP+.
- The conclusion: this board works up to 10 Gbps.

Test equipment

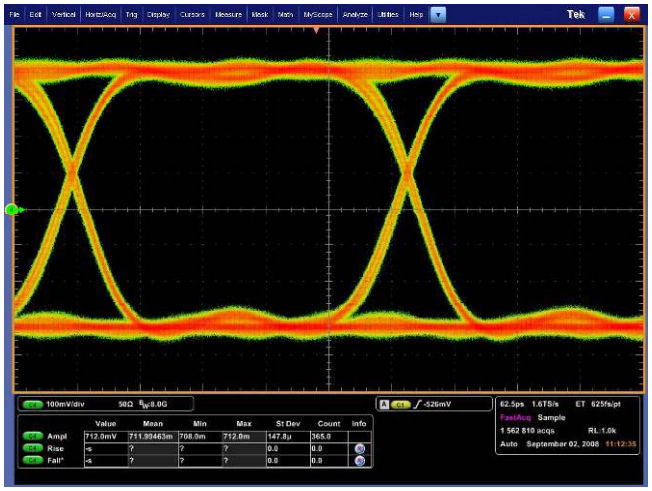
BERT



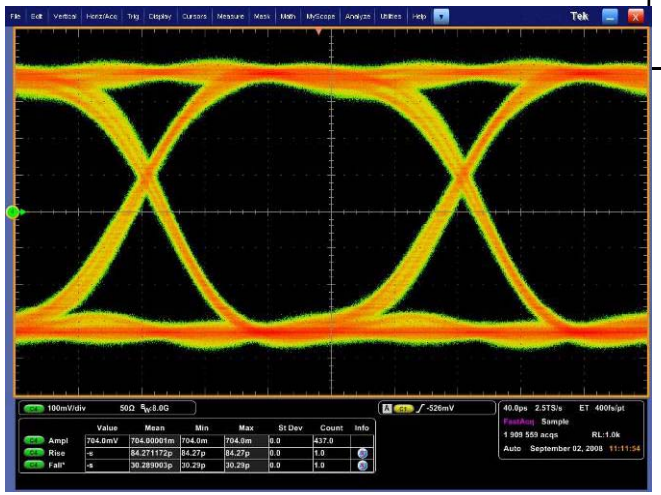
Real-time scope

sampling scope

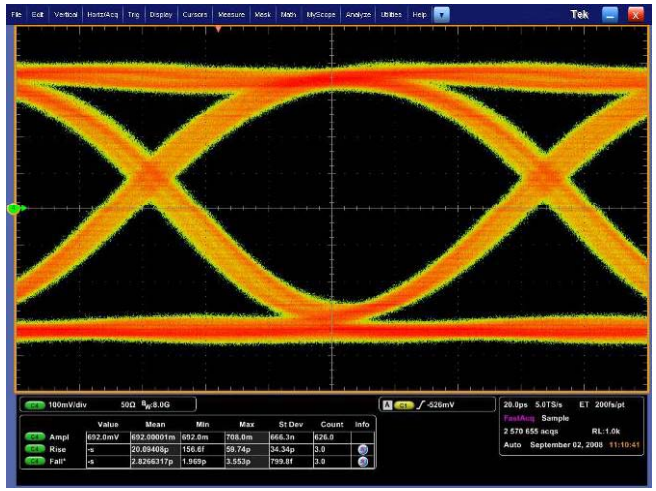
Eye diagrams



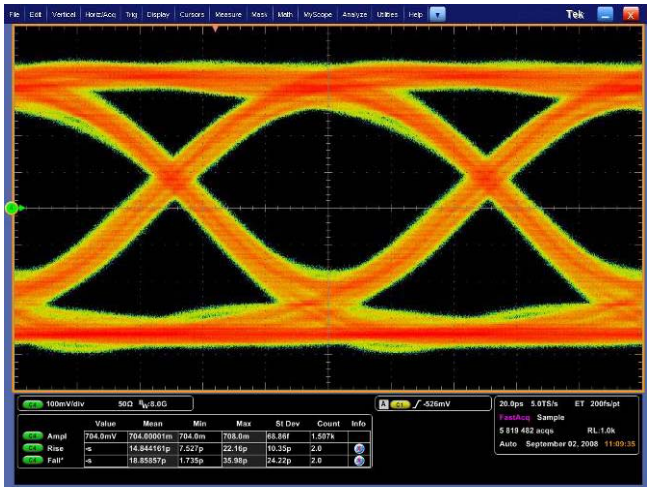
3 Gbps



5 Gbps



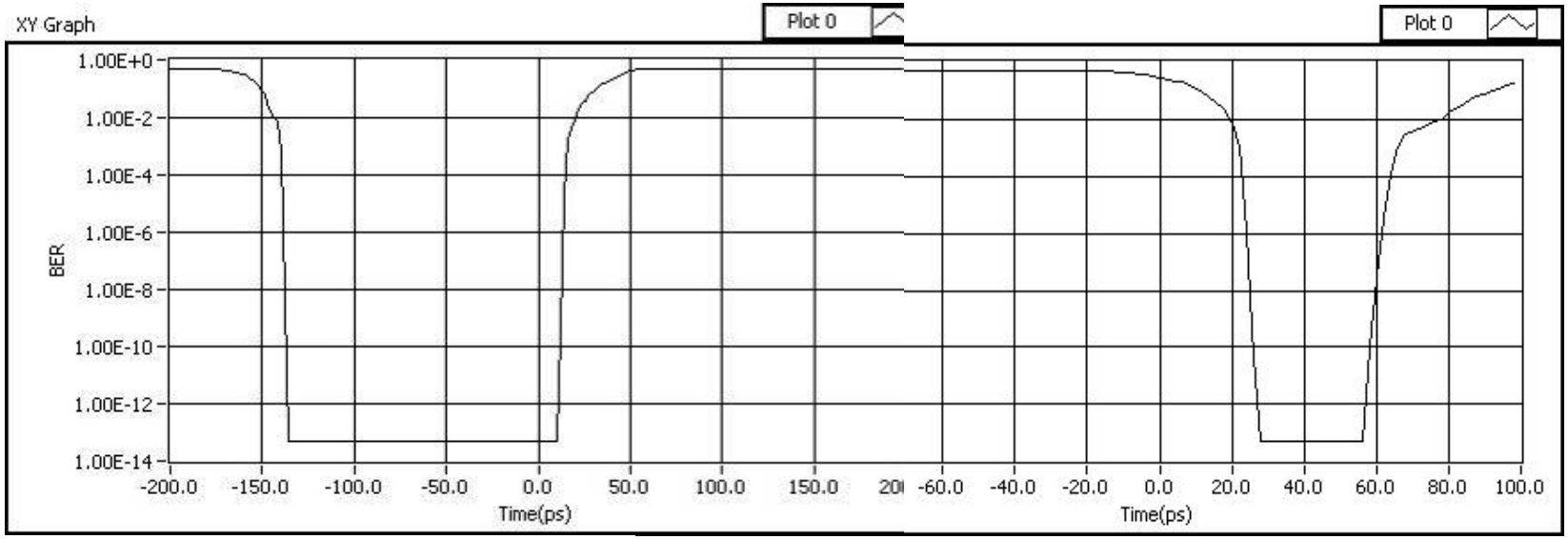
8 Gbps



10 Gbps

Bit Error Rate at 5 and 10 Gbps

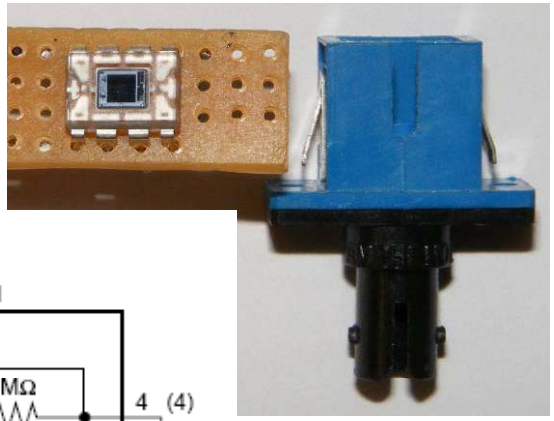
- The BER at 10 Gbps is better than 3E-14: no error for more than 1 hr.
- We still have issues between the eye diagram and this BERT measurement at 10 Gbps. The results are preliminary.

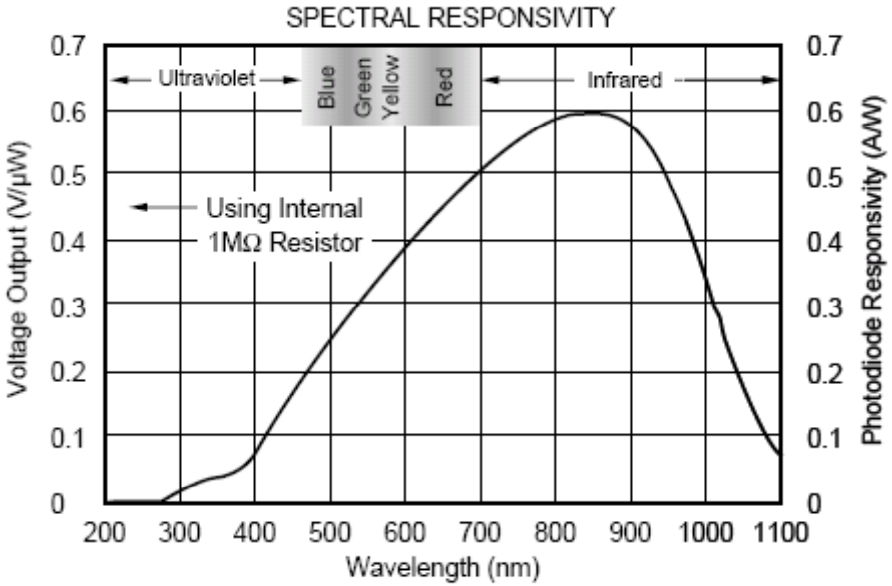


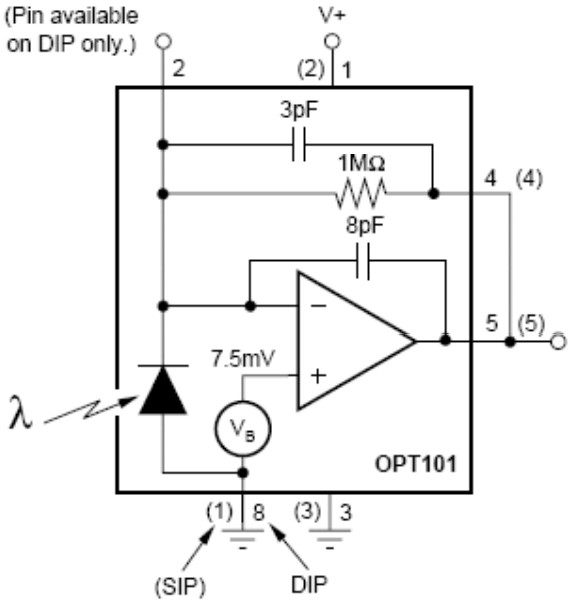
The bathtub curves at 5 Gbps and 10 Gbps

Other components identification for the added functions to reference link test bench

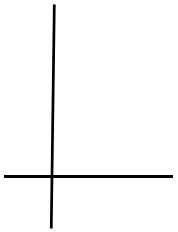
- At SMU we have a board that provide 8 channel adjustable and linearly regulated DC power with current monitoring (a voltage signal). This board takes an input from a switch power supply.
- Optical light source is chosen to be VCSEL at 850 nm for the moment. May add 1310 nm wavelength later.
- Optical power measurement: OPT101 from Burr-Brown.
  2.3×2.3 mm^2 photodiode + TIA.
  Dynamic range: 0.01 μw to a few mW.
  Can be easily packaged into a ST connector.







Summary and plan



- The optical transceiver board has been design, fabricated and is under tests. Preliminary results indicate that this board works up to 10 Gbps.
- The Stratix II GX has been purchased. Firmware porting and development for the BERT is taking place at SMU.
- Other components/boards have been identified for the added functions.
- The plan:
  - A demonstrator link for the core part of the reference link with the Stratix II GX evaluation board and the SFP+ board, and with the existing firmware: by the end of 2008.
  - Firmware (software included) development for a basic BERT function, ser-des channel and PC interface: Q2 of 2009.
  - “User” evaluation follows and a “user” document will be generated.
  - The added functions will be developed whenever engineering resource becomes available.