Trigger Hardware
GCT Muon and Future Developments

GCT Muon and Quiet Bits System
Production and Status

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Overview

- New Trigger Processing system
- Originally required for GCT Muon and Quiet bits
  - New system required to meet this requirement
- Design for more general purpose system
  - Meets GCT requirements
  - Can be used for more generic purposes
  - Evolution of current GCT design
- Based on Commercial standard
  - Micro TCA
    - Modular telecommunication industry standard
  - Two components
    - Processing module (known as Matrix processor)
    - Full connectivity backplane
    - This review will focus on the processing module
Hardware “Family Tree”

- The Current GCT processing hardware is an evolution of several related successful designs at LANL and CERN
- 2004: Double PMC channelizer mezzine (LMA/LANL)
  - First use of 2Gb SERDES (external TLK series)
    - 8 full duplex links
  - Xilinx Virtex 2 FPGAs (2x 2V6000)
- 2005: Single PMC processing mezzine (LANL)
  - First use of embedded SERDES (Xilinx V2P40)
    - 4 full duplex links
    - High power density, link isolation
- 2006: GCT Leaf (CERN)
  - 32, 2Gb embedded SERDES receive channels (2x 2VP70)
  - First use of SNAP-12 optics
- 2007: CPCI MRM satellite signal processor (LANL)
  - Very large rad tolerant FPGAs (V4LX200, V4SX55)
  - 300MHz RAM interfaces (QDR SRAM), high density matched busses
  - Radiation tolerant, flight design
- 2008: Current Design – Matrix uTCA processing module (CERN/LANL)
  - Full serial design, 72+ 3.2Gb full duplex links
  - 500MHz RAM interfaces, 512Mb DDR2 RAM
  - First use of large crosspoint SERDES switch
Primary System Design Goals

- Modular
  - Reasonably fine grained
    - Smaller circuit boards
    - Easier and less expensive to develop
  - Should scale well
- Well defined internal interfaces
  - Allows modules to be developed independently
    - Perhaps shared across projects
  - At least electrically compatible
- Flexible in both logic and interconnect
  - Retain flexibility of FPGAs
  - Add complementary data routing flexibility
    - Modify data flow without altering hardware
    - Give the ability of dynamic reconfiguration
GCT Muon and Quiet Bits System

• Secondary Function of the GCT
  – Receive data from 18 RCT crates
  – Reformat and pass on to GMT

• Details
  – 18 fiber inputs
    • 2.0Gbps from GCT source cards
      – Located in RCT racks
    • Standard 8b/10b encoding
    • Each fiber represents 40 degrees in phi, ½ barrel in eta
  – Serial outputs now routed to Opto GTI on GMT
    • 2.0 - 3.2Gbps to GMT
    • Exact details of interface still being finalized
    • Data organized in 120 degree phi, full barrel eta
Initial System

- Three processing modules
  - Known as “matrix processors”
- Custom or commercial backplane
  - Custom preferred for flexibility
  - Commercial usable for this application
    - Only processing module needed for this system
- “Dumb” power module for initial systems
  - Does not implement uTCA power management
  - Commercially available
  - Move toward full compliance as time permits
Processing module Block diagram

12 channel MTP receive

8 channel MTP transceiver

12 channel MTP transmit

Xilinx V5LX110T (16, 3.2Gbps MGTs)

Mindspeed M21141 72x72 crosspoint

uTCA 21 3.2 Gbps Links

12V

POL supplies
3.3V switcher
1.0V switcher
2.5V linear

NXP LPC23xx uController

Enet

3.2 Gbps Links

12V
Key Features of Processing Module

- **Xilinx Virtex 5LX110T/FX70T FPGA**
  - 16 low power MGTs, Superior logic density/speed
  - Board supports both 3.2 and 6.0 Gbps transcievers

- **Data I/O direct from fiber**
  - 16 channels full duplex @ 3.2 Gbps

- **Crosspoint routes to FPGA, backplane, and fiber**
  - 1:N data replication supported at wire speed
  - FPGA output data sent to backplane or fiber
  - Switches clocks as well as data
    - Dedicated low jitter clock tree provided for MGT reference
    - Clock output to backplane from crosspoint

- **Slow control via standard Ethernet**
  - Standard Ethernet protocols supported by NXP 2368
  - Connection provided for stand alone operation
Additional Features

- Module development is co-funded by Los Alamos
  - First use of related design in 4/09
- Additional RAM
  - 512MB DDR2 SDRAM added to module
    - Two banks of 128Mx16 @ >500MHz
    - Enables sophisticated SoC possibilities
      - Processor subsystems used in some MRM firmware
      - ~100 high speed (500 MHz), length matched traces
- Other Xilinx V5 features of interest
  - PCIEExpress endpoint
    - Growth path for LANL CPCI systems
    - Currently implemented on test systems at Princeton
  - GigE MAC
    - Independent fast link to high level systems
  - Power PC (FX70T)
  - 6 Gbps transceivers (FX70T)
Design Considerations

• Signal Integrity
  – ~150 3.2 Gbps differential pairs
    • 72 full duplex pairs + clocks
    • 1.6GHz requirement (3.2GHz edge rate)
      – 3GHz desired to support latest Xilinx devices
    – 2 500MHz DDR2 RAM interfaces
      • 128Mx16 devices
      • Requires tightly matched traces
• Power density
  – Total power > 20W
    • Split between analog and digital power
  – Single 12V source requires intermediate regulators
    • Switcher to reduce voltage for linear regulators
• Signal Density
  – Small board size (75x180mm) limits physical isolation
Base Attenuation Test

- Hardware test using coax with equivalent cross section derating
  - Pasternack 0.047 inch semi rigid coax with a 11.3 mil diameter center conductor.
    - 35.5 mils circumference
    - Board t-lines are 3.5 x 0.7 mils or 8.4 mils around. Skin effect losses are therefore about 4.2 times higher per cm in the circuit board.
  - Coax tested is equivalent to 14.4 cm of length in our board
- Measured output risetime of 89 ps is not significant since it is quite a bit less than the 312 ps in one half of the period of 1.6 GHz. 10-20% pre-emphasis will be required to maintain full amplitude at the receiving end.
Test Board

• Realization that simulation is likely not adequate
  – Actual tolerances in PCB construction
    • Impedance control
    • Effect of various via technologies
    • Sizable effects at frequencies approaching 3GHz

• Test board designed to test margins
  – Various routing and via types
  – Designed to connect cleanly to test equipment
    • TDR, Network analyzer, 40 GHz scope
  – Doubles as instrument interface to Matrix processor
    • Allows signal injection and monitoring
  – Will be used to test backplane as well

• Design is complete, production is commencing
Advanced PCB Techniques

- Lower risk and increase performance
  - Standard process for current fabrication technology
  - Less demanding than multi laminate process used on leaf
  - Less risk than multi laminate high layer count used on MRM signal processor (improved yield)
- Micro Vias (Laser drilled)
  - Penetrate several layers (2-3)
    - Provide lowest inductance/best impedance match
    - Useful for both power and high speed signals
  - Can be stacked with both standard and micro vias to provide larger spans
  - Used in conjunction with “build up” board fabrication
- Via in pad
  - Micro via or drill via
  - Eliminates BGA escape pattern for higher performance
    - A must for very fine pitch BGAs (<1mm)
- Both technologies are being used in the design
  - Vendor (DDI) considers this the lowest risk approach
  - 12 layer board with 12 possible via spans (8 used)
- Preliminary gerbers sent to DDI early June for inspection
  - No manufacturing issues identified
# Stackup

## CLASS 2 BOARD

### Proposed to DDI ON: 05/15/2008

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<th>Proposed AMC module stacks</th>
<th>Conventional</th>
<th>Micro-laser drill with B-Stage</th>
<th>Visual only</th>
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<th>Visual only</th>
<th>Micro-laser DDI WILL BE TAKING MY 1-6 AND STACK IT WITH THE 1-2 &amp; 2-6 VIA'S AND MY 7-12 AND STACKING IT WITH 11-12</th>
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Fabrication Process

- Top and bottom 4 layer sections
  - Layers 3-6 and 7-10
  - Conventional process with 8 mil drill through vias
  - Micro via 2-3 and 11-10
- Laminate top and bottom sections and drill 8 mil through vias
- Deposit layer 2 and 11
  - Micro via 2-3 and 10-11
  - Stack micro on conventional to obtain 2-6, 7-11
- Deposit layer 1 and 12
  - Micro via 1-2 and 12-11
  - Stack micro vias to obtain 1-3, 1-6, 12-10, 12-7
  - Conventional drill through vias
- Layers 3, 5, 8, and 10 are controlled impedance
  - 100 ohm differential traces
- Layers 1 and 12 “semi controlled”
  - 100 ohm differential traces with larger tolerance >10%
Component Layout
Component Layout (bottom)
Layer 3 Routing
Layer 10 Routing
Production Status

• Prototype circuit boards received
• In process of qualifying an assembly house
  – Outfit used in the past several years was acquired
    • New owners not interested in small runs
  – Several candidates
    • Vendor used for satellite work
      – Class 3 facility
      – Track record of good performance
      – Very expensive
    • New vendor recommended by board manufacturer (DDI)
      – Unknown quality
      – Very reasonably price (perhaps too reasonable)
    • Assembly requires fine pitch components and mixed Pb/RoHs
• All components in hand or commodity items
  – Assembly will commence as soon as vendor selected
Embedded software

- Microcontroller software
  - Basic communication
    - I2C, Ethernet
  - Debug support
- No significant progress
  - Disappointing progress by part time student
- Initial work is being taken over by Princeton
- Related project starting at Los Alamos
  - Take over from Princeton for common functions
  - Build on publicly available uTCA core functionality
  - Flight quality application required
    - Hopefully can create a common framework
    - Will allow collaboration on higher level software as well
Update on Backplane

- Layout has now started
  - Initial component placement done
  - Overall construction method chosen
    - Relatively thin PCB laminated to rigid stiffener board
- Production review scheduled for 2/09
  - Time to include results of testing
    - Matrix module
    - Test board margin tests
  - Likely will require more aggressive routing
    - Test board will define what structures will be permitted
      - Processing module design rules allow limited layer switching
      - Need to understand how far one can go and maintain performance
  - Looking into design tool upgrade
    - Poor support of differential pair routing
    - Currently a hand optimized process – very time consuming