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SPECS: a Serial Protocol for the Experiment Control System of LHCb

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The LHCb sub-detector electronics requires a configuration bus able to communicate efficiently and reliably over an up to 120-meter line, between a master, located in the counting room which is not exposed to radiation, and up to 32 slaves located on the detector close to electronics boards. The slaves have been developed in order to work properly in radiation exposed environment (up to 40Krad of total dose). The SPECS system is composed of a master board, that hosts 4 SPECS masters, and slaves (mezzanine boards) which provides all the necessary service functions and offers different bus interfaces.

Summary

SPECS: a Serial Protocol for the Experiment
Control System of LHCb.
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The LHCb sub-detector electronics is organized around the detector in crates or individual boards, which require a configuration access to load and read different types of information. These operations will be driven from computers located in the control room, roughly at a distance of 60 meters from the various front-end elements. Therefore, the experiment requires a configuration bus able to communicate fast and properly over an up to 120-meter line, with a unique master, and up to 32 slaves. In such a configuration, the master card will be located in the control room, which is not exposed to radiation, and the slave close to the detector electronics boards. The slave thus has to be both SEL and SEU immune, in order to work properly in radiation sensitive environments (up to 40Krad of total dose).
The SPECS protocol is a 10 Mbit/s serial link designed for the configuration of remote electronics elements. SPECS is a single-master multi-slave bus. The protocol requires 4 or 8 copper links (4 lines or 4 pairs) in BLVDS technology with pole-zero cancellation at the emitter side. The 8-pin RJ45 connector was thus chosen for the interconnections. It is a cheap and compact standard, which can be associated with Etherne cables (cat 6 type).
The SPECS frame is composed of a fixed-size header (8-bit words which contain information relevant to the transfer), a variable-size data block, and a fixed-size trailer with the checksum of the data block.
The SPECS master board will host 4 SPECS masters. This board is implemented on a standard 3.3V 32-bit 33 MHz PCI board, which can be plugged into any PC. The board also includes a SPECS slave for JTAG and I2C output capability. The heart of the system is designed as a portable VERILOG code and integrated within an Altera Cyclone FPGA, the PCI interface being performed by a dedicated circuit (PLX9030).
The SPECS slave offers different interfaces: Point to point SPECS interface for long distance interconnections, Multi drop SPECS bus, Local bus parallel interface, 32 configuration I/O lines, JTAG master interface, long distance I2C master bus: For the JTAG and I2C outputs, 24 command signals allow the slave chip to drive up to 12 independent links.
An intermediate mezzanine board of 0.47dm² houses the SPECS slave, and provides all the described functionalities using 2 SMC connectors. The mezzanine board also provides most of the necessary service functions for the sub-detector front-end electronics: long distance drivers, 6 channels ADC, local oscillator. The goal is indeed to avoid putting any unnecessary electronics in the radiation sensitive area.: corresponding author.

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