Development and Testing of an Advanced CMOS Readout Architecture dedicated to X-rays silicon strip detectors

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Abstract

Design methodology and first test results of a novel integrated readout front end analog processor in a 0.35 μm n-well complementary metal-oxide semiconductor technology are reported. The specific processing channel consists of a low noise preamplification block and a pulse shaping stage and has been designed for multi-channel radiation detectors with capacitance ranging from 2 to 10 pF. Important feature is the novel CR-RC^2 pulse shaper configuration. In this section, transconductance circuits are used and a new design approach using the Leapfrog methodology is applied Considering the architecture measured performance, the prototype provides peaking time 1.81 μs, conversion gain of 3.31 mV/fC and *enc* of 382 e^- + 21 e^-/pF. The system consumes 998 μW and the occupied area of the full VLSI structure is 0.202 mm^2. Characterization of the analog processor and measurements are presented supporting the theoretical analysis and confirming that the system operates according to nuclear spectroscopy design specifications.

I. Introduction

The current trend in high energy physics, biomedical applications, radioactivity control, space science and other disciplines that require radiation detectors, is towards smaller, higher density systems to provide better position resolution. Miniaturization, low power dissipation and low noise performance are stringent requests in modern instrumentation where portability and constant increase of channel numbers are the main streamlines. In most cases CMOS technologies have fully proven their adequacy for implementing data acquisition architectures based on functional blocks such as charge preamplifiers, continuous time or switch-capacitor filters, sample and hold amplifiers, analog-to-digital converters etc. in analog signal processing for particle physics, nuclear physics and X or beta ray detection.

While literature is available on the noise behaviour of the front end stages [1]-[2], contrary few studies have been performed on the pulse shaper circuit. The main problem in the design of nuclear spectroscopy VLSI shaping filters is the implementation of long shaping times in the order of *μs*. In the past, the possibility of implementing RC networks in integrated versions of high-order semi-Gaussian shapers were limited by technology constraints (maximum R and C values are in the MΩ range for the resistors and in the 100 pF range for the capacitors) with time constants usually not exceeding few hundreds of *ns*. To implement integrated RC networks with time constants in the range of *μs*, as is specified in our application, some topologies have been proposed [3]-[6]. All these solutions are based on the common principle of using current mirror to demagnify the current flowing in a resistor in order to operate as a higher value resistor with respect to its nominal value.

In this work an alternative design technique and a novel long shaping time readout analog processor, is presented with purpose to be used with a specific radiation detector. In the specific architecture the shaping filter, in controversy to the typical structures, is not based on op-amps which generally demand large-area input transistors and high bias currents, but on operational transconductance amplifiers (OTAs). The total CSA – shaper system is characterized by low power and low noise performance compatible with the stringent requirements of high resolution nuclear spectroscopy and appears being greatly flexible providing programmable operating bandwidth and consequently adjustable output pulse characteristics.

II. Preamplification Stage Design

The Preamplifier circuit is shown in Fig. 1. The core amplifier is a folded cascode structure, because of its high DC gain and the relatively large operating bandwidth. This configuration allows the DC level of the output signal to be the same as the dc level of the input signal. The CSA reset device was configured with a PMOS transistor (M11) biased in the triode region in order to avoid the use of a high value resistance.

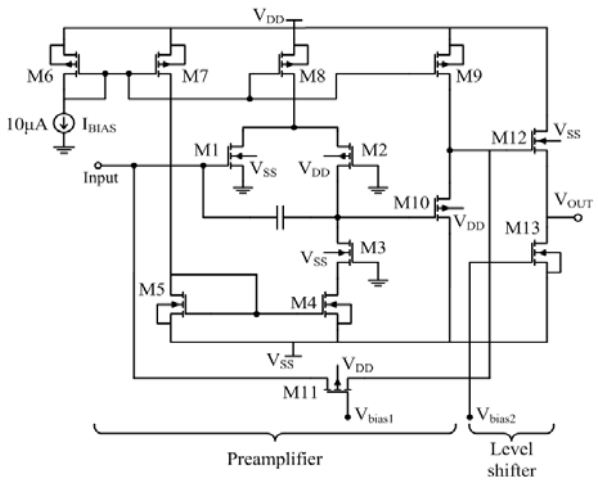

Figure 1: Preamplifier circuit with output level shifting stage

Transistors M11 and M12 comprise a level shifter for the CSA output signal providing the capability to externally control the pre-amplification stage output signal DC level. Regarding the noise optimization of the preamplifier, an NMOS transistor with optimized dimensions was selected as the circuit input device [1]-[2].

III. Shaping Filter Analysis and Design

Semi-Gaussian (S-G) pulse shaping filters are the most common pulse shapers employed in readout systems, their use in electronics spectrometer instruments is to measure the energy of charge particles [7] and their purpose is to provide a voltage pulse whose height is proportional to the energy of the detected particle. The theory behind pulse shaping systems, as well as different realization schemes, can be found in the literature [7]–[9]. It has been proved that a Gaussian shaped step response provides optimum signal to noise characteristics. However, the ideal S-G shaper in non casual and can not be implemented in a physical system. A well known technique to approximate a delayed Gaussian waveform is to use CR-RC^n filter [7]. Such shaper principal schema is shown in Fig.2

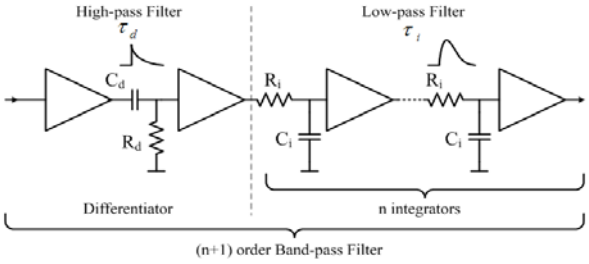

Figure 2: Principal diagram of a CR-(RC)^n shaping filter

A high-pass filter (HPF) sets the duration of the pulse by introducing a decay time constant. The low-pass filter (LPF), which follows, increases the rise time to limit the noise bandwidth. Although pulse shapers are often more sophisticated and complicated, the CR-RC^n shaper contains a lower frequency bound and an upper frequency bound and it is basically a (n+1) order band pass filter (BPF), where n is the integrators number. The transfer function of an S-G pulse shaper consisting of one CR differentiator and n RC integrators (Fig.4) is given by [1]:

$$H(s)_{shaper} = \left(\frac{s\tau_d}{1+s\tau_d}\right)\left(\frac{A}{1+s\tau_i}\right)^n = H(s)_{BPF} \qquad (1)$$

where τ_d is the time constant of the differentiator, τ_i of the integrators, and A is the integrators dc gain. The number n of the integrators is called shaper order. Peaking time is the time that shaper outputs signal reaches the peak amplitude and is defined by:

$$\tau_s = n\tau_i = nRC \qquad (2)$$

Increasing the value of n results in a step response, that is closer to an ideal Gaussian but with larger delay. The order n and peaking time τ_s, depending on the application, can be predefined by the design specifications or not. The operating bandwidth of an S-G shaper is given by:

$$BW = f_i - f_d = \frac{1}{2\pi\tau_i} - \frac{1}{2\pi\tau_d} \qquad (3)$$

The above combined band-pass frequency behaviour, enhances the SNR by separating the "noise sea" from the signal main Fourier components. The choice of the cut of frequencies defines the shaper noise performance and consequently the SNR. In addition, the frequency domain transfer characteristics are strictly linked to the shaper time domain behaviour or output pulse shape [10]. Concerning the shaper peaking time, in order to achieve a predefined from the application specifications value, the shaper model passive elements should be suitably selected. The total CSA – 2nd order S-G shaper system transfer function using a Laplace representation is:

$$H(s)_{total} = \left(\frac{A_{pr}}{1+s\tau_{pr}}\right)\left(\frac{s\tau_d}{1+s\tau_d}\right)\left(\frac{A_{sh}}{1+s\tau_i}\right)^2 \qquad (4)$$

where A_{pr} is the preamplifier gain and τ_{pr} is its time rise constant. If as input signal is a dirac pulse δ(t), considering the inverse Laplace transform of the product, the output signal in the time domain is given by:

$$h_{total}(t) = \int_{\sigma-j\omega}^{\sigma+j\omega} H_{total}(s)\cdot e^{st} ds \qquad (5)$$

Solving the above integral, the output signal of the readout system is:

$$h_{total}(t) = A_{pr}\cdot A_{sh}\cdot\left(k_1 e^{-t/\tau_{pr}} + k_2 e^{-t/\tau_d} + k_3 e^{-t/\tau_i} + k_4 t e^{-t/\tau_i}\right) \qquad (6)$$

k_1, k_2, k_3 and k_4 are the below constants:

$$k_1 = \frac{a}{a^3 - a^2(b+2c) + a\cdot c(c+2b) - b(c)^2} \qquad (7)$$

$$k_2 = \frac{b}{(b-a)\cdot(c-b)^2} \qquad (8)$$

$$k_3 = \frac{a\cdot b - c^2}{(c-a)^2\cdot(c-b)^2} \qquad (9)$$

$$k_4 = \frac{(a+b-c)\cdot c^2 - a\cdot b\cdot c}{(c-a)^2\cdot(c-b)^2} \qquad (10)$$

where $a = (\tau_{pr})^{-1}$, $b = (\tau_d)^{-1}$ and $c = (\tau_i)^{-1}$.

In order to design a flexible IC shaper that can provide a peaking time (μs range), the above theory was combined with the leapfrog design technique. The respective to Fig.4 two-port passive element network, was configured as to implement an equivalent IC 2nd order S-G shaping filter (Fig.3).

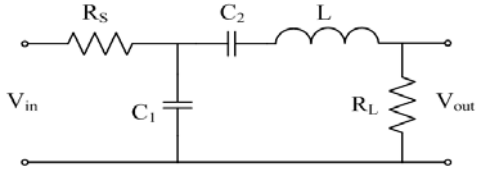

Figure 3:Equivalent RLC minimum inductance two port circuit of a 2nd order S-G shaper

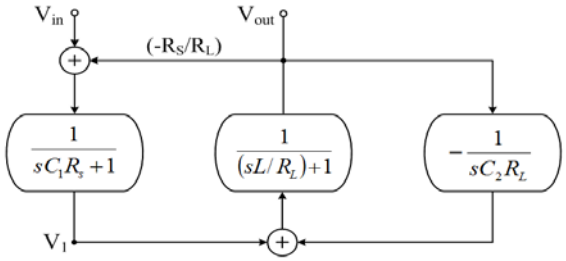

Figure 4: Signal flow graph of a voltage mode 2nd order semi-Gaussian shaper

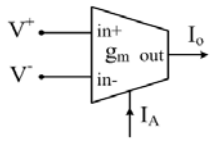

Figure 5: Symbol of the OTA

The above passive element topology has a respective transfer function (Laplace representation) to the typical shaper model of Fig.2. Its Laplace representation is given below (2nd order S-G shaper). From the above two port network, the signal flow graph (SFG) of a second order S-G shaping filter is extracted (Fig.4). The output signal of the passive network, in relation to the SFG is given in 12.

$$H(s)=\frac{\left(\frac{1}{LC_1}\right)s}{s^3+s^2\left(R_SR_LC_1+L\right)\frac{1}{LC_1}+s\left(\frac{C_1}{C_2}+R_L+R_S\right)\frac{1}{LC_1}+\frac{1}{LC_1C_2}} \quad (11)$$

$$V_{out}=\frac{1}{\frac{sL}{R_L}+1}\left(V_1-V_{out}\frac{1}{sC_2R_L}\right) \quad (12)$$

Using the extracted SFG and the Leapfrog (functional simulation method) design methodology a 2nd order shaper is designed. The main advantage of the Leapfrog method over others filter design methods which also provide integrated structures is the better sensitivity performance and the capability to optimize the dynamic range by properly intervening during the phase of the original passive synthesis [11]-[13]. In order to implement the shaping filter, operational transconductance amplifiers (OTAs) were selected as the basic building cells. The symbol of the OTA is shown in Fig.5. Ideally, the OTA is assumed to be an ideal voltage-controlled current source and can be described by:

$$I_0=g_m(V^+-V^-) \quad (13)$$

where I_0 is the output current, V^+ and V^- denote the non-inverting and inverting input voltages of the OTA, respectively. Note that g_m (transconductance gain) is a function of the bias current, I_A. An S-G shaping filter implementation using OTAs is greatly advantageous, since programmable characteristics are providing. In particular, tunability is achieved by replacing the *RC* and *CR* sections in the original passive model with active g_m-*C* sections, where the g_m can be adjusted with an external bias voltage or current. The 2nd order shaping filter that was designed using the above SFG and the leapfrog method is shown in Fig.6. The capacitor values and the OTA transconductances of the above S-G shaper are given in Table I. The shaper configuration was designed in order to provide a peaking time equal to 1.8 μs, which refer to a BW of 260 kHz in the low frequency region (f_{cl} = 140 Hz). The passive element values of the respective RLC two port network of Fig.3 are given in Table I.

Table 1: IC shaper and RLC network element values

IC Shaper		Discrete RLC Network	
Active and Passive Elements		Passive Elements	
g_{m1}	23.8 μA/V	*R*s	100 kΩ
g_{m2}	11.5 μA/V	R_L	100 kΩ
g_{m3}	950 nA/V	C_1	10.33 pF
C_1	12.36 pF	C_2	7.44 nF
C_2	1.00 nF	*L*	83.7 mH
C_3	13.77 pF		

Because of the non-integrable value of C_2 in the leapfrog shaper, the specific capacitance was substituted with a grounded OTA-C capacitor simulator. The respective OTA architecture is described in Fig.7 and its calculated value is shown below [11], [13]. The values of the transconductances and the capacitor *C* are $g_{m4}=g_{m5}=g_{m6}=74.4$ μA/V, $g_{m7}=950$ nA/V and *C* = 12.8 pF.

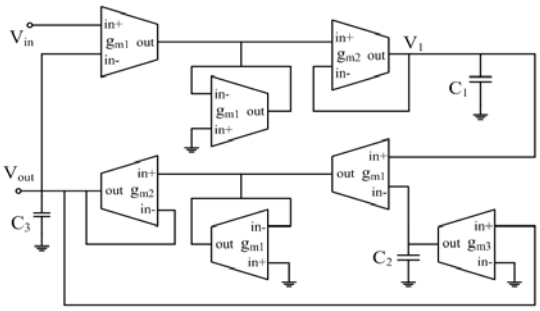

Figure 6: OTA based 2nd order S-G shaper using the leapfrog technique

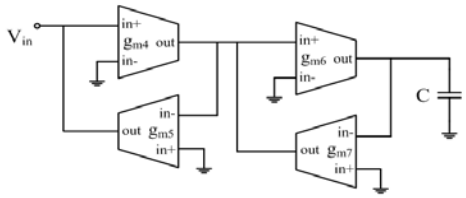

Figure 7:OTA based architecture for grounded capacitance simulation

$$C_{eq}=C\frac{g_{m4}g_{m5}}{g_{m6}g_{m7}} \quad (14)$$

Drawback of the shaper topology and specifically of the leapfrog design method is the 0.5 gain, an inherent loss of the specific technique [11], [13]. In order to cope with this loss, additional gain stage was used between the CSA and the shaper, using an OTA based structure (g_{m8}=153μA/V, g_{m9}=11.5μA/V) and is shown in Fig.8. This topology gives capability to program externally the gain by fixing the bias of the two OTA cells. The respective DC gain is given by 15.

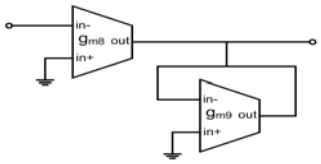

Figure 8: OTA based amplification stage

$$A = \frac{V_O}{V_I} = \frac{g_{m8}}{g_{m9}} \quad (15)$$

IV. Fully Integrated Readout System

The total IC readout analog processor was designed – simulated and fabricated in a 0.35 μm CMOS process (3M/2P 3.3/5V) by Austria Mikro Systeme (AMS) for a specific low energy X-rays silicon strip detector [14].

In the VLSI readout architecture, the power supplies are $V_{DD} = -V_{SS} = 1.65$ V. Considering the system pre-amplification stage (Fig.1), the feedback capacitance C_f is 550 fF and is placed between the input node and the gate of the source follower stage to avoid introduction on the closed loop of the follower stage complex poles and to isolate the C_f from the following stage. The bias current I_{bias} was selected to be 10 μA. The reset device bias voltage is fixed to 150 mV and the level shifting bias voltage is equal to -1.18 V. The dimensions of the CSA MOS devices are given in [14]-[15]. Considering the S-G OTA based shaping architecture, capacitor simulator and amplification topology, they were implemented using a CMOS OTA design, shown in Fig.9. In the transconductance circuit, a typical CMOS cascade configuration is used, where changing the bias voltage results in approximately equal changes for both the transconductance and the 3-dB frequency.

The total simplified block diagram of the analog readout ASIC is given in Fig.10. A photograph of the fabricated prototype chip where the above readout system was contained is shown in Fig.11.

V. Expiremental results

The measured X-ray IC front end system output signal is shown in Fig.12. The system provides dc gain equal to 120 dB. However this value can be externally modified by

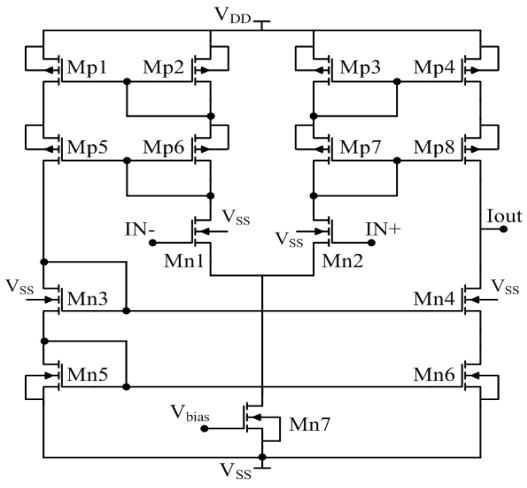

Figure 9: CMOS operational transconductance amplifier.

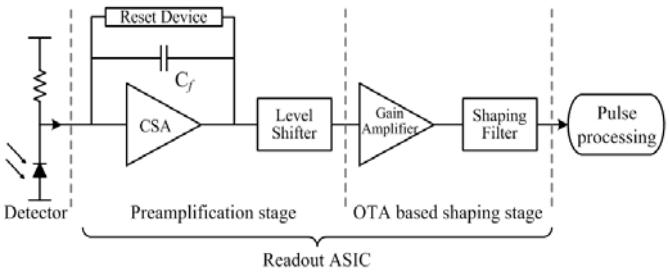

Figure 10:Block diagram of the IC readout system

fixing suitably the bias voltages and consequently changing the g_m values of the OTA based amplification topology. Regarding the application specifications, the output pulse has a peaking time value of 1.81 μs that shows no undershoot or pile up. The power consumption is 998 μW, far lower than the maximum allowed specified value of 8 mW, rendering the system as low power. The readout ASIC noise performance was also analytically studied. The system enc is 382 e− for a detector of 2 pF and noise performance increases with a slope of 21 e−/pF. The *enc* dependence on the detector capacitance variations is shown in Fig.13. Considering the front end system energy resolution – linearity, it is presented is Fig.14. The CMOS readout analog processor achieves an input charge gain-voltage output conversion of 3.31 mV/fC and a linearity of 0.69%. In terms of the total occupied area, the specific IC system is again advantageous since it consumes only 201743 μm^2 of a total 2983 μm × 2983 μm microchip (Fig.11).

Finally, another great advantage of the specific topology, and in particular of the proposed design methodology having OTAs as the architecture building cells, is the flexibility of the implementation. Both 3-dB frequencies of the system band-pass AC response can be externally modified. As a result the operating bandwidth and consequently the output pulse peaking time and the signal undershoot can be externally adjusted in relation to the application. The output noise can be regulated in relation to each application, since the output signal can have an undershoot (narrow BW) or not

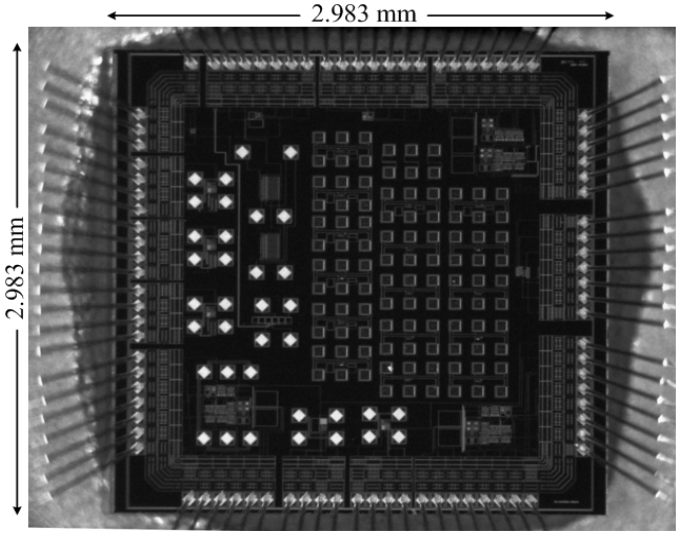

Figure 11: Microphotograph of the full fabricated microchip

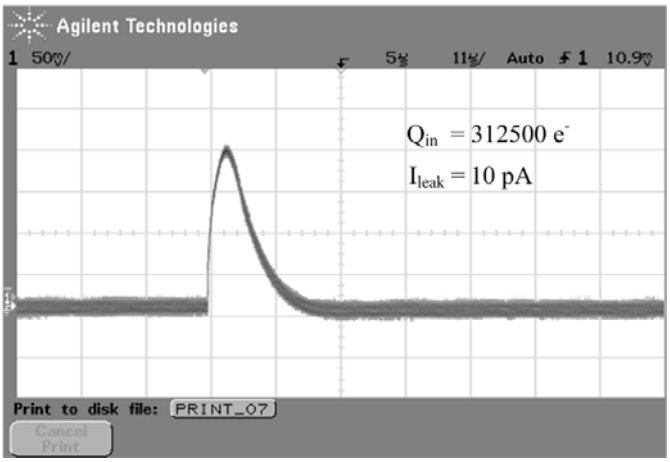

Figure 12:Readout system output pulse.

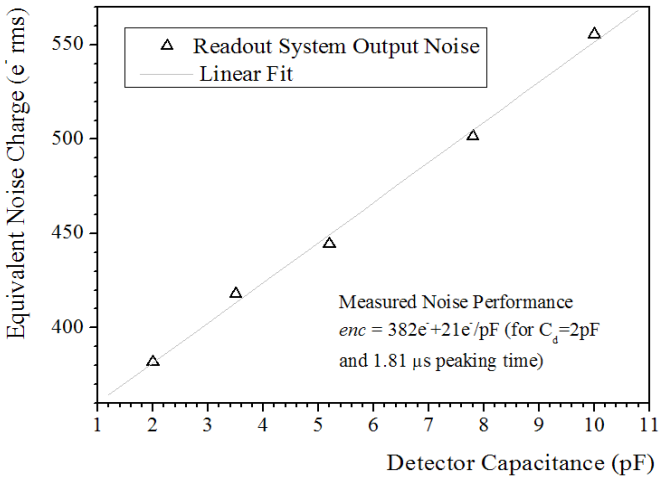

Figure 13: Readout ASIC *enc* dependence on the detector capacitance.

(wide BW) in relation to the necessitated noise performance. In addition, the DC gain performance can also be modified due to the additional OTA based gain topology. However, the range where the gain can be controlled is relatively small since the preamplifier is the main system gain contributor. The above capabilities indicate the architecture as suitable for a variety of readout application since the system performance can be programmable in order to best meet the speed requirements and the noise specification of the application.

VI. Conclusion and Discussion

Using the leapfrog filter design methodology and the Semi Gaussian shaping theory an advanced front end analog processor for a particular X-rays radiation detector was proposed. In the specific ASIC a novel shaping filter topology based on operational transconductance amplifiers is addressed. The total IC readout system compatibility to the stringent nuclear spectroscopy requirements is examined performing measurements that confirm its satisfactory performance. The architecture although it provides a relatively long peaking time, is fully integrated and appears to be greatly flexible since the use of OTAs as the topology building cells results to externally adjustable characteristics.

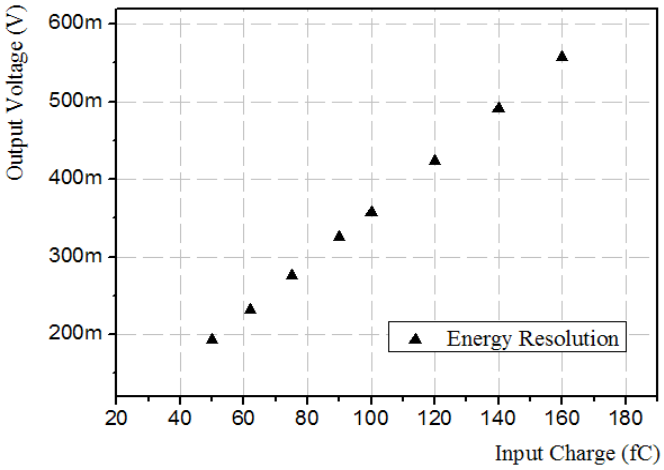

Figure 14: Readout ASIC measured energy response

Acknowledgment

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